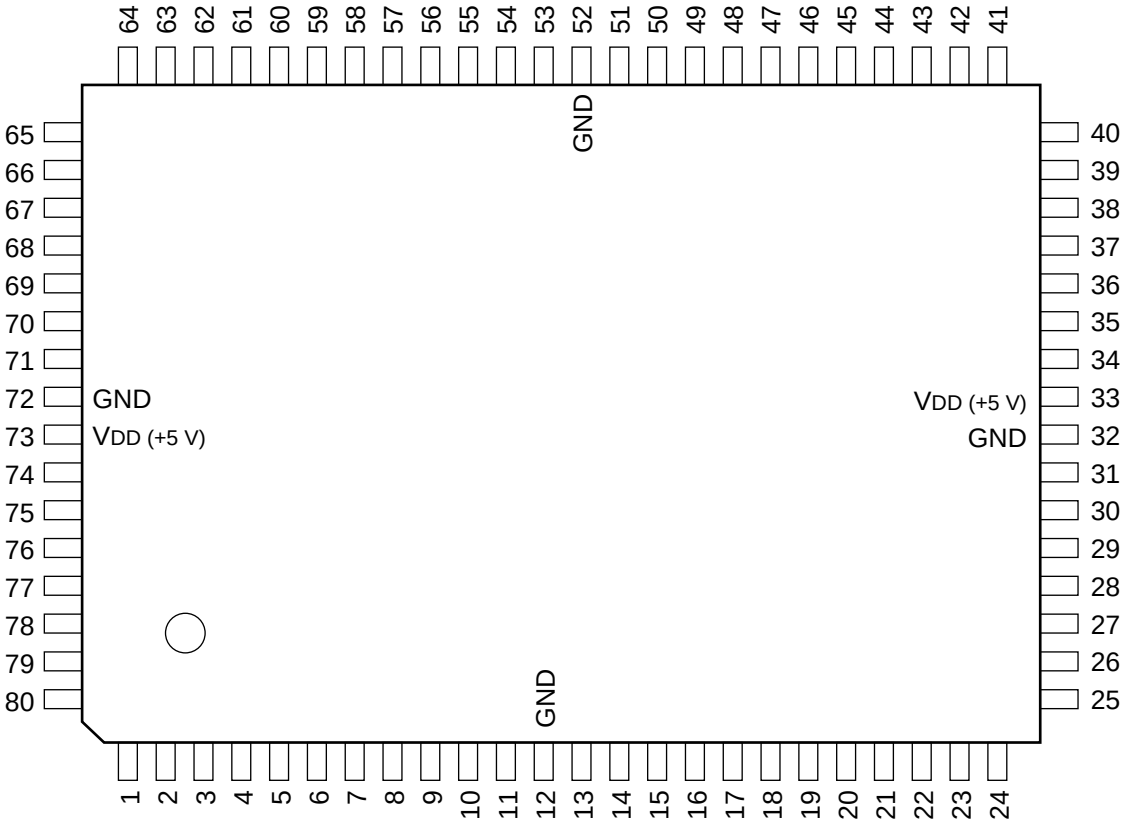
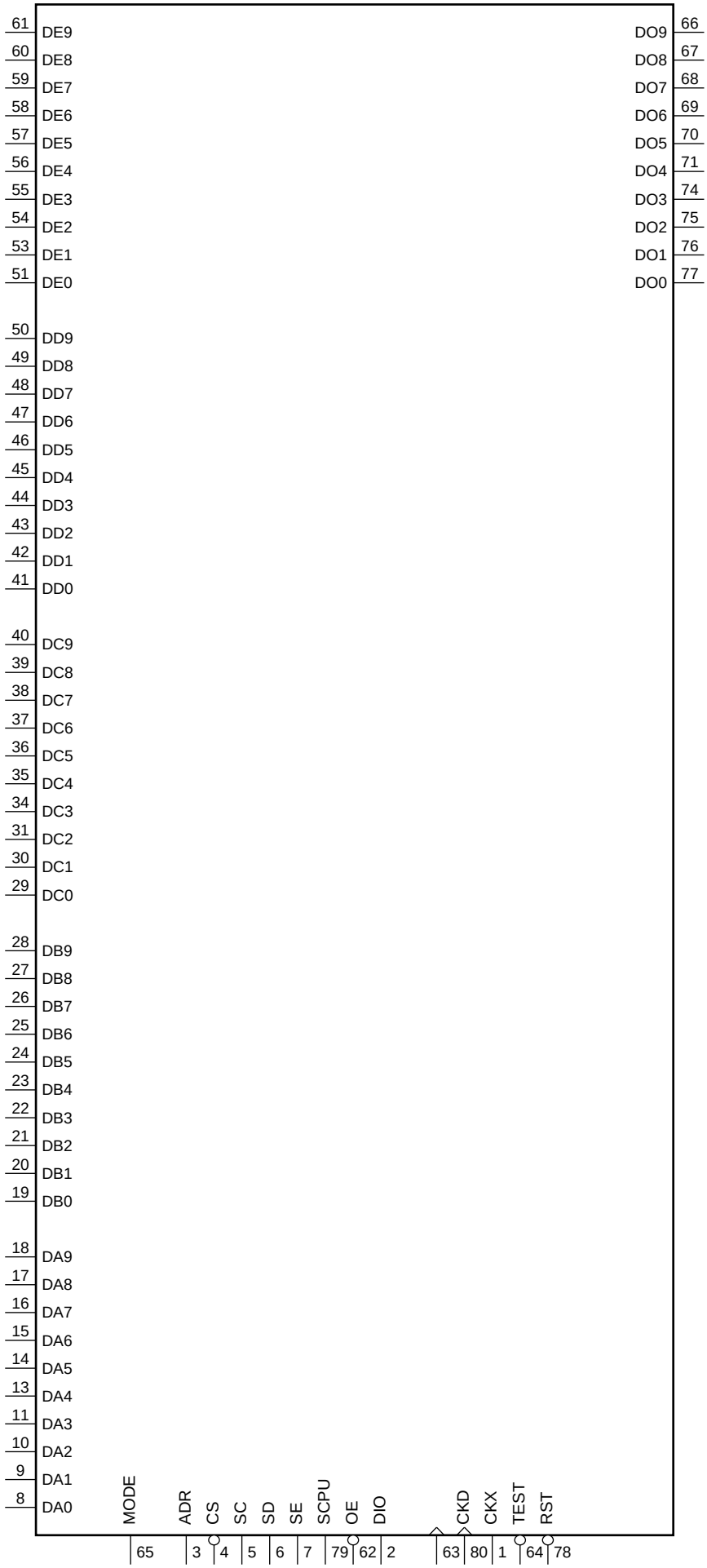
C-MOS NAM CROSS POINT

—TOP VIEW—



PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	I	CKX	21	I	DB2	41	I	DD0	61	I	DE9
2	I/O	DIO	22	I	DB3	42	I	DD1	62	I	OE
3	I	ADR	23	I	DB4	43	I	DD2	63	I	CK
4	I	CS	24	I	DB5	44	I	DD3	64	I	TEST
5	I	SC	25	I	DB6	45	I	DD4	65	I	MODE
6	I	SD	26	I	DB7	46	I	DD5	66	O	DO9
7	I	SE	27	I	DB8	47	I	DD6	67	O	DO8
8	I	DA0	28	I	DB9	48	I	DD7	68	O	DO7
9	I	DA1	29	I	DC0	49	I	DD8	69	O	DO6
10	I	DA2	30	I	DC1	50	I	DD9	70	O	DO5
11	I	DA3	31	I	DC2	51	I	DE0	71	O	DO4
12	—	GND	32	—	GND	52	—	GND	72	—	GND
13	I	DA4	33	—	V_{DD}	53	I	DE1	73	—	V_{DD}
14	I	DA5	34	I	DC3	54	I	DE2	74	O	DO3
15	I	DA6	35	I	DC4	55	I	DE3	75	O	DO2
16	I	DA7	36	I	DC5	56	I	DE4	76	O	DO1
17	I	DA8	37	I	DC6	57	I	DE5	77	O	DO0
18	I	DA9	38	I	DC7	58	I	DE6	78	I	RST
19	I	DB0	39	I	DC8	59	I	DE7	79	I	SCPU
20	I	DB1	40	I	DC9	60	I	DE8	80	I	CKD



INPUT

CK ; SYSTEM CLOCK
CKD ; SERIAL INTERFACE CLOCK
CKX ; SWITCHING TIMING PULSE
DA0-DA9 ; 10-BIT DIGITAL IN (CH A)
DB0-DB9 ; 10-BIT DIGITAL IN (CH B)
DC0-DC9 ; 10-BIT DIGITAL IN (CH C)
DD0-DD9 ; 10-BIT DIGITAL IN (CH D)
DE0-DE9 ; 10-BIT DIGITAL IN (CH E)
MODE ; MODE SELECT
LOW : 1 INPUT MODE (2CK DELAY MODE)
HIGH: 5 INPUT MODE
RST ; RESET PULSE
SCPU ; SELECT CPU
LOW : MANUAL MODE
HIGH: SERIAL INTERFACE MODE
TEST ; TEST MODE (LOW: TEST)

<SERIAL INTERFACE MODE>
ADR ; ADDRESS
CS ; CHIP SELECT
SC ; NOT USED
SD ; NOT USED
SE ; NOT USED

<MANUAL MODE>
ADR ; SELECT CH A
CS ; SELECT CH B
SC ; SELECT CH C
SD ; SELECT CH D
SE ; SELECT CH E

OUTPUT

DO0-DO9 ; 10-BIT DIGITAL OUT

INPUT/OUTPUT

DIO ; SERIAL DATA