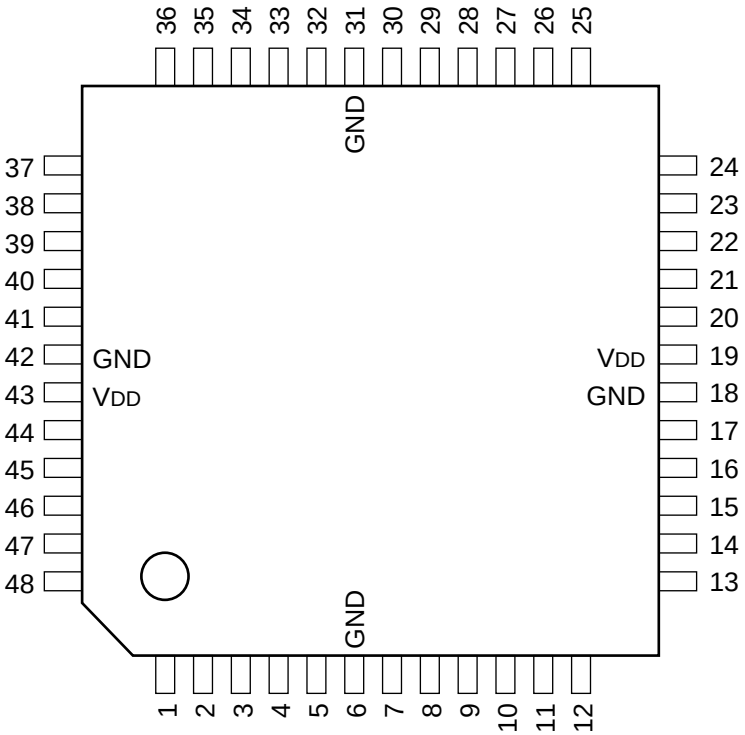
C-MOS MEMORY CONTROL

—TOP VIEW—



PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	I/O	D7/PA4	13	I/O	C4/PD4	25	O	B2	37	I	CK1
2	I/O	D6/PA3	14	I/O	C3/PD3	26	O	B1/PLS3	38	I	CK2
3	I/O	D5/PA2	15	I/O	C2/PD2	27	I/O	B0/EN3	39	I	CK3
4	I/O	D4/PA1	16	I/O	C1/PD1	28	I/O	A7/LD3	40	I	CK4
5	I/O	D3/PDB	17	I/O	C0/PD0	29	O	A6/PLS2	41	I	CKX
6	—	GND	18	—	GND	30	I/O	A5/EN2	42	—	GND
7	I/O	D2/PDA	19	—	VDD	31	—	GND	43	—	VDD
8	I/O	D1/PD9	20	I/O	B7/TEST	32	I/O	A4/LD2	44	I	RST
9	I/O	D0/PD8	21	O	B6/PLS4	33	O	A3/PLS1	45	I	CKD
10	I/O	C7/PD7	22	I/O	B5/EN4	34	I/O	A2/EN1	46	I/O	DIO
11	I/O	C6/PD6	23	I/O	B4/LD4	35	I/O	A1/LD1	47	I	ADR
12	I/O	C5/PD5	24	O	B3	36	O	A0	48	I	CS

MODE*	FUNCTION
MOD 0	4 CHANNEL (CH1 TO CH4) CYCLIC PULSE GENERATORS
MOD 1	2 CHANNEL (CH1 AND CH2) CYCLIC PULSE GENERATORS 1 CHANNEL (CH3) CLOCK FREQUENCY COUNTER
MOD 2	2 CHANNEL (CH1 AND CH2) CYCLIC PULSE GENERATORS 2 CHANNEL (CHC AND CHD) 8-BIT SERIAL TO PARALLEL CONVERTOR
MOD 3	4 CHANNEL (CHA TO CHD) 8-BIT SERIAL TO PARALLEL CONVERTOR

* THESE 4 MODE CONTROLS ARE DETERMINED AT MODE REGISTER.

<COMMON TERMINALS FOR ALL FUNCTION>

INPUT

ADR ; SERIAL ADDRESS
CKD ; SERIAL INTERFACE CLOCK
CKX ; SWITCHING TIMING PULSE
CS ; CHIP SELECT (LOW : ACTIVE)
RST ; RESET PULSE (LOW : RESET REGISTERS)

INPUT/OUTPUT

DIO ; SERIAL DATA
(MODE CONTROL DATA, REGISTER DATA IN
CH3 CLOCK FREQUENCY COUNTER DATA OUT)

<TERMINALS FOR CYCLIC PULSE GENERATORS>

INPUT

CK1-CK4 ; SYSTEM CLOCK FOR 12-BIT COUNTER OF CH1-CH4
EN1-EN4 ; ENABLE IN FOR 12-BIT COUNTER OF CH1-CH4
LD1-LD4 ; LOAD IN FOR 12-BIT COUNTER OF CH1-CH4

OUTPUT

PLS1-PLS4 ; PULSE OUT (CARRY OUTPUT) OF CH1-CH4

<TERMINALS FOR 8-BIT SERIAL TO PARALLEL CONVERTORS>

OUTPUT

A7-A0 ; 8-BIT PARALLEL DATA OUT OF CHA
B7-B0 ; 8-BIT PARALLEL DATA OUT OF CHB
C7-C0 ; 8-BIT PARALLEL DATA OUT OF CHC
D7-D0 ; 8-BIT PARALLEL DATA OUT OF CHD