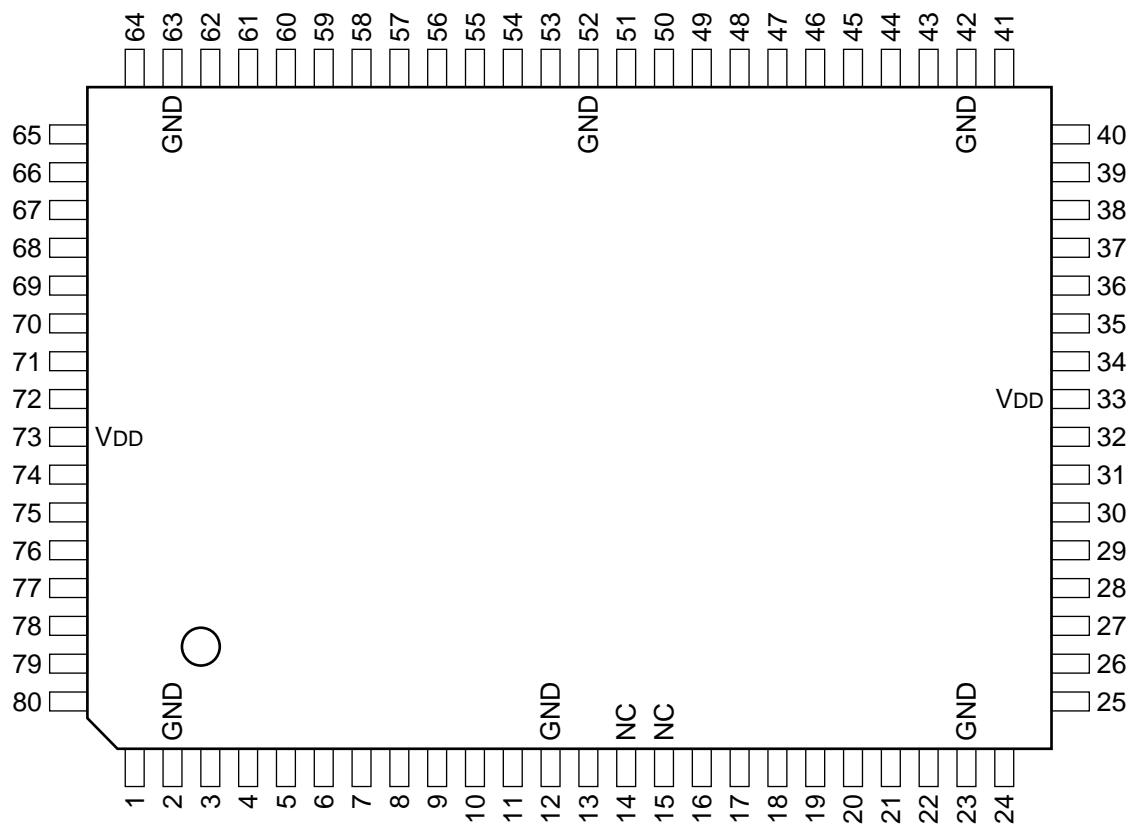


C-MOS SOLID GENERATOR

—TOP VIEW—



PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	I	CK	21	I	\overline{CS}	41	I	SEL0	61	I	A0
2	—	GND	22	I	CKX	42	—	GND	62	I	AEM3
3	O	P11	23	—	GND	43	I	SEL1	63	—	GND
4	O	P10	24	I	CKD	44	I	SEL2	64	I	AEM2
5	O	P9	25	I	B13	45	O	PM11	65	I	AEM1
6	O	P8	26	I	B12	46	O	PM10	66	I	AE0
7	O	P7	27	I	B11	47	O	PM9	67	I	AM1
8	O	P6	28	I	B10	48	O	PM8	68	I	AM2
9	O	P5	29	I	B9	49	O	PM7	69	I	AM3
10	O	P4	30	I	B8	50	O	PM6	70	I	AM4
11	O	P3	31	I	B7	51	O	PM5	71	I	AM5
12	—	GND	32	I	B6	52	—	GND	72	I	AM6
13	O	PM12	33	—	VDD	53	O	PM4	73	—	VDD
14	—	NC	34	I	B5	54	O	PM3	74	I	AM7
15	—	NC	35	I	B4	55	O	PM2	75	I	AM8
16	I	SRIL	36	I	B3	56	O	PM1	76	I	AM9
17	I	RNDL	37	I	B2	57	O	P0	77	I	AM10
18	I	ADR	38	I	B1	58	O	P1	78	I	AM11
19	I/O	DIO	39	I	B0	59	O	P2	79	I	AM12
20	I	\overline{RCS}	40	I	DCTL	60	I	\overline{OE}	80	I	AM13

INPUT

A0, AM1 - AM13	; MANTISSA OF FLOWTING-POINT REPRESENTATION
ADR	; SERIAL ADDRESS
AE0, AEM1 - AEM3	; EXPONENT OF FLOWTING-POINT REPRESENTATION
B0 - B13	; FIXED-POINT REPRESENTATION
CK	; SYSTEM CLOCK
CKD	; SERIAL INTERFACE CLOCK
CKX	; SWITCHING TIMING PULSE
\overline{CS}	; CHIP SELECT (LOW : ACTIVE)
DCTL	; DELAY CONTROL OF B0 - B13 INPUT (LOW : ACTIVE)
\overline{OE}	; OUTPUT ENABLE (LOW : ENABLE)
RNDL	; MULTIPLIER ROUNDING CONTROL (LOW : ACTIVE)
SEL0, SEL1	; SEL (0, 1) = (0, 0) BYPASS A (A IN → P OUT) = (0, 1) BYPASS B (B IN → P OUT) = (1, 0) P = A × B = (1, 1) P = A × B
SEL2	; DELAY CONTROL OF P2 - PM12 OUTPUT (HIGH : ACTIVE)
SRIL	; SERIAL CONTROL ENABLE (LOW : ACTIVE)

OUTPUT

P0 - P11, PM1 - PM12	; MULTIPLIER OUTPUT (SOLID DATA : P2 - P0, PM1 - PM12)
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INPUT / OUTPUT

DIO	; SERIAL DATA
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