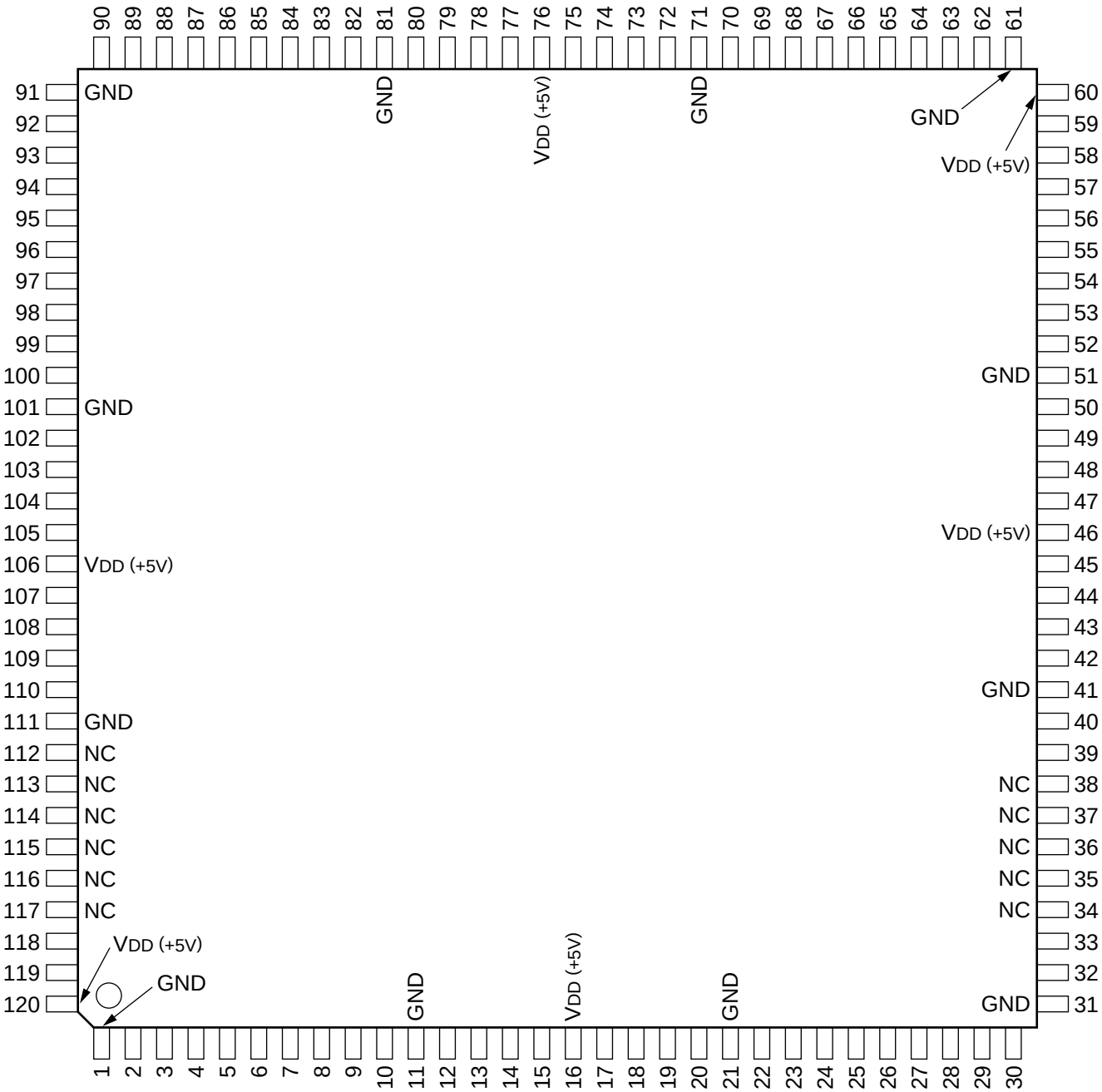
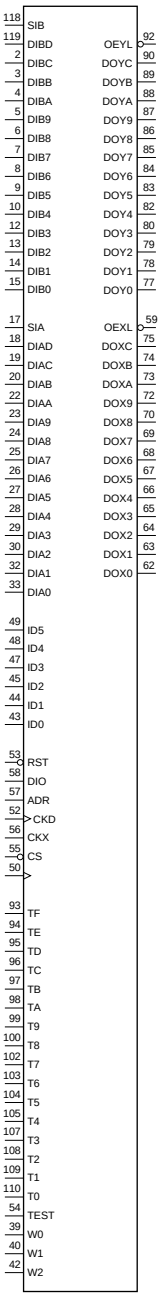
C-MOS KEY PROCESSOR

-TOP VIEW-



PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	—	GND	31	—	GND	61	—	GND	91	—	GND
2	I	DIBC	32	I	DIA1	62	O	DOX0	92	I	$\overline{\text{OEYL}}$
3	I	DIBB	33	I	DIA0	63	O	DOX1	93	I	TF
4	I	DIBA	34	—	NC	64	O	DOX2	94	I	TE
5	I	DIB9	35	—	NC	65	O	DOX3	95	I	TD
6	I	DIB8	36	—	NC	66	O	DOX4	96	I	TC
7	I	DIB7	37	—	NC	67	O	DOX5	97	I	TB
8	I	DIB6	38	—	NC	68	O	DOX6	98	I	TA
9	I	DIB5	39	I	WA0	69	O	DOX7	99	I	T9
10	I	DIB4	40	I	WA1	70	O	DOX8	100	I	T8
11	—	GND	41	—	GND	71	—	GND	101	—	GND
12	I	DIB3	42	I	WA2	72	O	DOX9	102	I	T7
13	I	DIB2	43	I	ID0	73	O	DOXA	103	I	T6
14	I	DIB1	44	I	ID1	74	O	DOXB	104	I	T5
15	I	DIB0	45	I	ID2	75	O	DOXC	105	I	T4
16	—	V_{DD}	46	—	V_{DD}	76	—	V_{DD}	106	—	V_{DD}
17	I	SIA	47	I	ID3	77	O	DOY0	107	I	T3
18	I	DIAD	48	I	ID4	78	O	DOY1	108	I	T2
19	I	DIAC	49	I	ID5	79	O	DOY2	109	I	T1
20	I	DIAB	50	I	CK	80	O	DOY3	110	I	T0
21	—	GND	51	—	GND	81	—	GND	111	—	GND
22	I	DIAA	52	I	CKD	82	O	DOY4	112	—	NC
23	I	DIA9	53	I	$\overline{\text{RST}}$	83	O	DOY5	113	—	NC
24	I	DIA8	54	I	TEST	84	O	DOY6	114	—	NC
25	I	DIA7	55	I	$\overline{\text{CS}}$	85	O	DOY7	115	—	NC
26	I	DIA6	56	I	CKX	86	O	DOY8	116	—	NC
27	I	DIA5	57	I	ADR	87	O	DOY9	117	—	NC
28	I	DIA4	58	I/O	DIO	88	O	DOYA	118	I	SIB
29	I	DIA3	59	I	$\overline{\text{OEXL}}$	89	O	DOYB	119	I	DIBD
30	I	DIA2	60	—	V_{DD}	90	O	DOYC	120	—	V_{DD}



INPUT

ADR ; SERIAL ADDRESS
CK ; SYSTEM CLOCK
CKD ; SERIAL INTERFACE CLOCK
CKX ; SWITCHING TIMING PULSE
$\overline{CS}$; CHIP SELECT (LOW : ACTIVE)
DIAA-DIAD,
DIA0-DIA9 ; DATA A IN
DIBA-DIBD,
DIB0-DIB9 ; DATA B IN
$\overline{RST}$; RESET
ID0-ID5 ; IC ADDRESS SELECT
SIA, SIB ; SIGN BIT OF "A", "B" IN
$\overline{OEXL}$, $\overline{OEYL}$; ENABLE CONTROL OF "X", "Y" OUT (LOW : ENABLE)
TA-TF,
T0-T9 ; TEST TERMINAL
W0-W2 ; MODE SELECT FOR TEST

OUTPUT

DOXA-DOXC,
DOX0-DOX9 ; DATA X OUT
DOYA-DOYC,
DOY0-DOY9 ; DATA Y OUT

INPUT/OUTPUT

DIO ; SERIAL DATA