

INPUT

CKC	: XH1 ACTIVE EDGE DECISION
CLK	: SYSTEM CLOCK
CR	: COMPENSATION DATA SELECT (H : μ -COM MODE, L : NORMAL MODE)
D0-D3	: 4-BIT PARALLEL DATA
DCK	: DATA INPUTS STROBE PULSE
EIAD	: H : EXT ADDRESS, L : INT ADDRESS
FDFM	: FRAME READ/FIELD READ : SWITCH (H : FIELD READ)
HD	: HORIZONTAL DRIVE
INVI	: INVERTER
SP	: INPUT DATA SERIAL/PARALLEL SWITCH (H : SERIAL)
TST1 - TST3	: TEST MODE SELECT
VD	: VERTICAL DRIVE
XH1	: CLOCK FOR COMPENSATION DATA
XV1	: LINE COUNTER INPUT TERMINAL

OUTPUT

A4 - A6	: DATA ADDRESS
GP1 - GP3	: GATE PULSE FOR COMPENSATION DATA (R, G, B-CH)
INVO	: INVERTER
PRTY	: 12-BIT DATA PARITY CHECK (H : EVEN)
TO0 - TO9	: TEST TERMINAL FOR INTERNAL DATA OUTPUTS
XVCT	: ROM POWER VOLTAGE CONTROL TERMINAL

INPUT/OUTPUT

A0 - A3	: DATA ADDRESS OUTPUTS (DATA ADDRESS INPUTS ; μ -COM MODE)
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