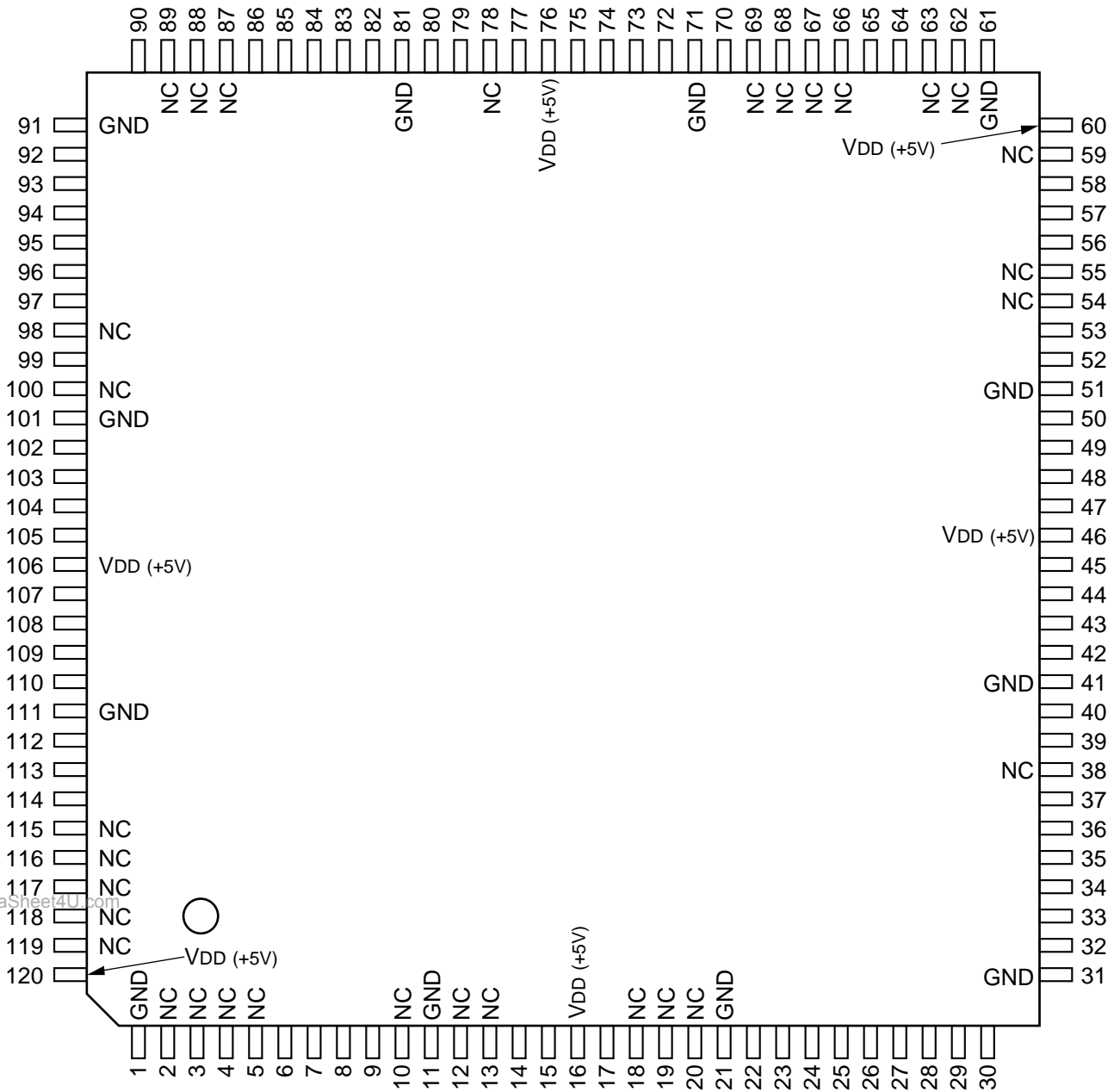

C-MOS SAMPLING RATE CONVERSION FILTER

—TOP VIEW—



PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	—	GND	41	—	GND	81	—	GND
2	—	NC	42	O	DO2	82	I	A3
3	—	NC	43	O	DO3	83	I	A2
4	—	NC	44	O	DO4	84	I	A1
5	—	NC	45	O	DO5	85	I	A0
6	I	SI0	46	—	VDD	86	I	EXTA
7	I	SI1	47	O	DO6	87	—	NC
8	I	SI2	48	O	DO7	88	—	NC
9	I	SI3	49	O	DO8	89	—	NC
10	—	NC	50	O	DO9	90	O	DOEN
11	—	GND	51	—	GND	91	—	GND
12	—	NC	52	O	DO10	92	I	TSA0
13	—	NC	53	O	DO11	93	I	TSA1
14	I	AISA	54	—	NC	94	I	TSA2
15	I	AISB	55	—	NC	95	I	MRSC
16	—	VDD	56	I	FI0	96	I	TESTH
17	I	PRINV	57	I	FI1	97	I	DDOTS
18	—	NC	58	I	FI2	98	—	NC
19	—	NC	59	—	NC	99	I	CLK1
20	—	NC	60	—	VDD	100	—	NC
21	—	GND	61	—	GND	101	—	GND
22	O	SO0	62	—	NC	102	I	DI10
23	O	SO1	63	—	NC	103	I	DI9
24	O	SO2	64	I	SYSEL	104	I	DI8
25	O	SO3	65	I	RMODE	105	I	DI7
26	I	TD0	66	—	NC	106	—	VDD
27	I	TD1	67	—	NC	107	I	DI6
28	I	TD2	68	—	NC	108	I	DI5
29	I	TD3	69	—	NC	109	I	DI4
30	I	TD4	70	I	CLK2	110	I	DI3
31	—	GND	71	—	GND	111	—	GND
32	I	TD5	72	I	CALT	112	I	DI2
33	I	TD6	73	—	NC	113	I	DI1
34	I	TD7	74	I	OBDSEL	114	I	DI0
35	I	TD8	75	I	OBFRST	115	—	NC
36	I	TD9	76	—	VDD	116	—	NC
37	I	TD10	77	I	EXSEN	117	—	NC
38	—	NC	78	—	NC	118	—	NC
39	O	DO0	79	I	A5	119	—	NC
40	O	DO1	80	I	A4	120	—	VDD

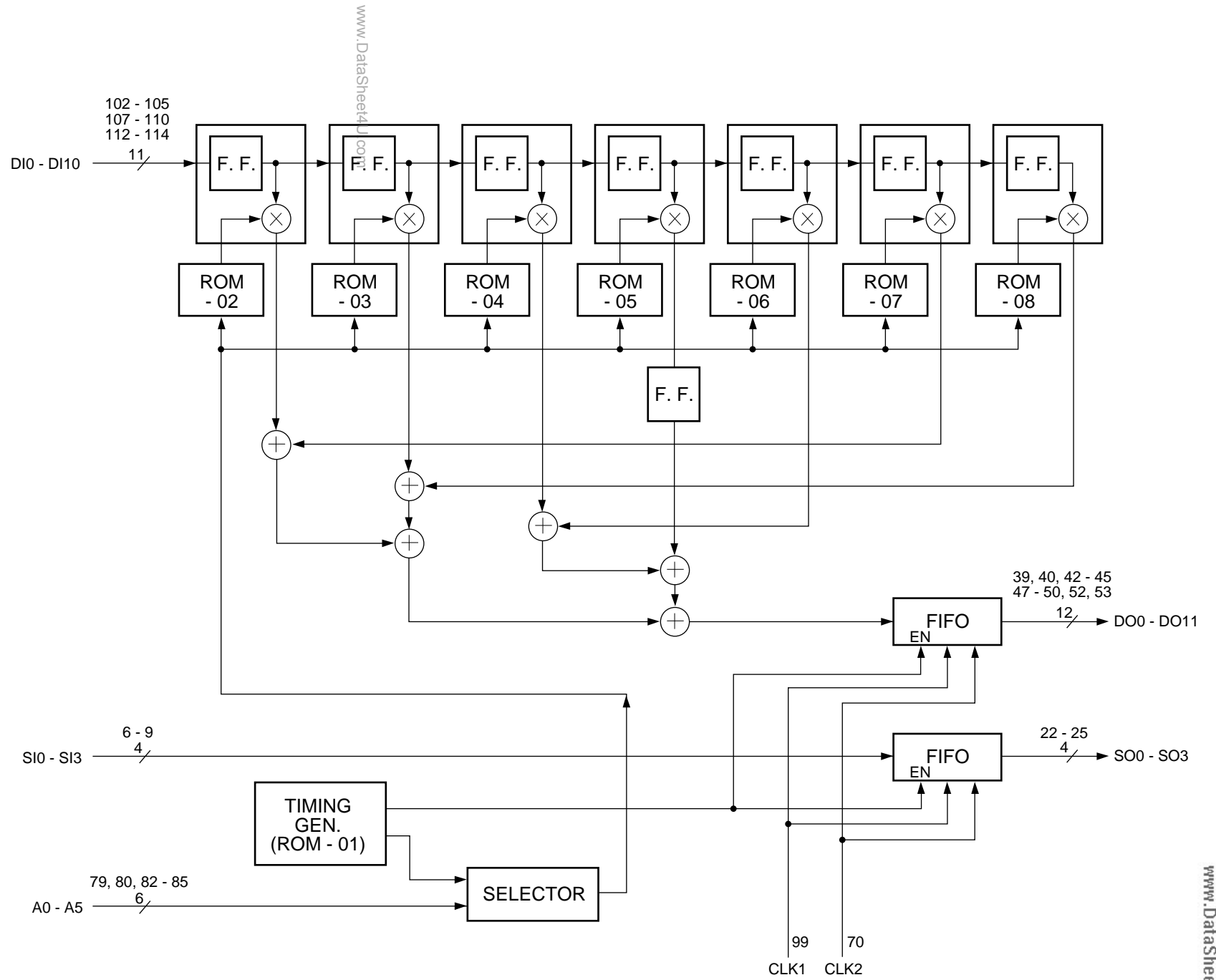
102	DI10	DO11	53
103	DI9	DO10	52
104	DI8	DO9	50
105	DI7	DO8	49
107	DI6	DO7	48
108	DI5	DO6	47
109	DI4	DO5	45
110	DI3	DO4	44
112	DI2	DO3	43
113	DI1	DO2	42
114	DI0	DO1	40
		DO0	39
9	SI3		
8	SI2	SO3	25
7	SI1	SO2	24
6	SI0	SO1	23
		SO0	22
79	A5		
80	A4		
82	A3	DOEN	90
83	A2		
84	A1	TD10	37
85	A0	TD9	36
		TD8	35
58	FI2	TD7	34
57	FI1	TD6	33
56	FI0	TD5	32
		TD4	30
14	AISA	TD3	29
15	AISB	TD2	28
		TD1	27
17	PRINV	TD0	26
65	RMODE		
64	CYSEL	TSA2	94
72	CALT	TSA1	93
77	EXSEN	TSA0	92
86	EXTA		
95	MRSC	TESTH	96
70	CLK2	DDOTS	97
99	CLK1		
74	OBDSEL		
75	OBFRST		

INPUT

A0 - A5	; EXT. ADDRESS
AISA	; ADDRESS COUNTER A RESET
AISB	; ADDRESS COUNTER B RESET
CALT	; PHASE OF INPUT DATA OF CHROMA
CLK1	; INPUT SAMPLING CLOCK
CLK2	; OUTPUT SAMPLING CLOCK
CYSEL	; Y/C SELECT (L: LUMINANCE)
DDOTS	; TEST FIFO
DI0 - DI10	; VIDEO DATA
EXSEN	; DATA SHIFT ENABLE
EXTA	; EXT. ADDRESS MODE SELECT
FI0 - FI2	; FIFO START ADDRESS SET
MRSC	; OUTPUT CODE (L: OFFSET BINARY) (H: 2's COMPLIMENT)
OBDSEL	; OUTPUT RESET TIMING
OBFRST	; INPUT RESET TIMING
PRINV	; H: INVERT OF ALT PULSE PHASE
RMODE	; L: D1 TO D2, H: D2 TO D1
SI0 - SI3	; AUX. DATA
TD0 - TD10	; TEST DATA
TESTH	; TEST MULTIPLIER
TSA0 - TSA2	; TEST MULTIPLIER

OUTPUT

DO0 - DO11	; VIDEO DATA
DOEN	; TEST FIFO
SO0 - SO3	; AUX. DATA



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