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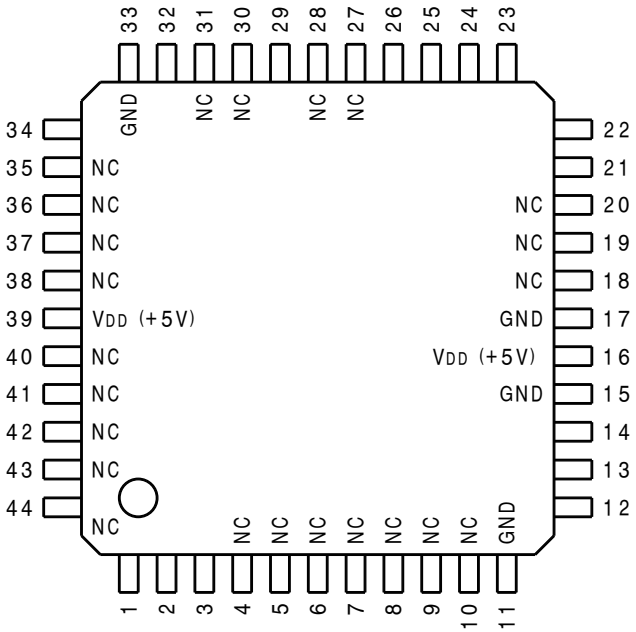
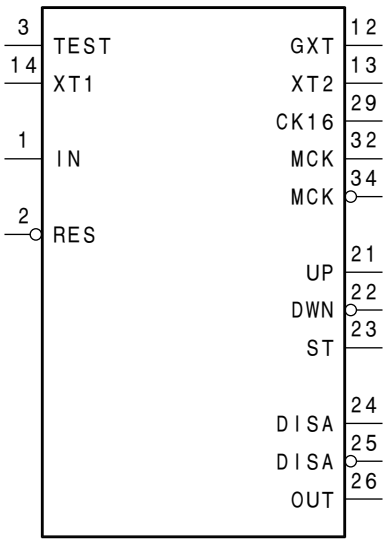
C-MOS BREAK SIGNAL DETECTOR

-TOP VIEW-



PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	I	IN	12	O	GXT	23	O	ST	34	O	$\overline{MCK}$
2	I	$\overline{RES}$	13	O	XT2	24	O	DISA	35	–	NC
3	I	TEST	14	I	XT1	25	O	$\overline{DISA}$	36	–	NC
4	–	NC	15	–	GND	26	O	OUT	37	–	NC
5	–	NC	16	–	VDD	27	–	NC	38	–	NC
6	–	NC	17	–	GND	28	–	NC	39	–	VDD
7	–	NC	18	–	NC	29	O	CK16	40	–	NC
8	–	NC	19	–	NC	30	–	NC	41	–	NC
9	–	NC	20	–	NC	31	–	NC	42	–	NC
10	–	NC	21	O	UP	32	O	MCK	43	–	NC
11	–	GND	22	O	$\overline{DWN}$	33	–	GND	44	–	NC



INPUT

$\overline{\text{IN}}$	;START-STOP SYNCHRO SIGNAL INPUT
$\overline{\text{RES}}$	;SYSTEM RESET INPUT
TEST	;FOR TEST INPUT, PULLDOWN TO THE INTERNAL GND
XT1	;SYSTEM CLOCK INPUT (9.83MHz)

OUTPUT

CK16	;OUTPUT THE 1/16 FREQUENCY FROM SYSTEM CLOCK
$\overline{\text{DISA}}$	;INVERSION SIGNAL OF DISA
DISA	;BREAK SIGNAL DETECTED :H DATA LINE MARKED :L
$\overline{\text{DWN}}$	;OUTPUT THE "L" PULSE WHEN DATA LINE IS FALL
GXT	;NC
$\overline{\text{MCK}}$	;INVERSION SIGNAL OF MCK
MCK	;SYSTEM CLOCK (9.83MHz)
OUT	;OR OUTPUT SIGNAL FROM IN TO INPUT SIGNAL AND THE DISA OUTPUT SIGNAL
ST	;1BIT DETECTOR PULSE OUTPUT FROM DATA
UP	;OUTPUT THE "H" PLUSE WHEN THE DATA LINE IS RISE
XT2	;INVERSION SIGNAL OF XT1