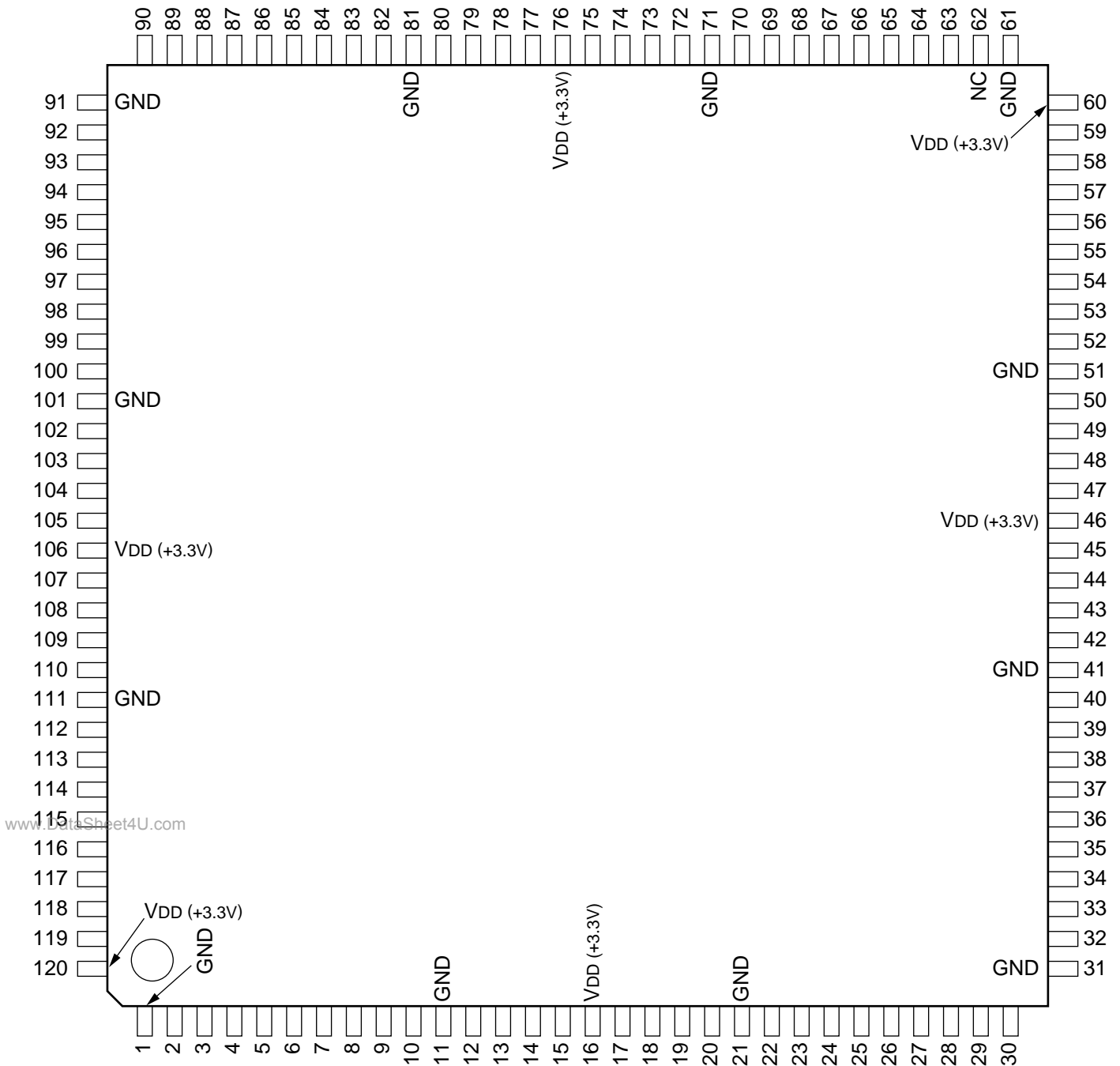


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# C-MOS DIGITAL RF INTERFACE

-TOP VIEW-



(VDD = +3.3V)

PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	—	GND	31	—	GND	61	—	GND	91	—	GND
2	O	ADVBDD0	32	I	CKCNFBDP	62	—	NC	92	I	CK64
3	O	ADVBDD1	33	I	CNFBDD3V	63	I	$\overline{\text{PRCDOFF}}$	93	I	RECACD0
4	O	ADVBDD2	34	I	CNFBDD2V	64	I	$\overline{\text{OEMPXD}}$	94	I	RECACD1
5	O	ADVBDD3	35	I	CNFBDD1V	65	I	$\overline{\text{OERECSD}}$	95	I	RECACD2
6	O	ADVBDD4	36	I	CNFBDD0V	66	I	TEST	96	I	RECACD3
7	O	CKADVBD	37	I	CKCNFACP	67	I	DLENSEL	97	I	RECBDD0
8	O	CNFACD0	38	I	CNFACD3V	68	I	EXTSTP	98	I	RECBDD1
9	O	CNFACD1	39	I	CNFACD2V	69	I	STARTSEL	99	I	RECBDD2
10	O	CNFACD2	40	I	CNFACD1V	70	I	DIVSEL	100	I	RECBDD3
11	—	GND	41	—	GND	71	—	GND	101	—	GND
12	O	CNFACD3	42	I	CNFACD0V	72	O	PRTYERR	102	I	RENA
13	O	CNFACD4	43	I	BDMUTE	73	I	$\overline{\text{CAM/ED}}$	103	I	RENB
14	O	CKCNFAC	44	I	CKBDV	74	I	$\overline{\text{EE/PB}}$	104	I	RENC
15	I	SATACEN	45	I	CANBDS	75	I	LTCH	105	I	REND
16	—	VDD	46	—	VDD	76	—	VDD	106	—	VDD
17	O	CNFBDD0	47	I	EDBDD3	77	I	RECACEL	107	I	FEENA
18	O	CNFBDD1	48	I	EDBDD2	78	I	RECBDSL	108	I	FEENB
19	O	CNFBDD2	49	I	EDBDD1	79	I	ADVACSL	109	I	PRTY
20	O	CNFBDD3	50	I	EDBDD0	80	I	ADVBDL	110	I	SATAC
21	—	GND	51	—	GND	81	—	GND	111	—	GND
22	O	CNFBDD4	52	I	CKACV	82	I	CNFACSL	112	O	ADVACD0
23	O	CKCNFBD	53	I	CAMACSD	83	I	CNFBDSL	113	O	ADVACD1
24	I	SATBDEN	54	I	EDACD3	84	I	BETACAM	114	O	ADVACD2
25	O	ODIVCK	55	I	EDACD2	85	I	ASEL0	115	O	ADVACD3
26	O	OSTPULSE	56	I	EDACD1	86	I	ASEL1	116	O	ADVACD4
27	O	MPX	57	I	EDACD0	87	I	ASEL2	117	O	CKADVAC
28	O	PECK	58	O	RECBDS	88	I	ASEL3	118	I	SATBD
29	O	PEDATA	59	O	RECACSD	89	O	CK16	119	I	RST
30	O	SVCNTERR	60	—	VDD	90	O	CK16	120	—	VDD

93	RECACD0	RECACSD	59
94	RECACD1		
95	RECACD2		
96	RECACD3		
97	RECBDD0	RECBDS0	58
98	RECBDD1		
99	RECBDD2		
100	RECBDD3		
65	OERECSD		
63	PRCDOFF		
110	SATAC		
118	SATBD		
15	SATACEN		
24	SATBDEN		
43	BDMUTE		
102	RENA	PRTYERR	72
103	RENB		
104	RENC		
105	REND		
109	PRTY		
75	LTCH		
57	EDACD0	ADVACD0	112
56	EDACD1	ADVACD1	113
55	EDACD2	ADVACD2	114
54	EDACD3	ADVACD3	115
53	CAMACSD	ADVACD4	116
52	CKACV	CKADVAC	117
50	EDBDD0	ADVBD0	2
49	EDBDD1	ADVBD1	3
48	EDBDD2	ADVBD2	4
47	EDBDD3	ADVBD3	5
45	CAMBDS0	ADVBD4	6
44	CKBDV	CKADVBD	7
42	CNFACD0V	CNFACD0	8
40	CNFACD1V	CNFACD1	9
39	CNFACD2V	CNFACD2	10
38	CNFACD3V	CNFACD3	12
37	CKCNFACP	CNFACD4	13
		CKCNFAC	14
36	CNFBDD0V	CNFBDD0	17
35	CNFBDD1V	CNFBDD1	18
34	CNFBDD2V	CNFBDD2	19
33	CNFBDD3V	CNFBDD3	20
32	CKCNFBDP	CNFBDD4	22
		CKCNFBD	23
73	CAM / ED		
74	EE / PB		
77	RECACSEL	SVCNTERR	30
78	RECBSEL		
79	ADVACSEL		
80	ADVBDSEL		
82	CNFACSEL		
83	CNFBSEL		
107	FEENA		
108	FEENB		
66	TEST	PEDATA	29
84	BETACAM	PECK	28
85	ASEL0		
86	ASEL1	MPX	27
87	ASEL2	ODIVCK	25
88	ASEL3	OSTPULSE	26
67	DLENSEL		
68	EXTSTP		
69	STARTSET		
70	DIVSEL		
64	OEMPXD		
92	CK64	CK16	90
119	RST	CK16	89

**INPUT**

ADVACSL, ADVBDSL : ADV HEAD OR AMPLIFIER SELECT  
 ASELO - ASEL3 : MPX DATA (RESERVE)  
 BDMUTE : BD REC MUTE FOR SAT  
 BETACAM : BETACAM MODE OR NONE SELECT  
 CAMACSD, CAMBDS0 : PB AC, BD DATA INPUT AT CAMCORDER MODE  
 CAM / ED : MODE SELECT EDITOR OR CAMCORDER  
 (0 : CAM, 1 : ED)  
 CK64 : 64MHZ CLOCK  
 CKACV, CKBDV : CLOCK FOR PB AC, BD DATA  
 CKCNFACP, CKCNFBDP : CLOCK FOR CONF AC, BD DATA  
 CNFACD3V - CNFACD0V : PB AC, BD DATA FROM CONF HEAD  
 CNFACSL, CNFBDSL : CONF HEAD OR AMPLIFIER SELECT  
 DIVSEL : MPX CK DIVID RETIO SELECT  
 DLENSEL : MPX DATA LENGTH SELECT (0 : 8-BIT, 1 : 17-BIT)  
 EE / PB : SELECT SYSTEM EE OR PR (0 : EE, 1 : PB)  
 EDACD3 - EDACD0, EDBDD3 - EDBDD0 : PB AC, BD DATA FROM ADVANCE HEAD  
 EXTSTP : MPX DATA SYNCHRONIZING SYSTEM SELECT  
 (0 : EXT, 1 : INT)  
 FEENA, FEENB : FE A, B HEAD ENABLE  
 LTCH : PARITY RESULT SY RECIEVED END SIGNAL INPUT  
 OEMPXD : MPX DATA AND CLOCK OUTPUT ENABLE  
 OERECSD : REC SERIAL DATA OUTPUT ENABLE  
 PRCDOFF : PRECODE ON / OFF CONTROL FOR REC DATA  
 PRTY : PARITY FOR PROCESSOR ALL DATA  
 RECACD0 - RECACD3, RECBDD0 - RECBDD3 : REC AC, BD DATA FROM PROCESSOR  
 RECACSL, RECBDSL : REC HEAD OR AMPLIFIER SELECT  
 RENA - REND : REC A, B, C, D HEAD ENABLE  
 RST : RESET  
 SATAC, SATBD : 400K / 4MHZ SIGNAL FOR SAT  
 SATACEN, SATBDEN : SAT AC, BD SIGNAL ENABLE  
 STARTSEL : EXT SYNCHRONIZED MPX DATA  
 TEST : MODE SELECT FOR SERVO CONNECT CHECK

**OUTPUT**

ADVACD0 - ADVACD4, ADVBD0 - ADVBD4 : ADVANCE AC, BD DATA TO PROCESSOR  
 CK16, CK16 : 16MHZ CLOCK TO PROCESSOR  
 CKADVAC, CKADVBD : CLOCK FOR ADV AC, BD  
 CKCNFAC, CKCNFBD : CLOCK FOR CONF AC, BD  
 CNFACD0 - ACNFC4, CNFBDD0 - CNFBDD4 : PB AC, BD DATA FROM CONF HEAD  
 MPX : MPX DATA BEFORE PRECODE  
 ODIVCK : CLOCK TO MPX CK 2 OR 4 DIVIDED  
 OSTPULSE : TIMING PULSE SYNCHRONIZED MPX DATA  
 PECK : MPX CLOCK (32MHZ)  
 PEDATA : PRECODED MPX DATA  
 PRTYERR : PARITY CHECH RESULT FROM PROCESSOR  
 RECACSD, RECBDS0 : REC AC, BD PRECODE SERIAL DATA  
 SVCNTERR : CHECK RESULT OF SERVO BETWEEN IC

