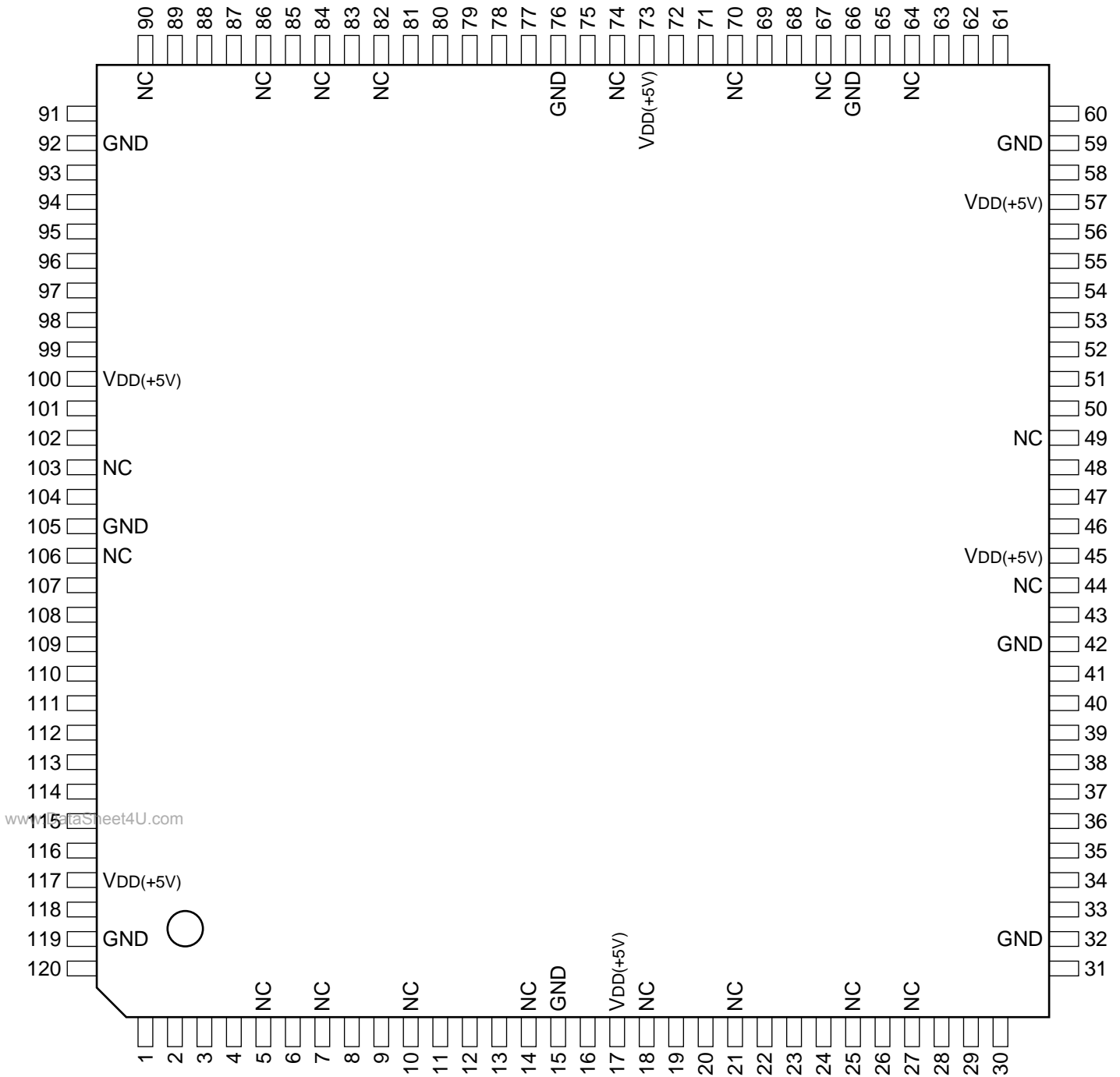

C-MOS DIGITAL VIDEO OUTPUT PROCESSOR

-TOP VIEW-



(VDD = +5V)

PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	I	U0	41	I/O	SDATA	81	I	SYNC EN
2	I	U1	42	—	GND	82	—	NC
3	I	U2	43	I	CLK	83	I	AUTO TRS
4	I	U3	44	—	NC	84	—	NC
5	—	NC	45	—	VDD	85	I	CKINV
6	I	U4	46	O	O0	86	—	NC
7	—	NC	47	O	O1	87	I	CLIP
8	I	U5	48	O	O2	88	I	LIMIT
9	I	U6	49	—	NC	89	I	V BLK FIX
10	—	NC	50	O	O3	90	—	NC
11	I	U7	51	O	O4	91	I	DBLK / ABLK
12	I	U8	52	O	O5	92	—	GND
13	I	U9	53	O	O6	93	I	BLK MODE0
14	—	NC	54	O	O7	94	I	BLK MODE1
15	—	GND	55	O	O8	95	I	BLK MODE2
16	I	DIAG SMPL	56	O	O9	96	I	MUX MODE0
17	—	VDD	57	—	VDD	97	I	MUX MODE1
18	—	NC	58	O	CKO	98	I	525 / 625
19	I	V0	59	—	GND	99	I	D1 / D2
20	I	V1	60	O	DATA PHS0	100	—	VDD
21	—	NC	61	O	DATA PHS1	101	I	BLK GATE
22	I	V2	62	O	TRS JST	102	I	TRS SEL0
23	I	V3	63	O	SEL STAT1	103	—	NC
24	I	V4	64	—	NC	104	I	TRS SEL1
25	—	NC	65	O	SEL STAT0	105	—	GND
26	I	V5	66	—	GND	106	—	NC
27	—	NC	67	—	NC	107	I	Y0
28	I	V6	68	I	TEST MODE0	108	I	Y1
29	I	V7	69	I	TEST MODE1	109	I	Y2
30	I	V8	70	—	NC	110	I	Y3
31	I	V9	71	I	TEST MODE2	111	I	Y4
32	—	GND	72	I	TNCON	112	I	Y5
33	I	HD	73	—	VDD	113	I	Y6
34	I	FD	74	—	NC	114	I	Y7
35	I	CFP	75	O	TOUT	115	I	Y8
36	I	PARA / SERI	76	—	GND	116	I	Y9
37	I	CKX	77	I	RDCLR	117	—	VDD
38	I	CS	78	I	DR ON	118	I	EWRST
39	I	SADRS	79	I	TRS EN	119	—	GND
40	I	CKD	80	I	BURST EN	120	I	ERRST

INPUT

525 / 625 ; 525 / 625 SELECT
 AUTO TRS ; AUTO TRS ADD MODE
 BLK GATE ; BLANKING SIGNAL
 BLK MODE 0 - 2 ; BLANKING MODE
 BURST EN ; BURST ADD ENABLE
 CKD ; SERIAL INTERFACE SERIAL DATA
 CKINV ; CLOCK INVERT ENABLE
 CKX ; CONTROL REGISTER OPERATION TIMING
 CLIP ; WHITE CLIP AND DARK CLIP ENABLE
 CLK ; SYSTEM CLOCK
 CFP ; SYSTEM CFP (D2 MODEL)
 CS ; CHIP SELECTOR
 D1 / D2 ; CONTROL REGISTER PARALLEL DATA
 DBLK ABLK ; DIGITAL / ANALOG BLANKING SELECT
 DIAG SMPL ; SELF DIAGNOSIS SAMPLE PULSE
 DR ON ; ROUNDING ENABLE
 ERRST ; INPUT READ RESET PULSE
 EWRST ; INPUT WRITE RESET PULSE
 FD ; SYSTEM FD (D1 MODEL)
 HD ; SYSTEM HD
 LIMIT ; LIMITER ENABLE
 MUX MODE 0, 1 ; MULTIPLEX MODE
 PARA / SERI ; PARALLEL / SERIAL SELECT
 RDCLR ; CLEAR PULSE
 SADRS ; CONTROL REGISTER SIGNAL ADDRESS
 SYNC EN ; SYNC ADD ENABLE
 TEST MODE 0 - 2 ; TEST POINT
 TNCON ; TEST POINT
 TRS EN ; TRS ADD ENABLE
 TRS SEL 0, 1 ; MANUAL MODE TRS MIX
 V BLX FIX ; VERTICAL BLANKING LENGTH FIX
 U0 - U9, Y0 - Y9, V0 - V9 ; VIDEO SIGNAL

OUTPUT

CKO ; CLOCK
 DATA PHS 0, 1 ; OUTPUT VIDEO DATA PHASE
 O0 - O9 ; VIDEO SIGNAL
 SET STAT 0, 1 ; SYNC, TRS ADD TIMING
 TOUT ; TEST POINT
 TRS JST ; TRS PHASE CHECK PULSE

INPUT/OUTPUT

SDATA ; CONTROL REGISTER SERIAL DATA

116	Y9	O9	56
115	Y8	O8	55
114	Y7	O7	54
113	Y6	O6	53
112	Y5	O5	52
111	Y4	O4	51
110	Y3	O3	50
109	Y2	O2	48
108	Y1	O1	47
107	Y0	O0	46
13	U9	CKO	58
12	U8		
11	U7	DATA PHS1	61
9	U6	DATA PHS0	60
8	U5	TRS JST	62
6	U4	SEL STAT1	63
4	U3	SEL STAT0	65
3	U2	TOUT	75
2	U1		
1	U0		
		BLK MODE2	95
31	V9	BLK MODE1	94
30	V8	BLK MODE0	93
29	V7	MUX MODE1	97
28	V6	MUX MODE0	96
26	V5	525 / 625	98
24	V4	D1 / D2	99
23	V3	TRS SEL1	104
22	V2	TRS SEL0	102
20	V1		
19	V0	RDCLR	77
		DR ON	78
43	>	TRS EN	79
33	HD	BURST EN	80
34	FD	SYNC EN	81
35	CFP	AUTO TRS	83
101	BLK GATE	CKINV	85
		CLIP	87
39	SADRS	LIMIT	88
41	SDATA	V BLK FIX	89
40	CKD	DBLK / ABLK	91
38	CS		
37	CKX	TNCON	72
36	PARA / SERI	TEST MODE2	71
16	DIAG SMPL	TEST MODE1	69
		TEST MODE0	68
118	EWRST		
120	ERRST		

