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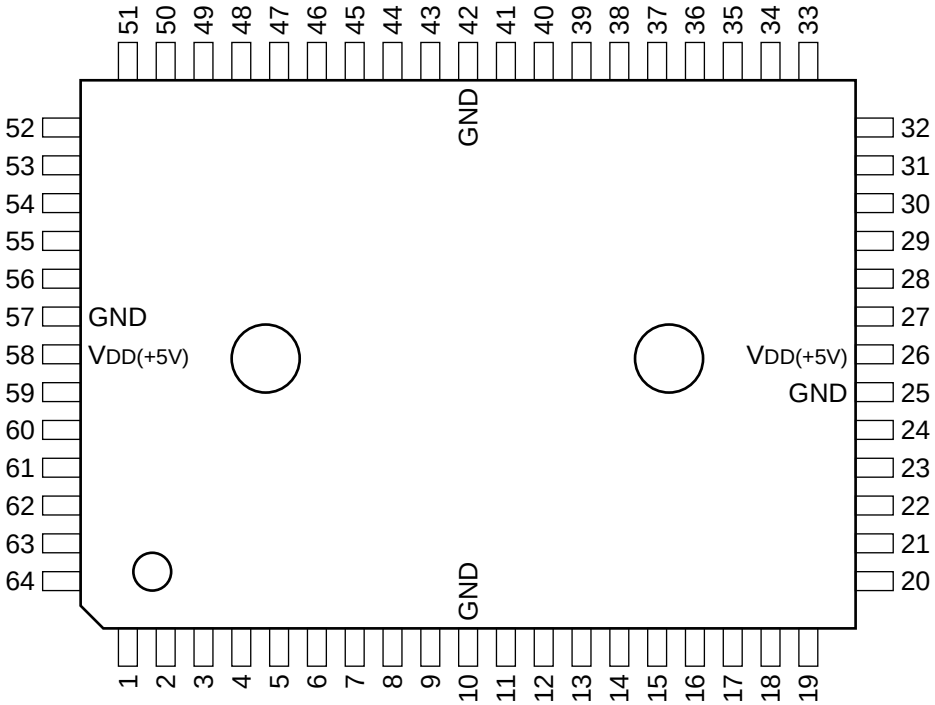
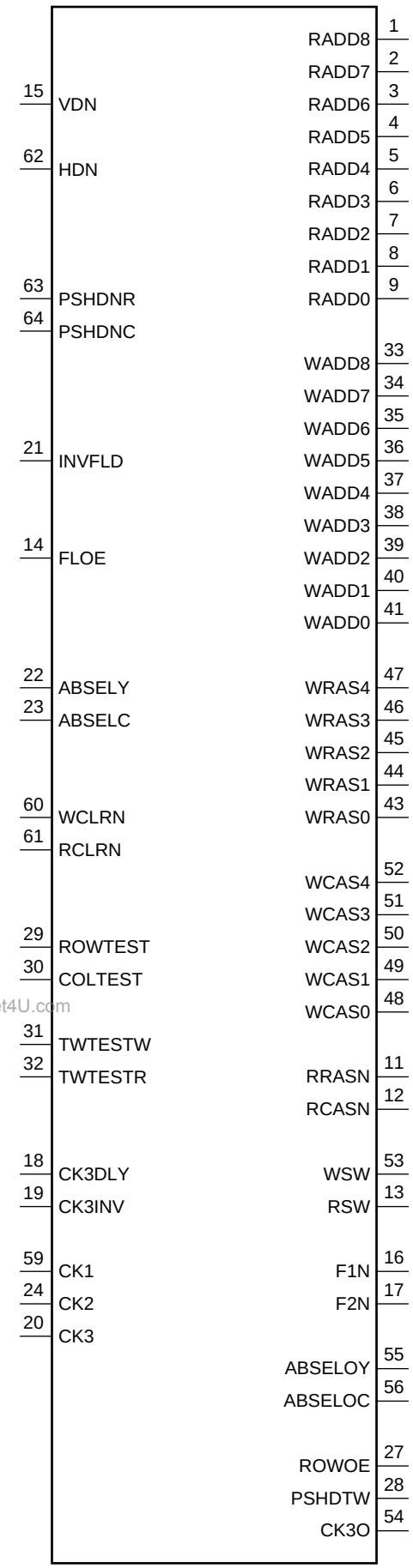
C-MOS DRAM ADDRESS GENERATOR

-TOP VIEW-



(V_{DD} = +5V)

PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	O	RADD8	17	O	F2N	33	O	WADD8	49	O	WCAS1
2	O	RADD7	18	I	CK3DLY	34	O	WADD7	50	O	WCAS2
3	O	RADD6	19	I	CK3INV	35	O	WADD6	51	O	WCAS3
4	O	RADD5	20	I	CK3	36	O	WADD5	52	O	WCAS4
5	O	RADD4	21	I	INVFLD	37	O	WADD4	53	O	WSW
6	O	RADD3	22	I	ABSELY	38	O	WADD3	54	O	CK3O
7	O	RADD2	23	I	ABSELC	39	O	WADD2	55	O	ABSELOY
8	O	RADD1	24	I	CK2	40	O	WADD1	56	O	ABSELOC
9	O	RADD0	25	—	GND	41	O	WADD0	57	—	GND
10	—	GND	26	—	V_{DD}	42	—	GND	58	—	V_{DD}
11	O	RRASN	27	O	ROWOE	43	O	WRAS0	59	I	CK1
12	O	RCASN	28	O	PSHDTW	44	O	WRAS1	60	I	WCLRN
13	O	RSW	29	I	ROWTEST	45	O	WRAS2	61	I	RCLRN
14	I	FLOE	30	I	COLTEST	46	O	WRAS3	62	I	HDN
15	I	VDN	31	I	TWTESTW	47	O	WRAS4	63	I	PSHDNR
16	O	F1N	32	I	TWTESTR	48	O	WCAS0	64	I	PSHDNC



INPUT

ABSELC	;	ABSEL FOR C-IN
ABSELY	;	ABSEL FOR Y-IN
CK1	;	27.0 MHz / 28.6 MHz
CK2	;	13.5 MHz / 14.3 MHz
CK3	;	CK3 IN
CK3DLY	;	CK3 DELAY
CK3INV	;	CK3 INVERT
COLTEST	;	COLUMN ADD TEST
FLOE	;	FIELD ODD / EVEN
HDN	;	H-SCAN SYNC
INVFLD	;	ABSEL INVERT
PSHDNC	;	V-SCAN SYNC
PSHDNR	;	V-SCAN SYNC
RCLRN	;	READ ADD CLEAR
ROWTEST	;	ROW ADD TEST
TWTESTR	;	READ ADD TEST
TWTESTW	;	WRITE ADD TEST
VDN	;	FIELD CLEAR
WCLRN	;	WRITE ADD CLEAR

OUTPUT

ABSELOC	;	ABSEL FOR C-OUT
ABSELOY	;	ABSEL FOR Y-OUT
CK3O	;	CK3 OUT
F1N	;	FIELD1-LOW
F2N	;	FIELD2-LOW
PSHDTW	;	PSHDN ODD / EVEN
RADD0 - RADD8	;	READ ADDRESS
RCASW	;	READ ADDRESS-CAS
ROWOE	;	ROW-ADD ODD / EVEN
RRASN	;	READ ADDRESS-RAS
RSW	;	READ ADD SWITCHING
WADD0 - WADD8	;	WRITE ADDRESS
WCAS0 - WCAS4	;	WRITE ADDRESS-CAS
WRAS0 - WRAS4	;	WRITE ADDRESS-RAS
WSW	;	WRITE ADD SWITCHNG