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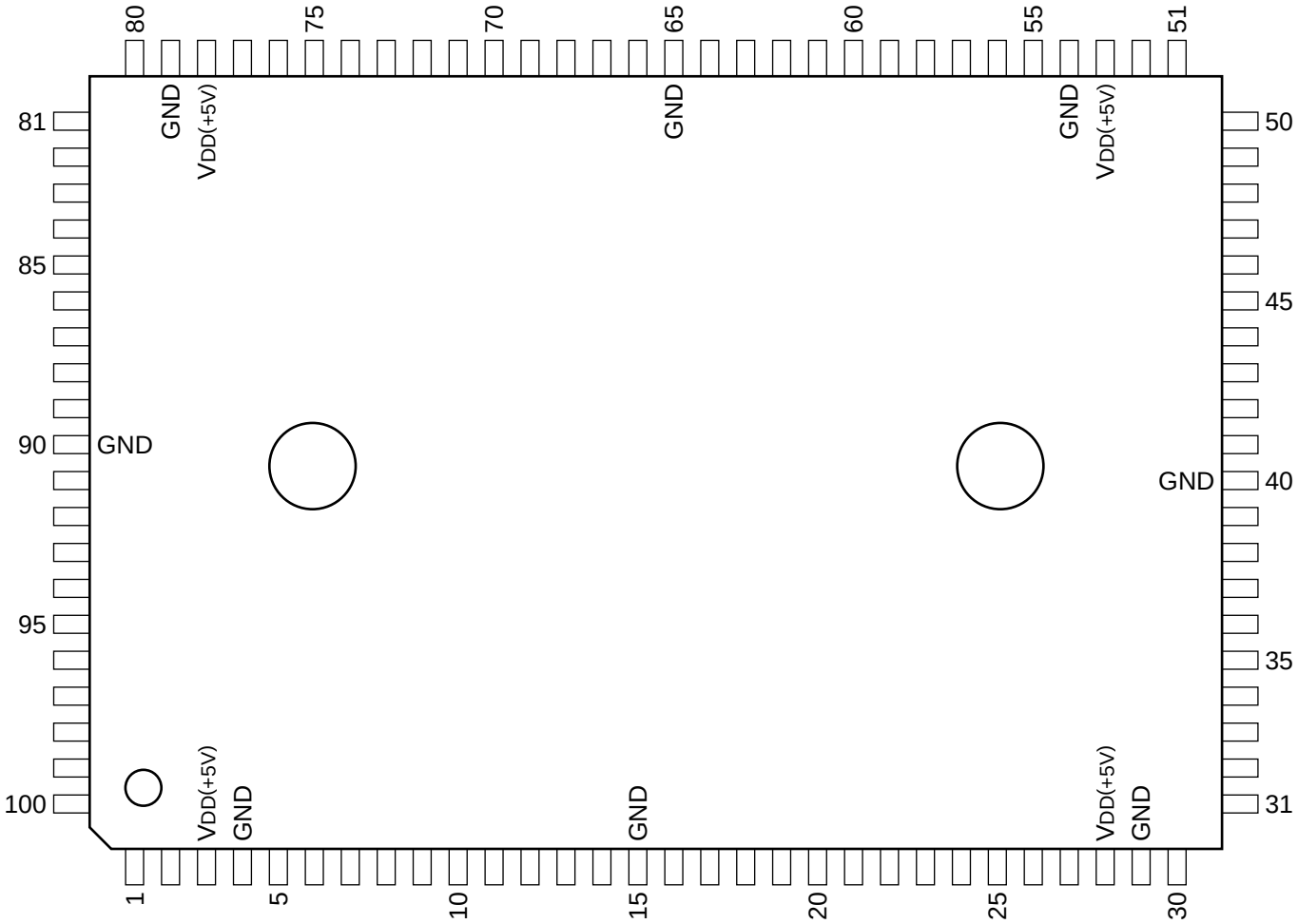
IL00

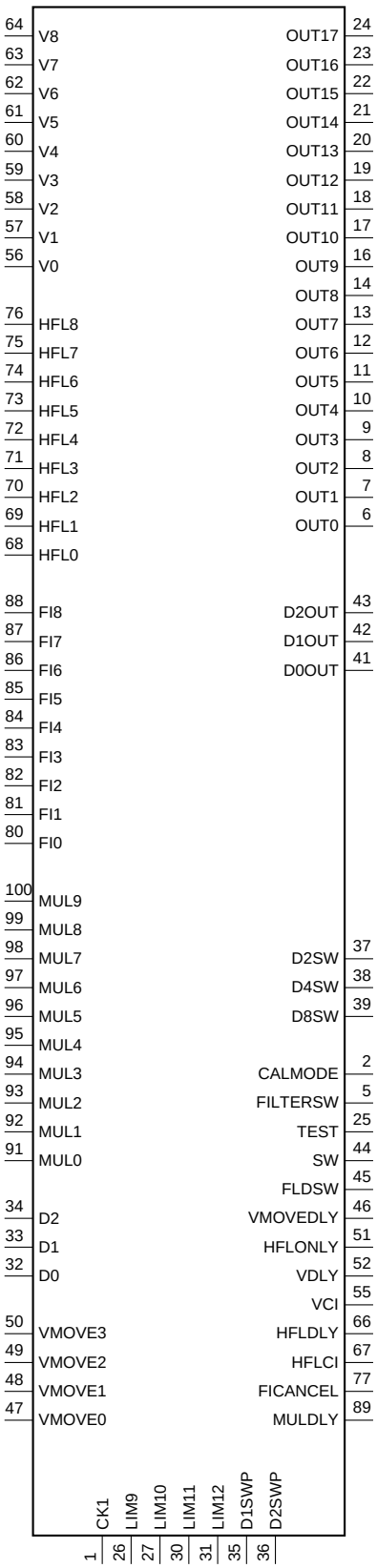
C-MOS SRAM READ ADDRESS ENCODER

-TOP VIEW-



(V_{DD} = +5V)

PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	I	CK1	35	I	D1SWP	69	I	HFL1
2	I	CALMODE	36	I	D2SWP	70	I	HFL2
3	—	V_{DD}	37	I	D2SW	71	I	HFL3
4	—	GND	38	I	D4SW	72	I	HFL4
5	O	FILTERSW	39	I	D8SW	73	I	HFL5
6	O	OUT0	40	—	GND	74	I	HFL6
7	O	OUT1	41	O	D0OUT	75	I	HFL7
8	O	OUT2	42	O	D1OUT	76	I	HFL8
9	O	OUT3	43	O	D2OUT	77	I	FICANCEL
10	O	OUT4	44	I	SW	78	—	V_{DD}
11	O	OUT5	45	I	FLDSW	79	—	GND
12	O	OUT6	46	I	VMOVEDLY	80	I	FI0
13	O	OUT7	47	I	VMOVE0	81	I	FI1
14	O	OUT8	48	I	VMOVE1	82	I	FI2
15	O	GND	49	I	VMOVE2	83	I	FI3
16	O	OUT9	50	I	VMOVE3	84	I	FI4
17	O	OUT10	51	I	HFLONLY	85	I	FI5
18	O	OUT11	52	I	VDLY	86	I	FI6
19	O	OUT12	53	—	V_{DD}	87	I	FI7
20	O	OUT13	54	—	GND	88	I	FI8
21	O	OUT14	55	I	VCI	89	I	MULDLY
22	O	OUT15	56	I	V0	90	—	GND
23	O	OUT16	57	I	V1	91	I	MUL0
24	O	OUT17	58	I	V2	92	I	MUL1
25	I	TEST	59	I	V3	93	I	MUL2
26	I	LIM9	60	I	V4	94	I	MUL3
27	I	LIM10	61	I	V5	95	I	MUL4
28	—	V_{DD}	62	I	V6	96	I	MUL5
29	—	GND	63	I	V7	97	I	MUL6
30	I	LIM11	64	I	V8	98	I	MUL7
31	I	LIM12	65	—	GND	99	I	MUL8
32	I	D0	66	I	HFLDLY	100	I	MUL9
33	I	D1	67	I	HFLCI			
34	I	D2	68	I	HFL0			



INPUT

CALMODE	;	CALCULATOR MODE
CK1	;	SYSTEM CLOCK
D0-D2	;	DELAY LINE-IN
D2SW	;	DELAY PARAMETER
D4SW	;	DELAY PARAMETER
D8SW	;	DELAY PARAMETER
D1SWP	;	DELEY PARAMETER
D2SWP	;	DELEY PARAMETER
FI0-FI8	;	FIELD SUBTRACT
FICANCEL	;	FI-INPUT CANCEL
FILTERSW	;	FILTER SWITCH
FLDSW	;	ALL-H SWITCH
HFL0-HFL8	;	FRAME SUB/H-ADD
HFLCI	;	HFL CARRY-IN
HFLDLY	;	HFL DELAY
HFLONLY	;	HFL ONLY
LIM9-LIM12	;	LIMITER SWITCH
MUL0-MUL9	;	MULTIPLE RATE
MULDLY	;	MUL DELAY
SW	;	ALL-H SWITCH
TEST	;	TEST
V0-V8	;	V-ADDRESS
VCI	;	V-ADDRESS CARRY-IN
VDLY	;	V DELAY
VMOVE0-VMOVE3	;	V-SUBTRACT
VMOVEDLY	;	VMOVE-IN DELAY

OUTPUT

D0OUT-D2OUT	;	DELAY LINE-OUT
OUT0-OUT17	;	OUTPUT