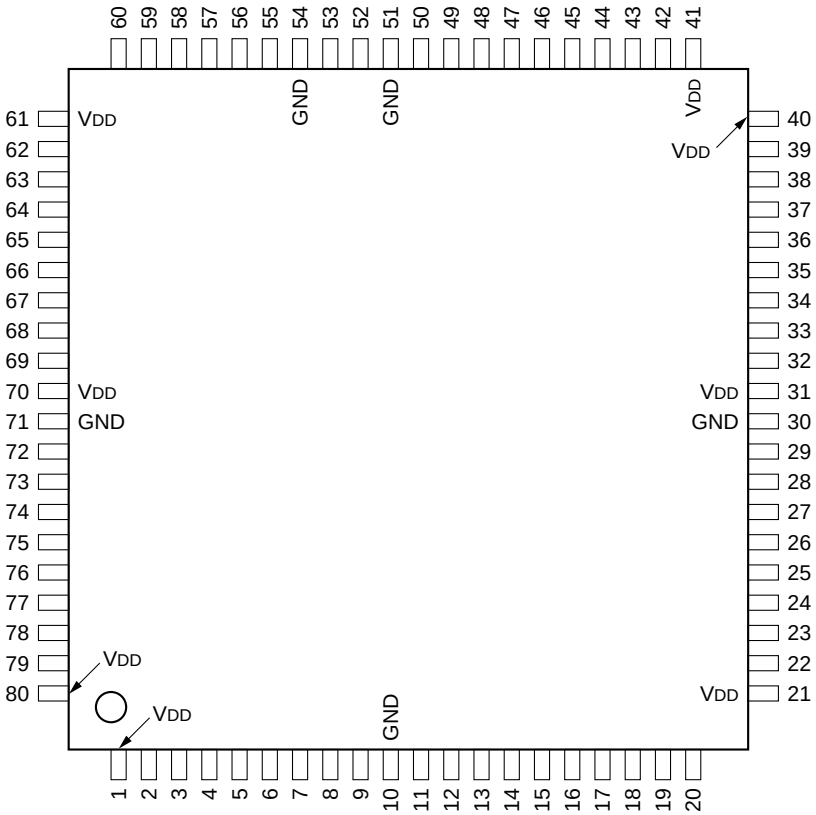
HC-MOS SYNC GENERATOR

—TOP VIEW—



PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	—	VDD	21	—	VDD	41	—	VDD	61	—	VDD
2	I	HR	22	O	ACK	42	I	PRST	62	O	HCOM1
3	I	HRSEL	23	I/O	SDA	43	I	TEST4	63	O	HCOM2
4	O	HD	24	I	SCL	44	O	COM1EX	64	I	HPHS0
5	O	SYNC	25	I	ASET	45	O	COM2	65	I	HPHS1
6	O	BF	26	I	HBLK0	46	I	MODE1	66	I	HPHS2
7	O	BLKG	27	I	HBLK1	47	I	MODE2	67	I	HPHS3
8	O	FH2	28	I	HBLK2	48	I	TEST5	68	I	INTH
9	O	LALT	29	I	HBLK3	49	O	CK27O	69	O	DLHD
10	—	GND	30	—	GND	50	I	CK27I	70	—	VDD
11	O	VD	31	—	VDD	51	—	GND	71	—	GND
12	O	FLD1	32	I	VBLK0	52	O	TGC	72	I	TDI
13	O	DPBLKG	33	I	VBLK1	53	O	SCCOM	73	O	TDO
14	O	NBLKG	34	I	CK36I	54	—	GND	74	I	TCK
15	O	SYNC2	35	O	CK36O	55	I	INTSC	75	O	$\overline{N}$/P
16	O	SAMPLE	36	I	TEST3	56	I	TEST6	76	O	TESTO
17	O	FLD	37	I	CLKSL1	57	I	EXTSC	77	I	LALTR
18	I	TEST1	38	I	CLKLS2	58	O	INTEXT	78	I	VLRSEL
19	I	TEST2	39	O	CK18O	59	I	EXSYNC	79	I	VR
20	I	DTCNT	40	—	VDD	60	I	TEST7	80	—	VDD

INPUT

ASET	:	IIC ASET
CK27I	:	27 MHz CLOCK
CK36I	:	36 MHz CLOCK
CLKSL1, CLKLS2	:	CLOCK FREQUENCY SELECT
DTCNT	:	DATA CONTROL
EXSYNC	:	EXTERNAL SYNC
EXTSC	:	EXTERNAL SUBCARRIER
HBLK0 - HBLK3	:	H BLANKING WIDTH PULSE
HPHS0 - HPHS3	:	H PHASE DATA
HR	:	H RESET
HRSEL	:	H RESET SELECT
INTH	:	PHASE CONTROLLED INTERNAL HD
INTSC	:	INTERNAL SUBCARRIER
LALTR	:	LINE ALTERNATE RESET
MODE1, MODE2	:	MODE SELECT
PRST	:	POWER ON RESET
SCL	:	IIC CLOCK
TCK	:	TEST CLOCK
TDI	:	TEST DATA
VBLK0, VBLK1	:	V BLANKING WIDTH PULSE
VLRSEL	:	V RESET/LALT RESET SELECT
VR	:	V RESET
TEST1 - TEST7	:	TEST MODE

OUTPUT

ACK	:	IIC ACK
BF	:	BURST FLAG
BLKG	:	BLANKING
CK18O	:	18 MHz CLOCK
CK27O	:	27 MHz CLOCK
CK36O	:	36 MHz CLOCK
COM1EX	:	PHASE COMPARATED CLOCK
COM2	:	PHASE COMPARATED CLOCK
DLHD	:	PHASE COMPARATED INTERNAL HD
DPBLKG	:	D1/PRE BLANKING
FH2	:	2fH
FLD	:	FIELD
FLD1	:	FIELD1
HCOM1, HCOM2	:	FH/HR PHASE COMPARATED SIGNAL
HD	:	HORIZONTAL DRIVE
INTEXT	:	INT/EXT SYNCHRONIZE MODE SELECT
LALT	:	LINE ALTERNATE
$\overline{N}$/P	:	NTSC/PAL DISCRIMINATION SIGNAL
NBLKG	:	NARROW BLANKING
SAMPLE	:	SAMPLE
SCCOM	:	INT SC/EXT SC PHASE COMPARATED SIGNAL
SYNC	:	SYNC
SYNC2	:	SYNC2
TDO	:	TEST DATA
TESTO	:	TEST MODE
TGC	:	BURST GATE PULSE
VD	:	VERTICAL DRIVE

INPUT/OUTPUT

SDA	:	IIC DATA