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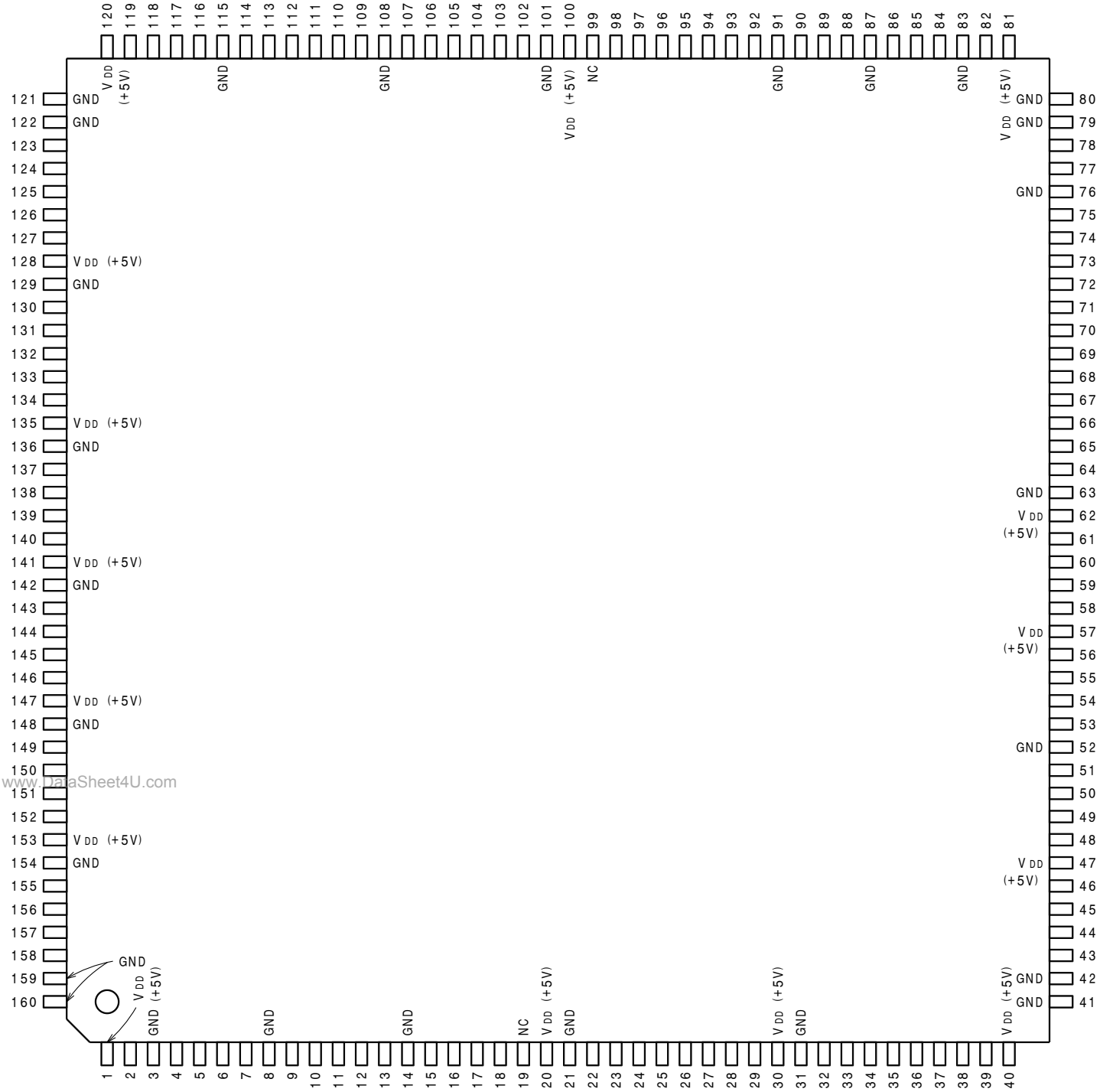
C-MOS SOUND MEMORY CONTROLLER FOR R-DAT

-TOP VIEW-



(V_{DD} = +5V)

PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	–	V_{DD}	41	–	GND	81	–	V_{DD}	121	–	GND
2	I	CPUCK	42	–	GND	82	I	F256	122	–	GND
3	–	GND	43	I/O	DB15	83	–	GND	123	O	RA9
4	I	$\overline{\text{RESET}}$	44	I/O	DB14	84	I	SBSY	124	O	RA8
5	O	READY	45	I/O	DB13	85	O	FS	125	O	RA7
6	I	$\overline{\text{I/ORD}}$	46	I/O	DB12	86	O	FS64	126	O	RA6
7	I	$\overline{\text{I/OWR}}$	47	–	V_{DD}	87	–	GND	127	O	RA5
8	–	GND	48	I/O	DB11	88	I	SDI	128	–	V_{DD}
9	I	$\overline{\text{MRD}}$	49	I/O	DB10	89	O	SDO1	129	–	GND
10	I	MWR/	50	I/O	DB9	90	O	SDO2	130	O	RA4
11	I	$\overline{\text{I/OEN}}$	51	I/O	DB8	91	–	GND	131	O	RA3
12	I	$\overline{\text{MEMEN}}$	52	–	GND	92	I	$\overline{\text{EMU SEL}}$	132	O	RA2
13	I	$\overline{\text{DSIEN}}$	53	I/O	DB7	93	I	EXTSDI	133	O	RA1
14	–	GND	54	I/O	DB6	94	O	EXTXRDY	134	O	RA0
15	O	WRREQ	55	I/O	DB5	95	O	EXTSDO	135	–	V_{DD}
16	I	$\overline{\text{WRACK}}$	56	I/O	DB4	96	O	EXTXSLD	136	–	GND
17	O	$\overline{\text{END}}$	57	–	V_{DD}	97	O	EXTSCK	137	I/O	RDQ15
18	I	ENDRTN	58	I/O	DB3	98	I	NA2	138	I/O	RDQ14
19	–	NC	59	I/O	DB2	99	–	NC	139	I/O	RDQ13
20	–	V_{DD}	60	I/O	DB1	100	–	V_{DD}	140	I/O	RDQ12
21	–	GND	61	I/O	DB0	101	–	GND	141	–	V_{DD}
22	I	AB15	62	–	V_{DD}	102	I	NA1	142	–	GND
23	I	AB14	63	–	GND	103	I	NA0	143	I/O	RDQ11
24	I	AB13	64	O	WRFRM	104	O	$\overline{\text{DSP SEL2}}$	144	I/O	RDQ10
25	I	AB12	65	I	EXCK	105	O	$\overline{\text{DSP SEL1}}$	145	I/O	RDQ9
26	I	AB11	66	O	SDSO	106	O	$\overline{\text{DSP SEL0}}$	146	I/O	RDQ8
27	I	AB10	67	I	ERRF	107	I	PGMSDI	147	–	V_{DD}
28	I	AB9	68	O	RDFRM	108	–	GND	148	–	GND
29	I	AB8	69	I	TEST3	109	O	PGMSCK	149	I/O	RDQ7
30	–	V_{DD}	70	I	TEST2	110	O	PGMXSLD	150	I/O	RDQ6
31	–	GND	71	I	TEST1	111	O	PGMSDO	151	I/O	RDQ5
32	I	AB7	72	O	$\overline{\text{RDSTS}}$	112	I	$\overline{\text{XRDY2}}$	152	I/O	RDQ4
33	I	AB6	73	O	$\overline{\text{WRSTS}}$	113	I	$\overline{\text{XRDY1}}$	153	–	V_{DD}
34	I	AB5	74	O	TRGB1	114	I	$\overline{\text{XRDY0}}$	154	–	GND
35	I	AB4	75	O	TRGA1	115	–	GND	155	I/O	RDQ3
36	I	AB3	76	–	GND	116	O	$\overline{\text{RAS}}$	156	I/O	RDQ2
37	I	AB2	77	I	LRCKI	117	O	$\overline{\text{CAS}}$	157	I/O	RDQ1
38	I	AB1	78	I	DATFRM	118	O	$\overline{\text{WE}}$	158	I/O	RDQ0
39	I	AB0	79	–	GND	119	O	$\overline{\text{OE}}$	159	–	GND
40	–	V_{DD}	80	–	GND	120	–	V_{DD}	160	–	GND

INPUT

AB0-AB15	;CPU ADDRESS BUS From SYSTEM
CPUCK	;CPU CLOCK
DATFRM	;DAT FRAME INPUT SIGNAL
DSIEN	;DSP ENABLE SIGNAL
$\overline{\text{EMU SEL}}$	;EMULATOR SELECTION PIN
ENDRTN	;END RETURN SIGNAL
ERRF	;TEST SIGNAL (NOT USE)
EXCK	;TEST SIGNAL (NOT USE)
EXTSDI	;EXTERNAL SERIAL DATA INPUT
F256	;256fs
I/O EN/	;I/O (AREA) ENABLE SIGNAL
I/O RD/	;I/O (AREA) READ SIGNAL
I/O WR/	;I/O (AREA) WRITE SIGNAL
LRCKI	;LR CLOCK INPUT SIGNAL
MEMEN/	;MEMORY (AREA) ENABLE SIGNAL
MRD/	;MEMORY (AREA) READ SIGNAL
MWR/	;MEMORY (AREA) WRITE SIGNAL
NA0, 1, 2	;DSP ADDRESS
PGMSDI	;SERIAL DATA INPUT
READY	;READY SIGNAL
RESET/	;RESET SIGNAL
SBSY	;TEST SIGNAL (NOT USE)
SDI	;SERIAL DATA INPUT
WRACK	;WRITE ACKNOWLEDGE SIGNAL
$\overline{\text{XRDY 0}}$, $\overline{1}$, $\overline{2}$	;TRANSMISSION READY (SCK INPUT PROHIBITED)

OUTPUT

$\overline{\text{CAS}}$	;DRAM COLUMN ADDRESS STROBE OUTPUT SIGNAL
$\overline{\text{DSP SEL0}}$, $\overline{1}$, $\overline{2}$	;DSP CHIP SELECT PIN
END	;END SIGNAL
EXTSCK	;EXTERNAL SERIAL TRANSMISSION CLOCK
EXTSDO	;EXTERNAL SERIAL DATA INPUT
EXTXRDY	;EXTERNAL TRANSMISSION READY (SCK INPUT PROHIBITED)
EXTXSLD	;EXTERNAL SERIAL DATA INPUT LATCH
FS	;FS OUTPUT FOR DSP
FS64	;BIT SHIFT CLOCK OUTPUT FOR DSP
$\overline{\text{OE}}$	;DRAM OUTPUT ENABLE SIGNAL OUTPUT
PGMSCK	;SERIAL TRANSMISSION CLOCK
PGMSDO	;SERIAL DATA OUTPUT
PGMXSLD	;SERIAL DATA INPUT LATCH
RA0-RA9	;ADDRESS BUS to DRAM
$\overline{\text{RAS}}$	;DRAM LOW ADDRESS STROBE OUTPUT SIGNAL 2
RDFRM	;SIGNAL OUTPUT FOR MEMORY READ INTERRUPTION
$\overline{\text{RDSTS}}$	;LED OUTPUT FOR DRAM WRITE MONITOR
SDO1, 2	;SERIAL DATA OUTPUT 1, 2
SDSO	;TEST SIGNAL (NOT USE)
TRGA1	;TRGA OUTPUT SIGNAL
TRGB1	;TRGB OUTPUT SIGNAL
$\overline{\text{WE}}$	;DRAM WRITE ENABLE SIGNAL
WRFRM	;SIGNAL OUTPUT FOR MEMORY WRITE INTERRUPTION
WRREQ	;WRITE REQUEST SIGNAL
$\overline{\text{WRSTS}}$	;LED OUTPUT FOR DRAM READ MONITOR

INPUT/OUTPUT

DB0-DB15	;CPU DATA BUS From SYSTEM
RDQ0-RDQ15	;DATA BUS to DRAM