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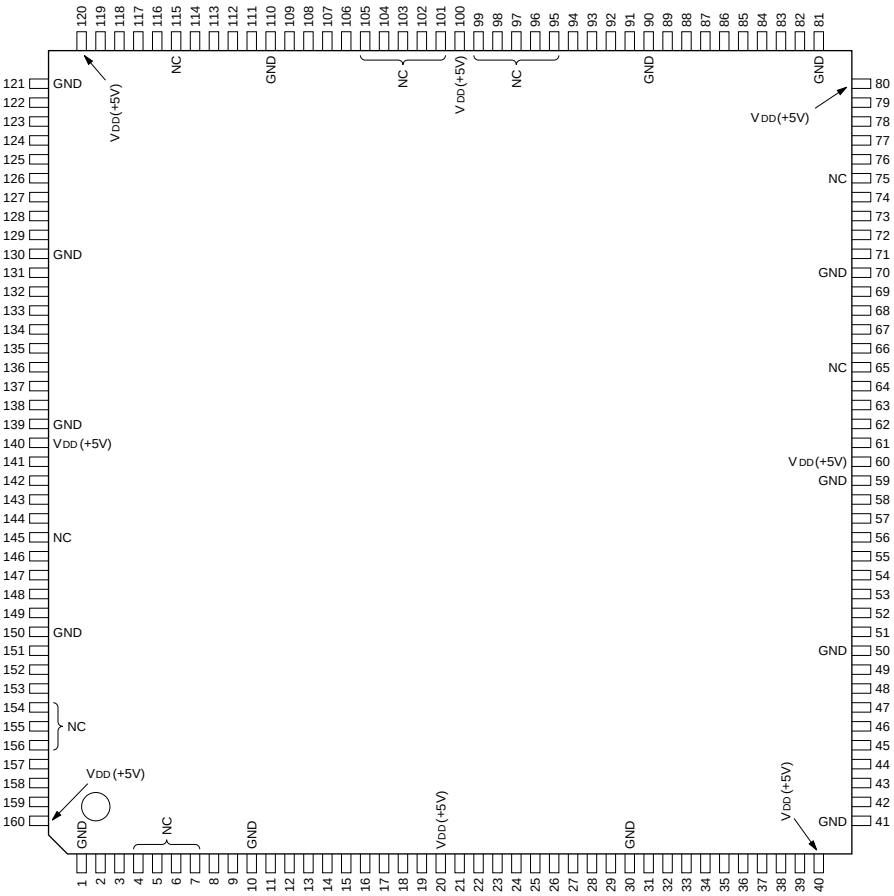
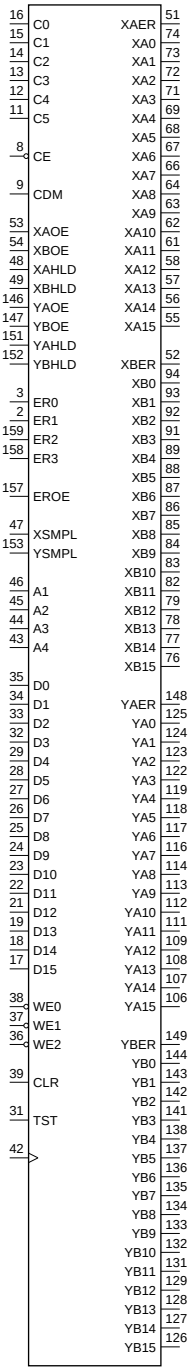
C-MOS ADDRESS ARITHMETIC PROCESSOR FOR 2D EFECT
- TOP VIEW -



(V_{DD} =+5V)

PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	–	GND	41	–	GND	81	–	GND	121	–	GND
2	O	ER1	42	I	CK	82	O	XB11	122	O	YA3
3	O	ER0	43	I	A4	83	O	XB10	123	O	YA2
4	–	NC	44	I	A3	84	O	XB9	124	O	YA1
5	–	NC	45	I	A2	85	O	XB8	125	O	YA0
6	–	NC	46	I	A1	86	O	XB7	126	O	YB15
7	–	NC	47	O	XSMPL	87	O	XB6	127	O	YB14
8	I	CE	48	I	XAHLD	88	O	XB5	128	O	YB13
9	I	CDM	49	I	XBHLD	89	O	XB4	129	O	YB12
10	–	GND	50	–	GND	90	–	GND	130	–	GND
11	I	C5	51	O	XAER	91	O	XB3	131	O	YB11
12	I	C4	52	O	XBER	92	O	XB2	132	O	YB10
13	I	C3	53	I	XAOE	93	O	XB1	133	O	YB9
14	I	C2	54	I	XBOE	94	O	XB0	134	O	YB8
15	I	C1	55	O	XA15	95	–	NC	135	O	YB7
16	I	C0	56	O	XA14	96	–	NC	136	O	YB6
17	I	D15	57	O	XA13	97	–	NC	137	O	YB5
18	I	D14	58	O	XA12	98	–	NC	138	O	YB4
19	I	D13	59	–	GND	99	–	NC	139	–	GND
20	–	V_{DD}	60	–	V_{DD}	100	–	V_{DD}	140	–	V_{DD}
21	I	D12	61	O	XA11	101	–	NC	141	O	YB3
22	I	D11	62	O	XA10	102	–	NC	142	O	YB2
23	I	D10	63	O	XA9	103	–	NC	143	O	YB1
24	I	D9	64	O	XA8	104	–	NC	144	O	YB0
25	I	D8	65	–	NC	105	–	NC	145	–	NC
26	I	D7	66	O	XA7	106	O	YA15	146	I	YAOE
27	I	D6	67	O	XA6	107	O	YA14	147	I	YBOE
28	I	D5	68	O	XA5	108	O	YA13	148	O	YAER
29	I	D4	69	O	XA4	109	O	YA12	149	O	YBER
30	–	GND	70	–	GND	110	–	GND	150	–	GND
31	I	TST	71	O	XA3	111	O	YA11	151	I	YAHLD
32	I	D3	72	O	XA2	112	O	YA10	152	I	YBHLD
33	I	D2	73	O	XA1	113	O	YA9	153	O	YSMPL
34	I	D1	74	O	XA0	114	O	YA8	154	–	NC
35	I	D0	75	–	NC	115	–	NC	155	–	NC
36	I	WE2	76	O	XB15	116	O	YA7	156	–	NC
37	I	WE1	77	O	XB14	117	O	YA6	157	I	EROE
38	I	WE0	78	O	XB13	118	O	YA5	158	O	ER3
39	I	CLR	79	O	XB12	119	O	YA4	159	O	ER2
40	–	V_{DD}	80	–	V_{DD}	120	–	V_{DD}	160	–	V_{DD}

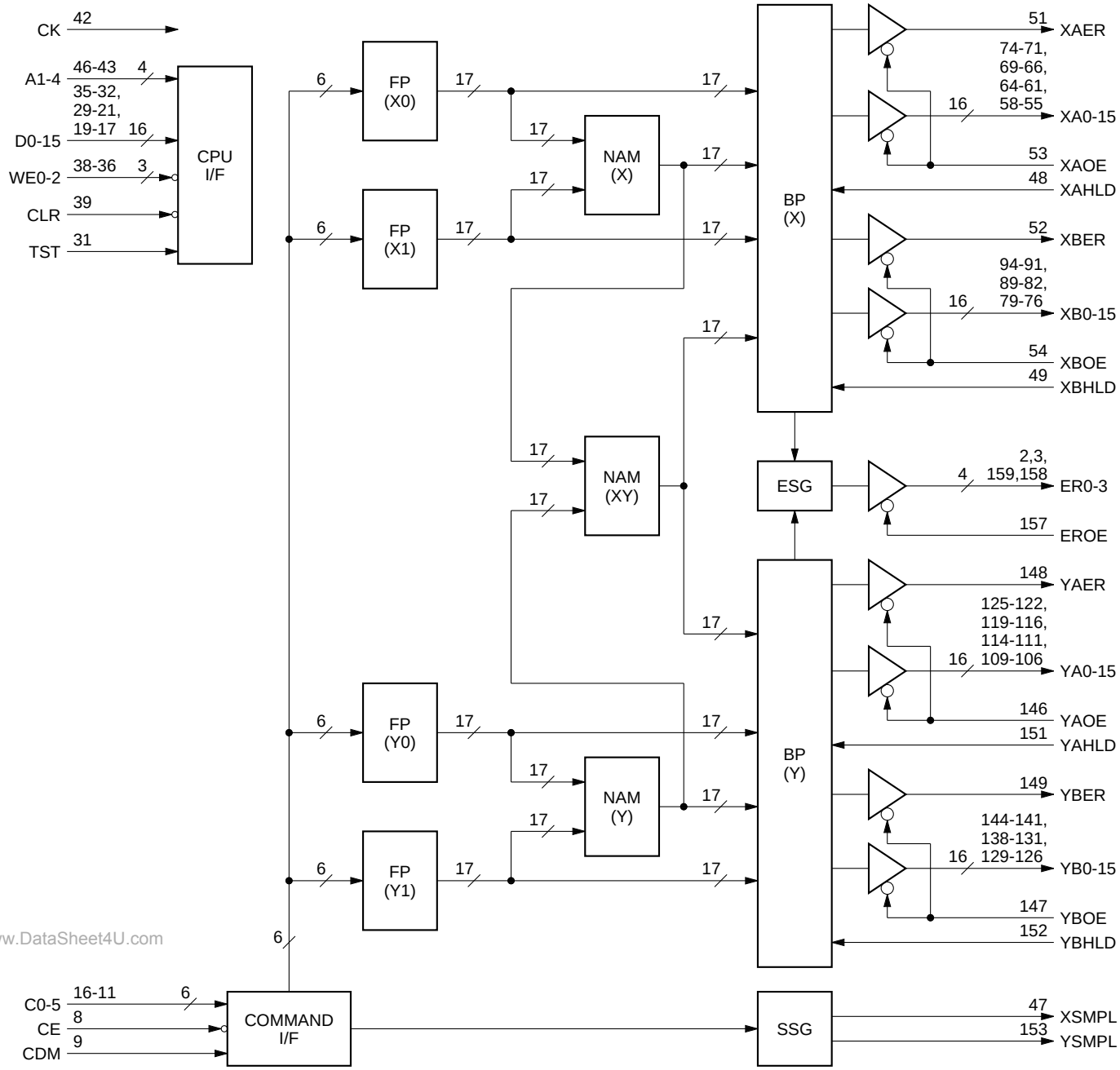


INPUT

A1-A4	; ADDRESS
C0-C5	; FP (FRONT PROCESSOR) CONTROL COMMAND
CE	; FP (FRONT PROCESSOR) CONTROL COMMAND ENABLE
CK	; CLOCK
CLR	; CLEAR
CMD	; COMMAND GENERATION MODE SELECT (L : INTERFACE MODE, H : DIRECT MODE)
D0-D15	; DATA
TST	; IC TEST
WE0-WE2	; WRITE ENABLE

OUTPUT

XA0-XA15	; XA PORT DATA
XAER	; XA PORT STATUS
XAHLD	; XA PORT OUTPUT HOLD (H : HOLD)
XAOE	; XA PORT OUTPUT ENEBLER (H : HIGH IMPEDANCE)
XB0-XB15	; XB PORT DATA
XBER	; XB PORT STATUS
XBHLD	; XB PORT OUTPUT HOLD (H : HOLD)
XBOE	; XB PORT OUTPUT ENEBLER (H : HIGH IMPEDANCE)
XSMPL	; ADDRESS SAMPLING SIGNAL OF HORIZONTAL DIRECTION
YA0-YA15	; YA PORT DATA
YAER	; YA PORT STATUS
YAHLD	; YA PORT OUTPUT HOLD (H : HOLD)
YAOE	; YA PORT OUTPUT ENEBLER (H : HIGH IMPEDANCE)
YB0-YB15	; YB PORT DATA
YBER	; YB PORT STATUS
YBHLD	; YB PORT OUTPUT HOLD (H : HOLD)
YBOE	; YB PORT OUTPUT ENEBLER (H : HIGH IMPEDANCE)
YSMPL	; ADDRESS SAMPLING SIGNAL OF VERTICAL DIRECTION



BP	; BACK PROCESSOR
COMMAND I/F	; COMMAND INTERFACE
CPU I/F	; CPU INTERFACE
ESG	; ERROR STATUS GENERATOR
FP	; FRONT PROCESSOR
NAM	; NON ADDITIVE MIX
SSG	; SAMPLING SIGNAL GENERATOR