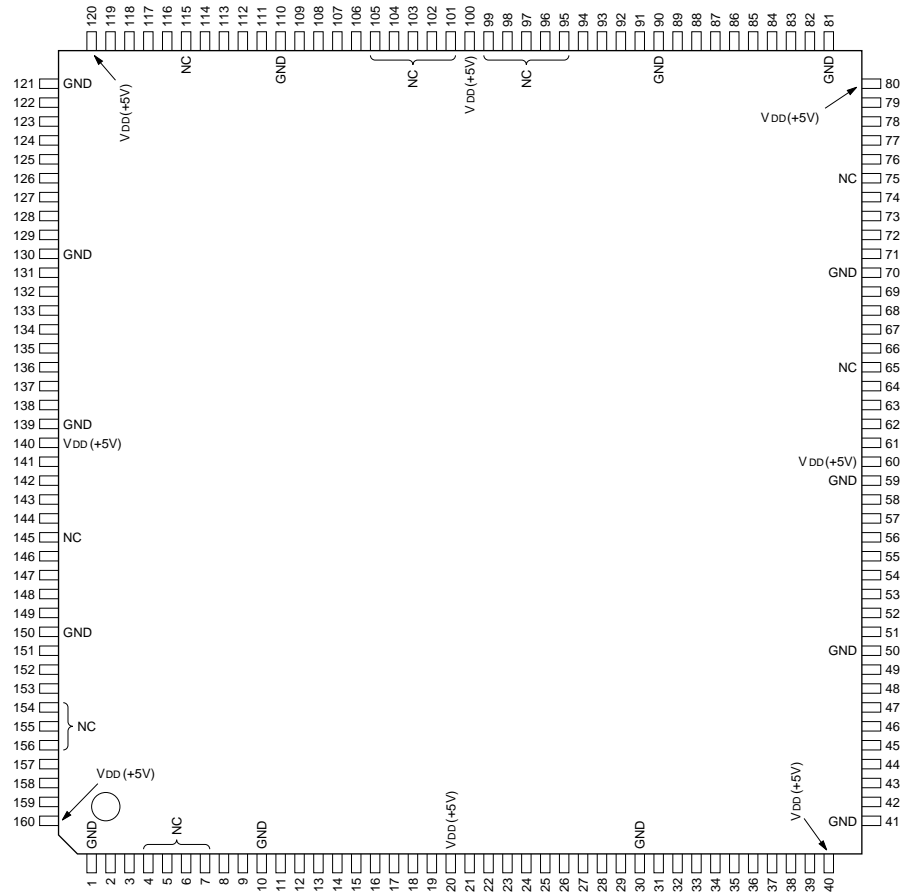

CXD8872Q (1/4)
IL08

C-MOS ADDRESS ARITHMETIC PROCESSOR FOR 2D EFFECT
- TOP VIEW -



CXD8872Q (2/4)

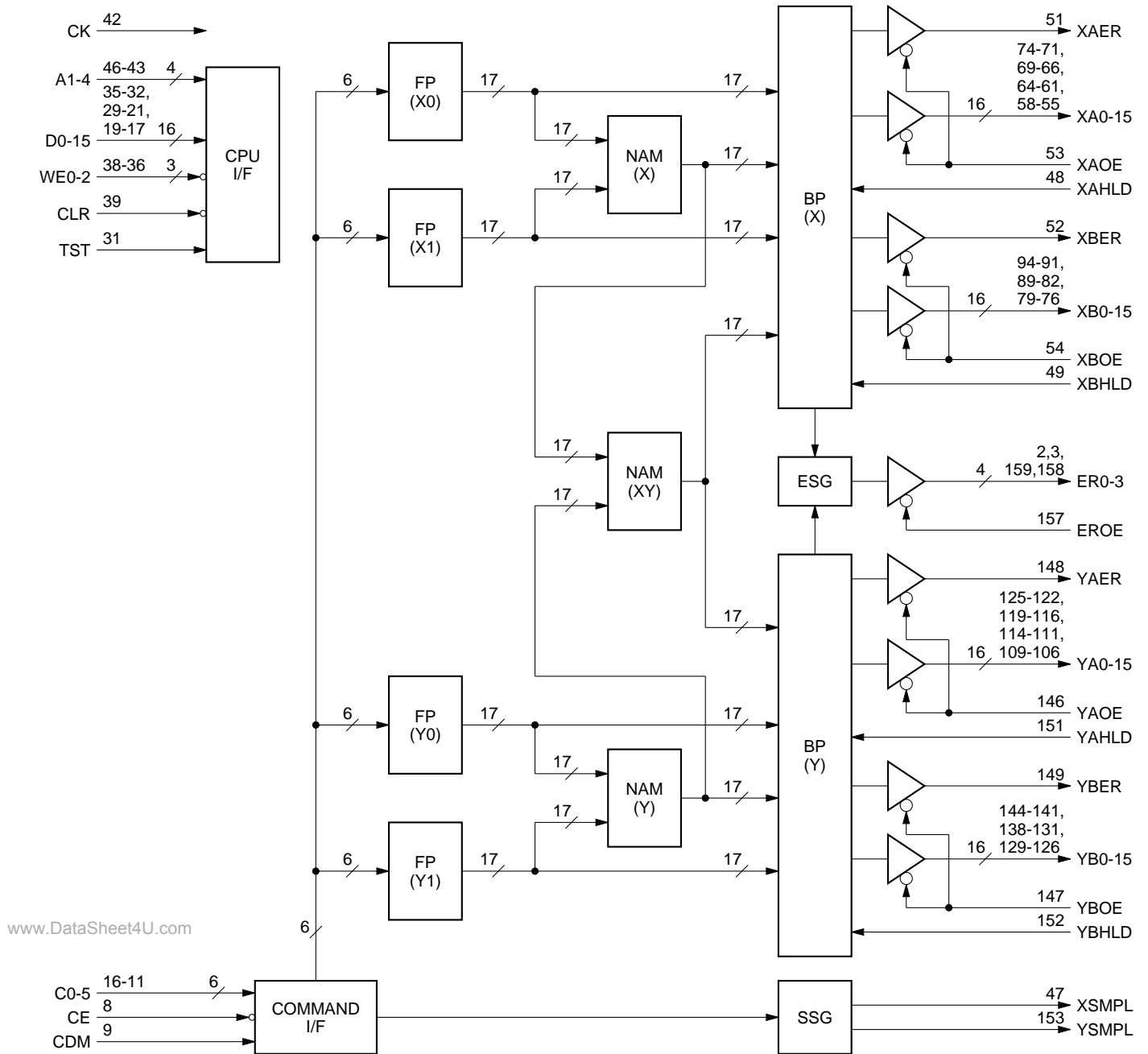
(V_{DD} = +5V)

PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	–	GND	41	–	GND	81	–	GND	121	–	GND
2	O	ER1	42	I	CK	82	O	XB11	122	O	YA3
3	O	ER0	43	I	A4	83	O	XB10	123	O	YA2
4	–	NC	44	I	A3	84	O	XB9	124	O	YA1
5	–	NC	45	I	A2	85	O	XB8	125	O	YA0
6	–	NC	46	I	A1	86	O	XB7	126	O	YB15
7	–	NC	47	O	XSMPL	87	O	XB6	127	O	YB14
8	I	CE	48	I	XAHLD	88	O	XB5	128	O	YB13
9	I	CDM	49	I	XBHLD	89	O	XB4	129	O	YB12
10	–	GND	50	–	GND	90	–	GND	130	–	GND
11	I	C5	51	O	XAER	91	O	XB3	131	O	YB11
12	I	C4	52	O	XBER	92	O	XB2	132	O	YB10
13	I	C3	53	I	XAOE	93	O	XB1	133	O	YB9
14	I	C2	54	I	XBOE	94	O	XB0	134	O	YB8
15	I	C1	55	O	XA15	95	–	NC	135	O	YB7
16	I	C0	56	O	XA14	96	–	NC	136	O	YB6
17	I	D15	57	O	XA13	97	–	NC	137	O	YB5
18	I	D14	58	O	XA12	98	–	NC	138	O	YB4
19	I	D13	59	–	GND	99	–	NC	139	–	GND
20	–	V _{DD}	60	–	V _{DD}	100	–	V _{DD}	140	–	V _{DD}
21	I	D12	61	O	XA11	101	–	NC	141	O	YB3
22	I	D11	62	O	XA10	102	–	NC	142	O	YB2
23	I	D10	63	O	XA9	103	–	NC	143	O	YB1
24	I	D9	64	O	XA8	104	–	NC	144	O	YB0
25	I	D8	65	–	NC	105	–	NC	145	–	NC
26	I	D7	66	O	XA7	106	O	YA15	146	I	YAOE
27	I	D6	67	O	XA6	107	O	YA14	147	I	YBOE
28	I	D5	68	O	XA5	108	O	YA13	148	O	YAER
29	I	D4	69	O	XA4	109	O	YA12	149	O	YBER
30	–	GND	70	–	GND	110	–	GND	150	–	GND
31	I	TST	71	O	XA3	111	O	YA11	151	I	YAHLD
32	I	D3	72	O	XA2	112	O	YA10	152	I	YBHLD
33	I	D2	73	O	XA1	113	O	YA9	153	O	YSMPL
34	I	D1	74	O	XA0	114	O	YA8	154	–	NC
35	I	D0	75	–	NC	115	–	NC	155	–	NC
36	I	WE2	76	O	XB15	116	O	YA7	156	–	NC
37	I	WE1	77	O	XB14	117	O	YA6	157	I	EROE
38	I	WE0	78	O	XB13	118	O	YA5	158	O	ER3
39	I	CLR	79	O	XB12	119	O	YA4	159	O	ER2
40	–	V _{DD}	80	–	V _{DD}	120	–	V _{DD}	160	–	V _{DD}

16	C0	XAER	51
15	C1	XA0	74
14	C2	XA1	73
13	C3	XA2	72
12	C4	XA3	71
11	C5	XA4	69
		XA5	68
8	CE	XA6	67
		XA7	66
9	CDM	XA8	64
		XA9	63
		XA10	62
53	XAOE	XA10	61
54	XBOE	XA11	58
48	XAHLD	XA12	57
49	XBHLD	XA13	56
146	YAOE	XA14	55
147	YBOE	XA15	55
151	YAHLD		52
152	YBHLD	XBER	94
		XB0	93
3	ER0	XB1	92
2	ER1	XB2	91
159	ER2	XB3	89
158	ER3	XB4	88
		XB5	87
157	EROE	XB6	86
		XB7	85
47	XSMPL	XB8	84
153	YSMPL	XB9	83
		XB10	82
46	A1	XB11	79
45	A2	XB12	78
44	A3	XB13	77
43	A4	XB14	76
		XB15	76
35	D0		148
34	D1	YAER	125
33	D2	YA0	124
32	D3	YA1	123
29	D4	YA2	122
28	D5	YA3	119
27	D6	YA4	118
26	D7	YA5	117
25	D8	YA6	116
24	D9	YA7	114
23	D10	YA8	113
22	D11	YA9	112
21	D12	YA10	111
19	D13	YA11	109
18	D14	YA12	108
17	D15	YA13	107
		YA14	106
		YA15	106
38	WE0		149
37	WE1		144
36	WE2	YBER	143
		YB0	142
39	CLR	YB1	141
		YB2	138
31	TST	YB3	137
		YB4	136
42		YB5	135
		YB6	134
		YB7	133
		YB8	132
		YB9	131
		YB10	129
		YB11	128
		YB12	127
		YB13	126
		YB14	126
		YB15	126

INPUT
A1-A4 ; ADDRESS
C0-C5 ; FP (FRONT PROCESSOR) CONTROL COMMAND
CE ; FP (FRONT PROCESSOR) CONTROL COMMAND ENABLE
CK ; CLOCK
CLR ; CLEAR
CMD ; COMMAND GENERATION MODE SELECT (L : INTERFACE MODE, H : DIRECT MODE)
D0-D15 ; DATA
TST ; IC TEST
WE0-WE2 ; WRITE ENABLE

OUTPUT
XA0-XA15 ; XA PORT DATA
XAER ; XA PORT STATUS
XAHLD ; XA PORT OUTPUT HOLD (H : HOLD)
XAOE ; XA PORT OUTPUT ENEBLER (H : HIGH IMPEDANCE)
XB0-XB15 ; XB PORT DATA
XBER ; XB PORT STATUS
XBHLD ; XB PORT OUTPUT HOLD (H : HOLD)
XBOE ; XB PORT OUTPUT ENEBLER (H : HIGH IMPEDANCE)
XSMPL ; ADDRESS SAMPLING SIGNAL OF HORIZONTAL DIRECTION
YA0-YA15 ; YA PORT DATA
YAER ; YA PORT STATUS
YAHLD ; YA PORT OUTPUT HOLD (H : HOLD)
YAOE ; YA PORT OUTPUT ENEBLER (H : HIGH IMPEDANCE)
YB0-YB15 ; YB PORT DATA
YBER ; YB PORT STATUS
YBHLD ; YB PORT OUTPUT HOLD (H : HOLD)
YBOE ; YB PORT OUTPUT ENEBLER (H : HIGH IMPEDANCE)
YSMPL ; ADDRESS SAMPLING SIGNAL OF VERTICAL DIRECTION



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- BP ; BACK PROCESSOR
- COMMAND I/F ; COMMAND INTERFACE
- CPU I/F ; CPU INTERFACE
- ESG ; ERROR STATUS GENERATOR
- FP ; FRONT PROCESSOR
- NAM ; NON ADDITIVE MIX
- SSG ; SAMPLING SIGNAL GENERATOR