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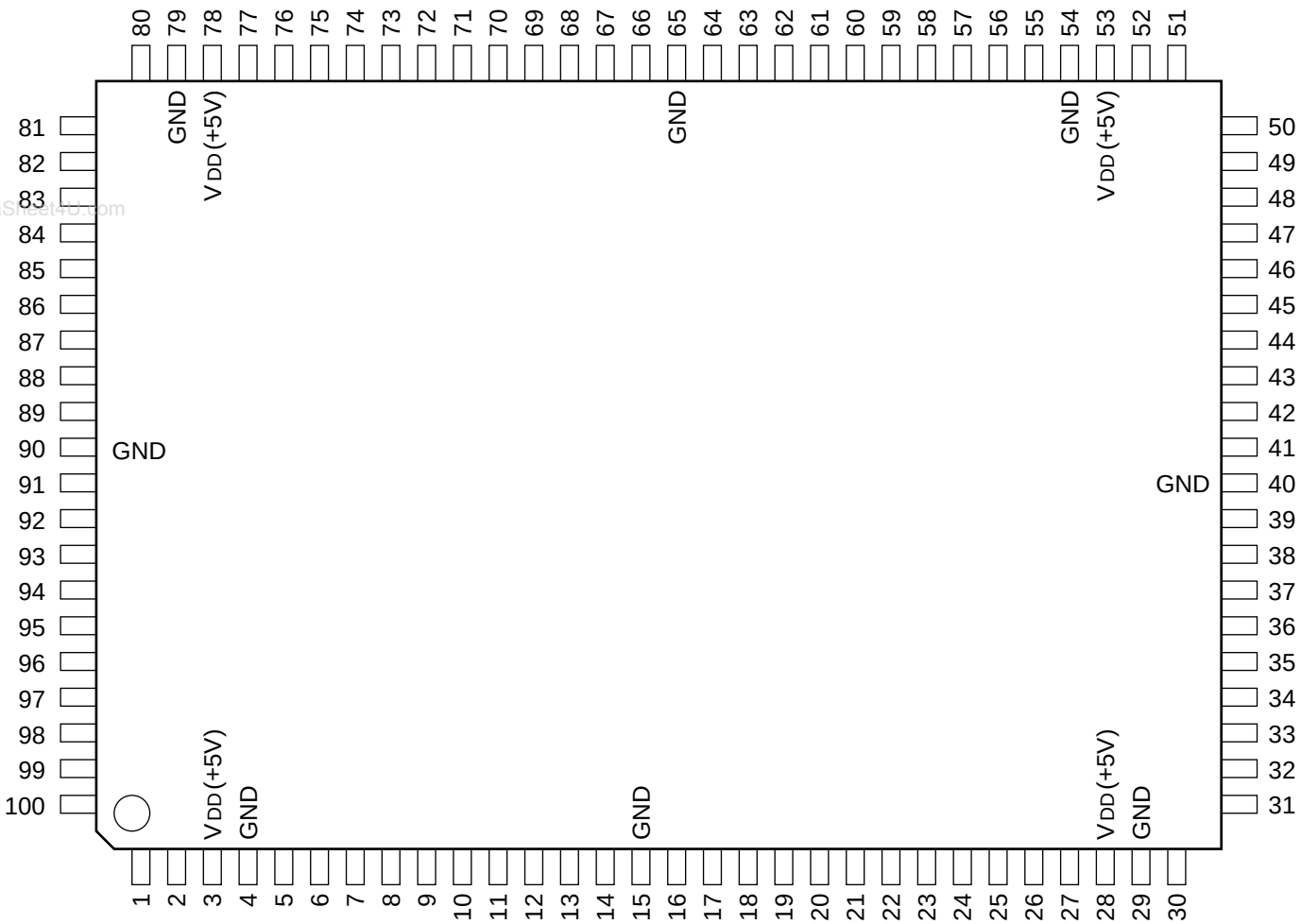
IL08

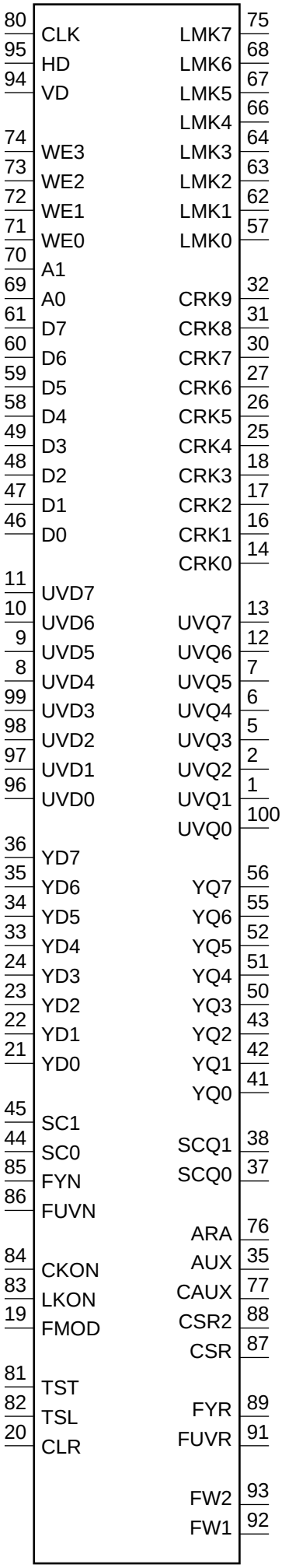
C-MOS CHROMA KEY PROCESSOR

- TOP VIEW -



(V_{DD} =+5V)

PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	O	UVQ1	26	O	CRK5	51	O	YQ4	76	O	ARA
2	O	UVQ2	27	O	CRK6	52	O	YQ5	77	O	CAUX
3	–	V_{DD}	28	–	V_{DD}	53	–	V_{DD}	78	–	V_{DD}
4	–	GND	29	–	GND	54	–	GND	79	–	GND
5	O	UVQ3	30	O	CRK7	55	O	YQ6	80	I	CLK
6	O	UVQ4	31	O	CRK8	56	O	YQ7	81	I	TST
7	O	UVQ5	32	O	CRK9	57	O	LMK0	82	I	TSL
8	I	UVD4	33	I	YD4	58	I	D4	83	I	LKON
9	I	UVD5	34	I	YD5	59	I	D5	84	I	CKON
10	I	UVD6	35	I	YD6	60	I	D6	85	I	FYN
11	I	UVD7	36	I	YD7	61	I	D7	86	I	FUVN
12	O	UVQ6	37	O	SCQ0	62	O	LMK1	87	O	CSR
13	O	UVQ7	38	O	SCQ1	63	O	LMK2	88	O	CSR2
14	O	CRK0	39	O	AUX	64	O	LMK3	89	O	FYR
15	–	GND	40	–	GND	65	–	GND	90	–	GND
16	O	CRK1	41	O	YQ0	66	O	LMK4	91	O	FUVR
17	O	CRK2	42	O	YQ1	67	O	LMK5	92	O	FW1
18	O	CRK3	43	O	YQ2	68	O	LMK6	93	O	FW2
19	I	FMOD	44	I	SC0	69	I	A0	94	I	VD
20	I	CLR	45	I	SC1	70	I	A1	95	I	HD
21	I	YD0	46	I	D0	71	I	WE0	96	I	UVD0
22	I	YD1	47	I	D1	72	I	WE1	97	I	UVD1
23	I	YD2	48	I	D2	73	I	WE2	98	I	UVD2
24	I	YD3	49	I	D3	74	I	WE3	99	I	UVD3
25	O	CRK4	50	O	YQ3	75	O	LMK7	100	O	UVQ0



INPUT

A0, 1	; ADDRESS DATA
CKON	; CHROMA KEY ON
CLK	; CLOCK
CLR	; CLEAR
D0-7	; CPU DATA
FMOD	; UV SAMPLING FREEQUENCY
FUVN	; UV FIFO NEXT DATA REQUEST (*1)
FYN	; Y FIFO NEXT DATA REQUEST (*1)
HD	; H SYNC
LKON	; LUMINANCE KEY ON
SC0, 1	; CYCLE
TSL	; TEST POINT SELECT
TST	; TEST
UVD0-7	; UV DATA
WE0-3	; WRITE ENABLE
YD	; Y
YD0-7	; Y DATA
VD	; V SYNC

OUTPUT

ARA	; CURSOR AREA
AUX	; AUX BIT DATA
CAUX	; CSR AND CAUX BIT OR OUTPUT
CRK0-9	; CHROMA KEY
CSR	; CURSOR
CSR2	; CSR 2 CLOCK DELAY
FUVR	; UV FIFO READ ENABLE (*1)
FW1	; FIFO WRITE ENABLE (*1)
FW2	; FIFO WRITE ENABLE (WITH DELAY) (*1)
FYR	; Y FIFO READ ENABLE (*1)
LMK0-7	; LUMINANCE KEY
SCQ0, 1	; CYCLE
UVQ0-7	; UV DATA
YQ0-7	; Y DATA

NOTE

*1 FIFO ; FIRST IN FIRST OUT