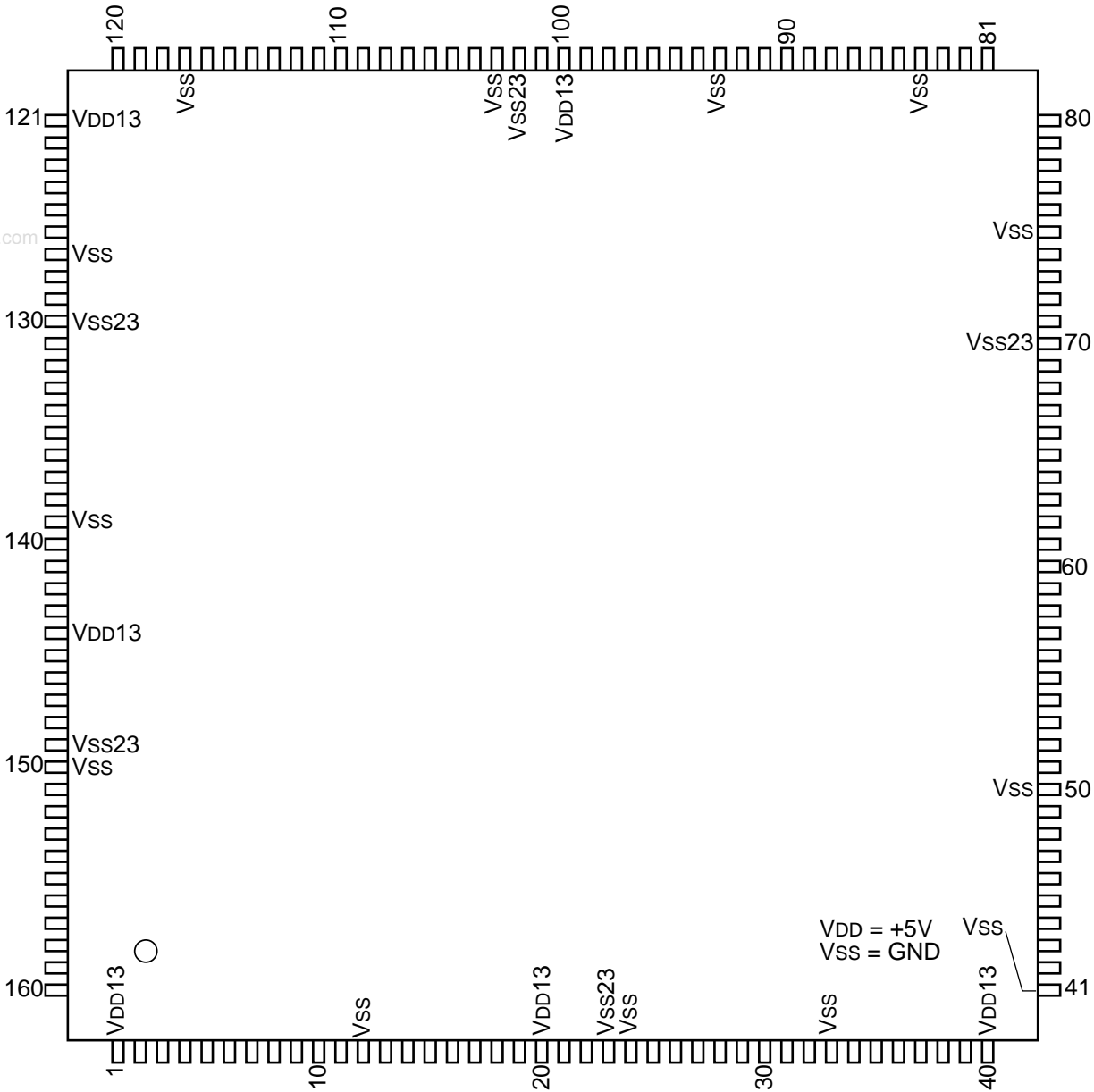


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### C-MOS ECC AND RLL1-7 ENCODE (GATE ARRAY)

-TOP VIEW-



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| PIN No. | I/O | SIGNAL    | PIN No. | I/O | SIGNAL     | PIN No. | I/O | SIGNAL     | PIN No. | I/O | SIGNAL     |
|---------|-----|-----------|---------|-----|------------|---------|-----|------------|---------|-----|------------|
| 1       | —   | VDD       | 41      | —   | Vss        | 81      | I/O | RAM2 I/O 5 | 121     | —   | VDD        |
| 2       | O   | DPBUF CS  | 42      | I/O | RAM1 I/O 0 | 82      | I/O | RAM2 I/O 6 | 122     | I/O | DATA I/O 4 |
| 3       | O   | DP CS     | 43      | I/O | RAM1 I/O 1 | 83      | I/O | RAM2 I/O 7 | 123     | I/O | DATA I/O 3 |
| 4       | I   | CK32M     | 44      | I/O | RAM1 I/O 2 | 84      | —   | Vss        | 124     | I/O | DATA I/O 2 |
| 5       | O   | SODN      | 45      | I/O | RAM1 I/O 3 | 85      | O   | RAM2 WE    | 125     | I/O | DATA I/O 1 |
| 6       | O   | SOCN      | 46      | I/O | RAM1 I/O 4 | 86      | O   | RAM2 A0    | 126     | I/O | DATA I/O 0 |
| 7       | O   | SODT      | 47      | I/O | RAM1 I/O 5 | 87      | O   | RAM2 A1    | 127     | —   | Vss        |
| 8       | O   | SOCT      | 48      | I/O | RAM1 I/O 6 | 88      | O   | RAM2 A2    | 128     | I   | CS3        |
| 9       | I   | CK46M     | 49      | I/O | RAM1 I/O 7 | 89      | O   | RAM2 A3    | 129     | I   | CS4        |
| 10      | O   | PTC CS    | 50      | —   | Vss (FIX)  | 90      | O   | RAM2 A4    | 130     | —   | Vss (FIX)  |
| 11      | O   | BUFC CS   | 51      | O   | RAM1 WE    | 91      | O   | RAM2 A5    | 131     | I   | CS6        |
| 12      | —   | Vss       | 52      | I   | WEEXT      | 92      | O   | RAM2 A6    | 132     | O   | SPC R/W    |
| 13      | O   | PI OE1    | 53      | O   | WEINT      | 93      | —   | Vss        | 133     | O   | UDS        |
| 14      | O   | PO WE1    | 54      | O   | BP 0       | 94      | O   | RAM2 A7    | 134     | O   | LDS        |
| 15      | O   | PI OE2    | 55      | O   | BP 1       | 95      | O   | RAM2 A8    | 135     | I   | CPU CK     |
| 16      | O   | PO WE2    | 56      |     |            | 96      | O   | RAM2 A9    | 136     | I   | WRH        |
| 17      | O   | SPC CS0   | 57      | I   | SIDN 0     | 97      | O   | RAM2 A10   | 137     | I   | WRL        |
| 18      | O   | SPC CS1   | 58      | I   | SIDN 1     | 98      | O   | RAM2 A11   | 138     | O   | WAIT       |
| 19      | O   | SPS RST   | 59      | I   | SICN       | 99      | O   | RAM2 A12   | 139     | —   | Vss        |
| 20      | —   | VDD (FIX) | 60      | I   | RENN       | 100     | —   | VDD (FIX)  | 140     | I/O | CPU D0     |
| 21      | I   | CPU RST   | 61      | I   | RSMN       | 101     | O   | RAM2 A13   | 141     | I/O | CPU D1     |
| 22      | I   | TGNTSEL   | 62      | I   | WRSTN      | 102     | —   | Vss        | 142     | I/O | CPU D2     |
| 23      | —   | Vss       | 63      | I   | WRSTT      | 103     | —   | Vss        | 143     | I/O | CPU D3     |
| 24      | —   | Vss       | 64      | I   | RENT       | 104     | I   | MCLK       | 144     | —   | VDD        |
| 25      | O   | RAM1 A0   | 65      | I   | RSMT       | 105     | O   | BP 4       | 145     | I/O | CPU D4     |
| 26      | O   | RAM1 A1   | 66      | O   | BP 2       | 106     | I   | CK25M      | 146     | I/O | CPU D5     |
| 27      | O   | RAM1 A2   | 67      | O   | BP 3       | 107     | O   | BUF EN     | 147     | I/O | CPU D6     |
| 28      | O   | RAM1 A3   | 68      | O   | SM EN      | 108     | O   | BP 5       | 148     | I/O | CPU D7     |
| 29      | O   | RAM1 A4   | 69      | I   | CHSEL      | 109     | O   | BP 6       | 149     | —   | Vss        |
| 30      | O   | RAM1 A5   | 70      | —   | Vss (FIX)  | 110     | O   | CRCERT     | 150     | —   | Vss (FIX)  |
| 31      | O   | RAM1 A6   | 71      | I   | SIDT 0     | 111     | O   | CRCERN     | 151     | I   | RD         |
| 32      | O   | RAM1 A7   | 72      | I   | SIDT 1     | 112     | O   | DERRT      | 152     | I   | CPU A0     |
| 33      | —   | Vss       | 73      | —   | VDD        | 113     | O   | DERRN      | 153     | I   | CPU A1     |
| 34      | O   | RAM1 A8   | 74      | I   | SICT       | 114     | I   | ECCTEST    | 154     | I   | CPU A2     |
| 35      | O   | RAM1 A9   | 75      | —   | Vss        | 115     | O   | DIR        | 155     | I   | CPU A3     |
| 36      | O   | RAM1 A10  | 76      | I/O | RAM2 I/O 0 | 116     | O   | BP 7       | 156     | I   | CPU A4     |
| 37      | O   | RAM1 A11  | 77      | I/O | RAM2 I/O 1 | 117     | —   | Vss        | 157     | I   | CPU A5     |
| 38      | O   | RAM1 A12  | 78      | I/O | RAM2 I/O 2 | 118     | I/O | DATA I/O 7 | 158     | I   | CPU A6     |
| 39      | O   | RAM1 A13  | 79      | I/O | RAM2 I/O 3 | 119     | I/O | DATA I/O 6 | 159     | I   | CPU A7     |
| 40      | —   | VDD       | 80      | I/O | RAM2 I/O 4 | 120     | I/O | DATA I/O 5 | 160     | I   | CA11       |

**INPUT**

|           |  |
|-----------|--|
| CA11      | ; CPU ADDRESS 11                               |
| CHSEL     | ; CHANNEL SELECT (L : CH1/H : CH2)             |
| CK25M     | ; MEMORY CONTROLLER CLOCK 2.5 MHz              |
| CK32M     | ; CHANNEL CLOCK (INSIDE) 32 MHz                |
| CK46M     | ; CHANNEL CLOCK (OUTSIDE) 46 MHz               |
| CPU A 0-7 | ; CPU ADDRESS                                  |
| CPU CK    | ; CPU CLOCK (20 MHz)                           |
| CPU RST   | ; RESET  |
| CS3, 4, 6 | ; CHIP SELECT                                  |
| ECCTEST   | ; H : ECC TEST MODE                            |
| MCLK      | ; ECC MASTER CLOCK (10 MHz)                    |
| RD        | ; CPU READ                                     |
| RENN      | ; READ ENABLE (INSIDE)                         |
| RENT      | ; READ ENABLE (OUTSIDE)                        |
| RSMN      | ; RESET SECTOR MARK (INSIDE)                   |
| RSMT      | ; RESET SECTOR MARK (OUTSIDE)                  |
| SICN      | ; SERIAL IN CLOCK (INSIDE)                     |
| SICT      | ; SERIAL IN CLOCK (OUTSIDE)                    |
| SIDN 0, 1 | ; SERIAL IN DATA (INSIDE)                      |
| SIDT 0, 1 | ; SERIAL IN DATA (OUTSIDE)                     |
| TGNTSEL   | ; REF. TIMING SELECT (L : INSIDE, H : OUTSIDE) |
| WEEXT     | ; EXTERNAL WE IN                               |
| WRH       | ; CPU WRITE (HIGH)                             |
| WRL       | ; CPU WRITE (LOW)                              |
| WRSTN     | ; WRITE RESET (INSIDE)                         |
| WRSTT     | ; WRITE RESET (OUTSIDE)                        |

**OUTPUT**

|             |   |
|-------------|---|
| BP 0-7      | ; BIT PORT                                |
| BUF EN      | ; BUFFER ENABLE                           |
| BUFC CS     | ; BUFFER CONTROLLER CHIP SELECT [OCYCEND] |
| CRCERN      | ; CRC ERROR (INSIDE)                      |
| CRCERT      | ; CRC ERROR (OUTSIDE)                     |
| DERRN       | ; DATA ERROR (INSIDE)                     |
| DERRT       | ; DATA ERROR (OUTSIDE)                    |
| DIR         | ; DIRECTION L : ENCODE/H : DECODE         |
| DP CS       | ; DUAL PORT RAM CHIP SELECT [OCDEND]      |
| DPBUF CS    | ; DUAL PORT BUFFER CHIP SELECT [OSTART]   |
| LDS         | ; SPC LOWER DATA SELECT                   |
| PI OE1      | ; PORT1 READ                              |
| PI OE2      | ; PORT2 READ [USGERR]                     |
| PO WE1      | ; PORT1 WRITE                             |
| PO WE2      | ; PORT2 WRITE                             |
| PTC CS      | ; PULSE TRAIN CONTROLLER CHIP SELECT      |
| RAM1 A 0-13 | ; MEMORY1 ADDRESS                         |
| RAM1 WE     | ; MEMORY1 WRITE ENABLE                    |
| RAM2 A 0-13 | ; MEMORY2 ADDRESS                         |
| RAM2 WE     | ; MEMORY2 WRITE ENABLE                    |
| SM EN       | ; SECTOR MARK ENABLE                      |
| SOCN        | ; SERIAL OUT CLOCK (INSIDE)               |
| SOCT        | ; SERIAL OUT CLOCK (OUTSIDE)              |
| SODN        | ; SERIAL OUT DATA (INSIDE)                |
| SODT        | ; SERIAL OUT DATA (OUTSIDE) [OCODEERR]    |
| SPC CS 0, 1 | ; SCSI PROTOCOL CONTROLLER CHIP SELECT    |
| SPC R W     | ; SPC READ/WRITE (H : READ/L : WRITE)     |
| SPC RST     | ; SCSI PROTOCOL CONTROLLER RESET          |
| UDS         | ; SPC UPPER DATA SELECT                   |
| WAIT        | ; CPU WAIT                                |
| WEINT       | ; INTERNAL WE OUT                         |

**INPUT/OUTPUT**

|             |                |
|-------------|----------------|
| CPU D 0-7   | ; CPU DATA     |
| DATAIO 0-7  | ; DATA I/O     |
| RAM1 IO 0-7 | ; MEMORY1 DATA |
| RAM2 IO 0-7 | ; MEMORY2 DATA |