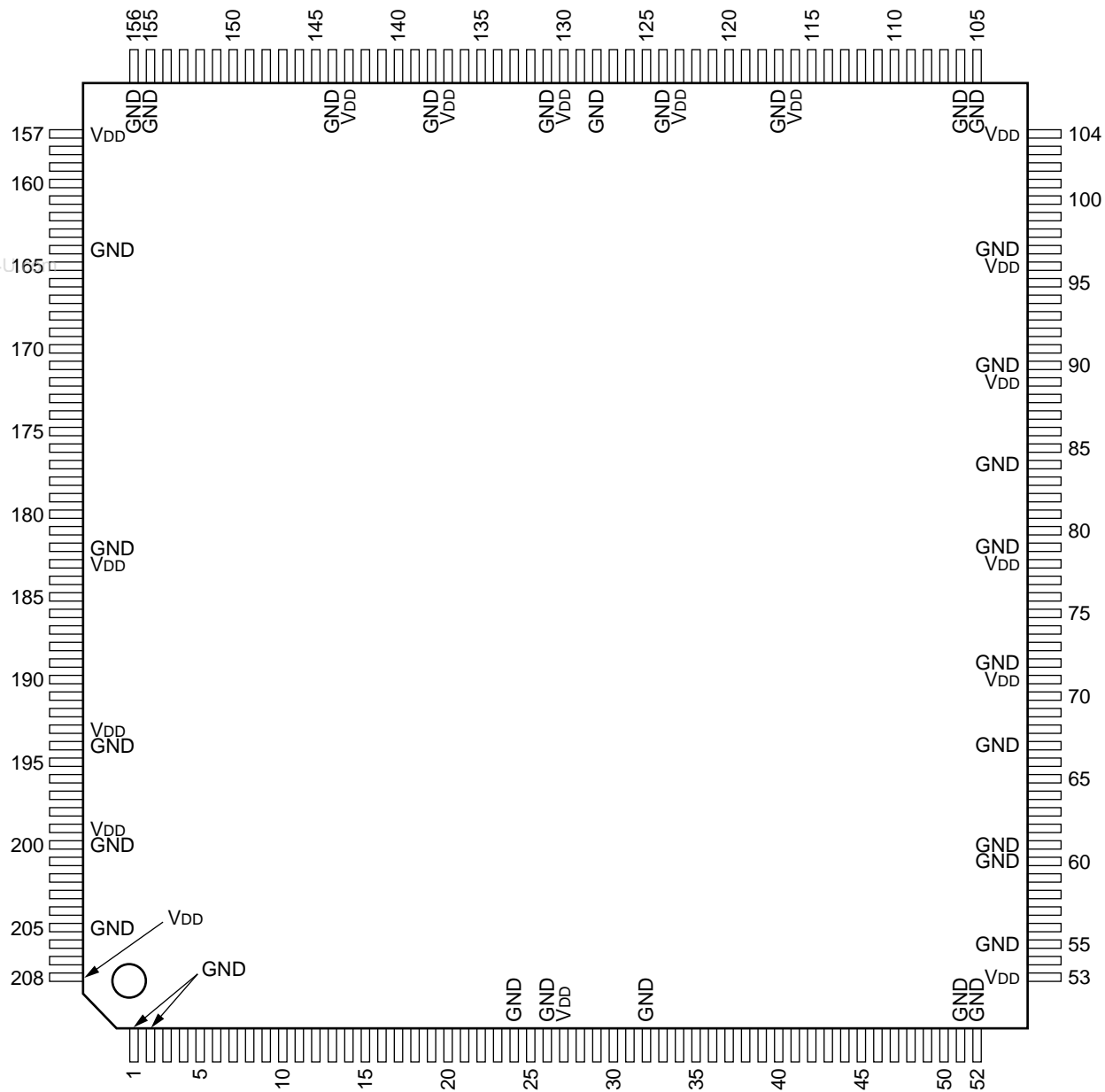


# C-MOS ECC OUTER DECODER

—TOP VIEW—



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PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	—	GND	53	—	V <sub>DD</sub>	105	—	GND	157	—	V <sub>DD</sub>
2	—	GND	54	I	CK27	106	—	GND	158	O	OBSY
3	I	AREID0	55	—	GND	107	I	MDTES1	159	I	RSTRT
4	I	AREID1	56	I	NTPLS	108	I	MDTES2	160	O	TESO0
5	I	SMC	57	I	DIN0	109	I	MDTES3	161	O	TESO1
6	I	SIN	58	I	DIN1	110	I	MDTES4	162	I	DECFR
7	O	SOT	59	I	DIN2	111	O	JADRS0	163	O	SYNCO
8	I	AREID2	60	—	GND	112	O	JADRS1	164	—	GND
9	I/O	SYSIO0	61	—	GND	113	O	JADRS2	165	O	DOUT0
10	I/O	SYSIO1	62	I	DIN3	114	O	JADRS3	166	O	DOUT1
11	I/O	SYSIO2	63	I	DIN4	115	O	JADRS4	167	O	DOUT2
12	I/O	SYSIO3	64	I	DIN5	116	—	V <sub>DD</sub>	168	O	DOUT3
13	I/O	SYSIO4	65	I	DIN6	117	—	GND	169	O	DOUT4
14	I/O	SYSIO5	66	I	DIN7	118	O	JADRS5	170	O	DOUT5
15	I/O	SYSIO6	67	—	GND	119	O	JADRS6	171	O	DOUT6
16	I/O	SYSIO7	68	I/O	NIODT0	120	O	JADRS7	172	O	DOUT7
17	I	IBUSEN	69	I/O	NIODT1	121	O	JADRS8	173	I	TMC1
18	O	OBUSEN	70	I/O	NIODT2	122	O	JADRS9	174	I	TMC2
19	I	$\overline{VD}$	71	—	V <sub>DD</sub>	123	—	V <sub>DD</sub>	175	O	EFLGO
20	I	STAT0	72	—	GND	124	—	GND	176	O	PRTYO
21	I	STAT1	73	I/O	NIODT3	125	O	JADRS10	177	O	FRMST
22	I	$\overline{STRB}$	74	I/O	NIODT4	126	O	JADRS11	178	O	GOPST
23	I	$\overline{CS}$	75	I/O	NIODT5	127	O	$\overline{JCKE}$	179	O	CYCID0
24	—	GND	76	I/O	NIODT6	128	—	GND	180	O	CYCID1
25	I	$\overline{RESET}$	77	I/O	NIODT7	129	I	CK54	181	O	CYCID2
26	—	GND	78	—	V <sub>DD</sub>	130	—	V <sub>DD</sub>	182	—	GND
27	—	V <sub>DD</sub>	79	—	GND	131	—	GND	183	—	V <sub>DD</sub>
28	I	SCK	80	O	$\overline{NWEN}$	132	O	$\overline{JWEN}$	184	O	TOUT0
29	I	AMC	81	O	$\overline{NRAS}$	133	O	$\overline{JRAS}$	185	O	TOUT1
30	I	BUNRI	82	O	$\overline{NCAS}$	134	O	$\overline{JCAS}$	186	O	TOUT2
31	I	TEST	83	O	$\overline{NCKE}$	135	O	$\overline{JCS0}$	187	O	TOUT3
32	—	GND	84	—	GND	136	O	JCS1	188	O	TOUT4
33	I	TIN0	85	O	NCS	137	—	V <sub>DD</sub>	189	O	TOUT5
34	I	TIN1	86	O	$\overline{NDQM}$	138	—	GND	190	O	TOUT6
35	I	TIN2	87	O	NADRS0	139	O	$\overline{JDQM}$	191	O	TOUT7
36	I	TIN3	88	O	NADRS1	140	I/O	JIODT0	192	O	TOUT8
37	I	TIN4	89	—	V <sub>DD</sub>	141	I/O	JIODT1	193	—	V <sub>DD</sub>
38	I	TIN5	90	—	GND	142	I/O	JIODT2	194	—	GND
39	I	TIN6	91	O	NADRS2	143	—	V <sub>DD</sub>	195	O	AU 1/2
40	I	TIN7	92	O	NADRS3	144	—	GND	196	O	AU 3/4
41	I	TIN8	93	O	NADRS4	145	I/O	JIODT3	197	O	$\overline{AVSTO}$
42	I	TIN9	94	O	NADRS5	146	I/O	JIODT4	198	O	SWFS
43	I	TIN10	95	O	NADRS6	147	I/O	JIODT5	199	—	V <sub>DD</sub>
44	I	TIN11	96	—	V <sub>DD</sub>	148	I/O	JIODT6	200	—	GND
45	I	TIN12	97	—	GND	149	I/O	JIODT7	201	I	FS512
46	I	TIN13	98	O	NADRS7	150	I	XMOD1	202	O	DEAUID0
47	I	XMOD0	99	O	NADRS8	151	I	SVBNK0	203	O	DEAUID1
48	I	REV	100	O	NADRS9	152	I	SVBNK1	204	O	DEAUID2
49	I	PRITY	101	O	NADRS10	153	I	SVBNK2	205	—	GND
50	I	$\overline{SYNC}$	102	O	NADRS11	154	I	SVBNK3	206	I	$\overline{AREFV}$
51	—	GND	103	I	MDTES0	155	—	GND	207	I	FS
52	—	GND	104	—	V <sub>DD</sub>	156	—	GND	208	—	V <sub>DD</sub>

**INPUT**

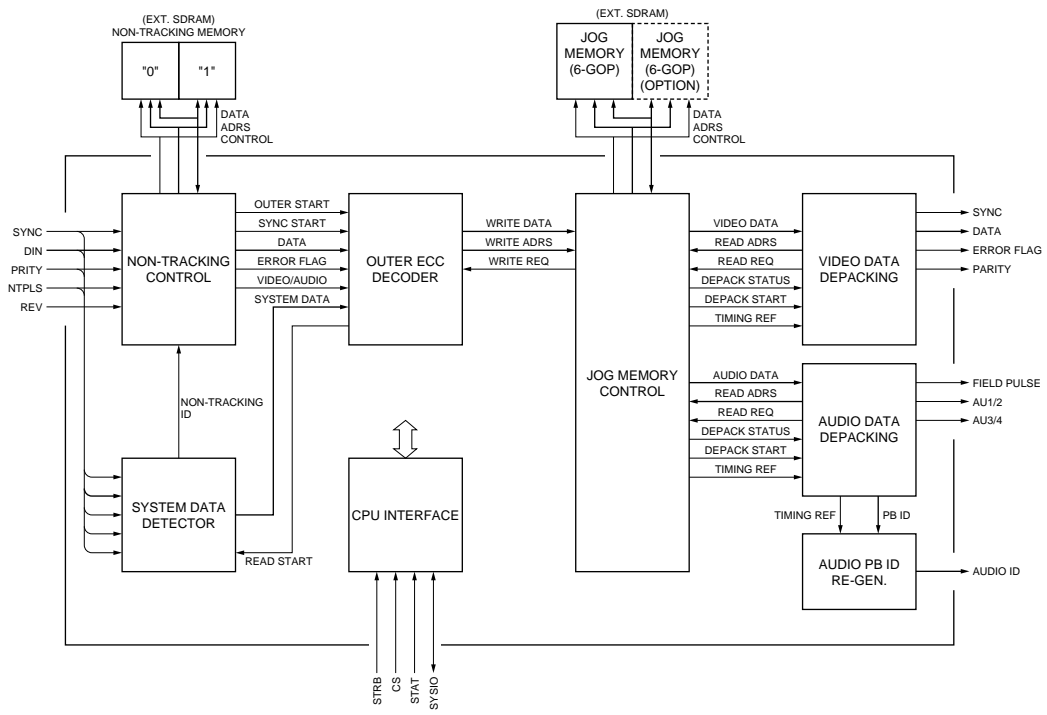
AMC	; ATG MODE CONTROL
AREFV	; AUDIO REFERENCE V
AREID0 - AREID2	; AUDIO REFERENCE ID
BUNRI	; RAM RELEASE TEST
CK27	; 27 MHz CLOCK
CK54	; 54 MHz CLOCK
CS	; CPU INTERFACE CHIP SELECT
DECFR	; DECODE FRAME
DIN0 - DIN7	; DATA
FS	; FS
FS512	; 512fs CLOCK
IBUSEN	; CPU I/F DATA BUS OUTPUT ENABLE
MDTES0 - MDTES4	; TEST MODE
NTPLS	; NON-TRACKING PULSE
PRITY	; PARITY
REEST	; POWER ON RESET
REV	; CAPSTAN FWD/REV (L : FWD, H : REV)
RSTRT	; JOG MEMORY READ START
SCK	; SCAN CLOCK
SIN	; TEST (SCAN CHECK)
SMC	; TEST (SCAN CHECK)
STAT0, STAT1	; CPU INTERFACE STAT
STRB	; CPU INTERFACE STROBE
SVBNK0 - SVBNK3	; JOG MEMORY BANK CONTROL
SYNC	; INNER SYNC
TEST	; RAM TEST MODE
TIN0 - TIN13	; TEST DATA
TMC1, TMC2	; TEST MODE CONTROL
VD	; VERTICAL DRIVE
XMOD0	; SYSTEM AUXILIARY DETECT MODE
XMOD1	; JOG MEMORY AUTO BANK MODE

**OUTPUT**

AU 1/2	; CH-1/CH-2 SERIAL AUDIO DATA
AU 3/4	; CH-3/CH-4 SERIAL AUDIO DATA
AVSTO	; AUDIO FIELD START
CYCID0 - CYCID2	; CYCLIC ID
DEAUDIO0 - DEAUDIO2	; DECODED AUDIO ID
DOU0 - DOU7	; BIT RATE REDUCTION STREAM DATA
EFLGO	; BIT RATE REDUCTION STREAM ERROR FLAG
FRMST	; FRAME START PULSE
GOPST	; GROUP OF PICTURE START PULSE
JADRS0 - JADRS11	; ADDRESS BUS FOR JOG MEMORY SDRAM
JCAS	; COLUMN ADDRESS STROBE FOR JOG MEMORY SDRAM
JCKE	; CLOCK ENABLE FOR JOG MEMORY SDRAM
JCS0, JCS1	; CHIP SELECT FOR JOG MEMORY SDRAM
JDQM	; DATA MASK CONTROL FOR JOG MEMORY SDRAM
JRAS	; RAW ADDRESS STROBE FOR JOG MEMORY SDRAM
JWEN	; WRITE ENABLE FOR JOG MEMORY SDRAM
NADRS0 - NADRS11	; ADDRESS BUS FOR NON-TRACKING SDRAM
NCAS	; COLUMN ADDRESS STROBE FOR NON-TRACKING SDRAM
NCKE	; CLOCK ENABLE FOR NON-TRACKING SDRAM
NCS	; CHIP SELECT FOR NON-TRACKING SDRAM
NDQM	; DATA MASK CONTROL FOR NON-TRACKING SDRAM
NRAS	; RAW ADDRESS STROBE FOR NON-TRACKING SDRAM
NWEN	; WRITE ENABLE FOR NON-TRACKING SDRAM
OBSY	; JOG MEMORY READ BUSY
OBUSEN	; CPU I/F DATA BUS OUTPUT ENABLE
PRTYO	; BIT RATE REDUCTION STREAM PARITY
SOT	; TEST (SCAN CHECK)
SWFS	; FS
SYNCO	; BIT RATE REDUCTION STREAM SYNC
TES00, TES01	; TEST DATA
TOUT0, TOUT8	; TEST DATA

**INPUT/OUTPUT**

JIODT0 - JIODT7	; DATA BUS FOR JOG MEMORY SDRAM
NIODT0 - NIODT7	; DATA BUS FOR NON-TRACKING SDRAM
SYSIO0 - SYSIO7	; CPU INTERFACE DATA BUS



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