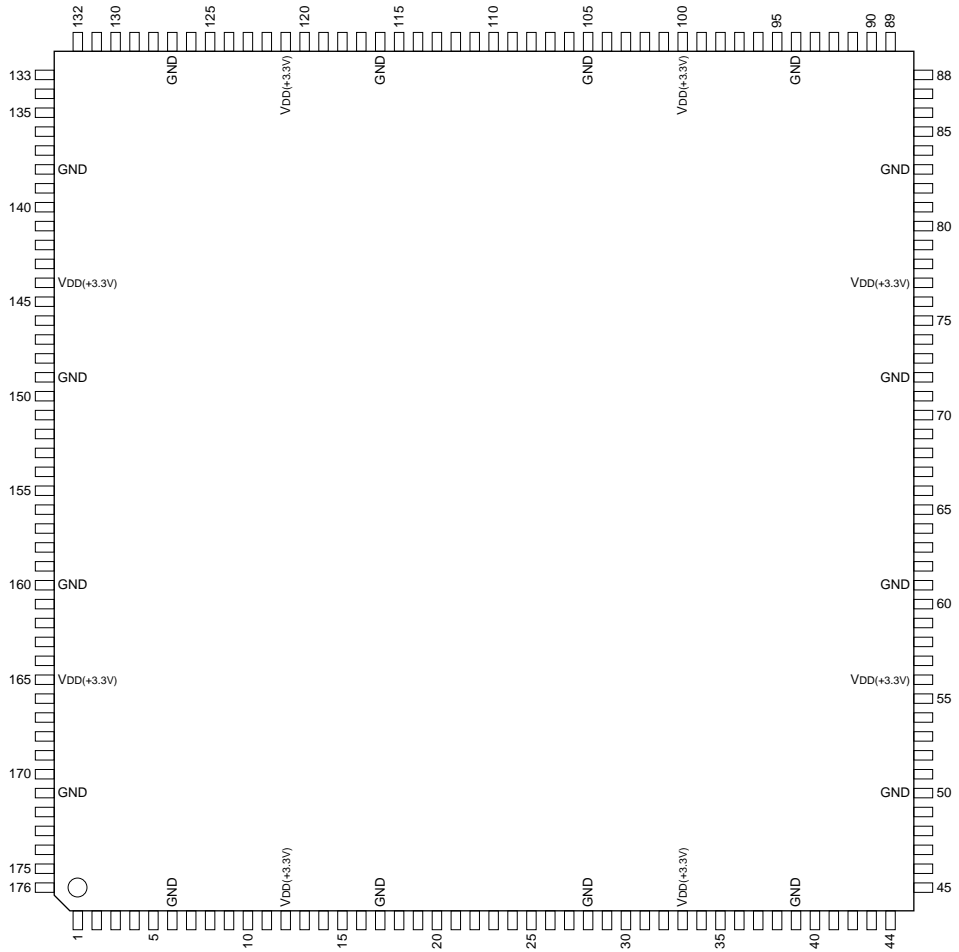

CXD8977R(1/5)
IL08

C-MOS SDDI VIDEO PACKING
-TOP VIEW-



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(V_{DD} = +3.3V)

PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	I	IRDFSL2	45	O	OPACKMD	89	O	OFIE2	133	O	OGTERR2
2	O	OWRFSL2	46	O	OBYPMD	90	O	OFWE21	134	O	OFTERR2
3	I	IRDFSL1	47	I	ICPU1	91	O	OFWE22	135	O	OLBERR2
4	O	OWRFSL1	48	I	ICPU0	92	O	OFRSTW2	136	O	OPERR2
5	I	IRESET	49	I	ICK27	93	O	OFWR20	137	I	IVDP2
6	—	GND	50	—	GND	94	—	GND	138	—	GND
7	I	TCKX	51	O	OENDVD	95	O	OFWR21	139	I	IVDMB2
8	O	OGFTOP2	52	I	IENVD	96	O	OFWR22	140	I	IVD27
9	O	OGFTOP1	53	I	IINTVD	97	O	OFWR23	141	I	IVD26
10	O	OEXIST2	54	O	OVDP	98	O	OFWR24	142	I	IVD25
11	O	OEXIST1	55	O	OVDMB	99	O	OFWR25	143	I	IVD24
12	—	V _{DD}	56	—	V _{DD}	100	—	V _{DD}	144	—	V _{DD}
13	O	OTRANS2	57	O	OVD7	101	O	OFWR26	145	I	IVD23
14	O	OTRANS1	58	O	OVD6	102	O	OFWR27	146	I	IVD22
15	O	OSTATE2	59	O	OVD5	103	O	OFMB2	147	I	IVD21
16	O	OSTATE1	60	O	OVD4	104	O	OFSY2	148	I	IVD20
17	—	GND	61	—	GND	105	—	GND	149	—	GND
18	O	OBYP2	62	O	OVD3	106	O	OFLB2	150	I	IVDP1
19	O	OBYP1	63	O	OVD2	107	O	OFVDP2	151	I	IVDMB1
20	O	OSHUTLE	64	O	OVD1	108	I	IREFV	152	I	IVD17
21	O	OFPERR	65	O	OVD0	109	I	XTST	153	I	IVD16
22	O	OMBERR	66	O	OOE	110	I	XSM	154	I	IVD15
23	O	OMBVAL	67	I	IOE	111	I	XWE	155	I	IVD14
24	O	OCPU1	68	O	OFOE1	112	O	OFIE1	156	I	IVD13
25	O	OCPU0	69	O	OFOE2	113	O	OFWE11	157	I	IVD12
26	O	OLACHMD	70	O	OFOE3	114	O	OFWE12	158	I	IVD11
27	O	ODEMD	71	O	OFOE4	115	O	OFRSTW1	159	I	IVD10
28	—	GND	72	—	GND	116	—	GND	160	—	GND
29	I/O	SYSIO0	73	O	OFRE	117	O	OFRCK27	161	O	OGTERR1
30	I/O	SYSIO1	74	O	OFRSTR	118	I	EA	162	O	OFTERR1
31	I/O	SYSIO2	75	I	IFRD0	119	O	OFWR10	163	O	OLBERR1
32	I/O	SYSIO3	76	I	IFRD1	120	O	OFWR11	164	O	OPERR1
33	—	V _{DD}	77	—	V _{DD}	121	—	V _{DD}	165	—	V _{DD}
34	I/O	SYSIO4	78	I	IFRD2	122	O	OFWR12	166	I	ISXP
35	I/O	SYSIO5	79	I	IFRD3	123	O	OFWR13	167	I	ISXMB
36	I/O	SYSIO6	80	I	IFRD4	124	O	OFWR14	168	I	ISX7
37	I/O	SYSIO7	81	I	IFRD5	125	O	OFWR15	169	I	ISX6
38	I	STRB	82	I	IFRD6	126	O	OFWR16	170	I	ISX5
39	—	GND	83	—	GND	127	—	GND	171	—	GND
40	I	STAT0	84	I	IFRD7	128	O	OFWR17	172	I	ISX4
41	I	STAT1	85	I	IFMB	129	O	OFMB1	173	I	ISX3
42	I	CS	86	I	IFSY	130	O	OFSY1	174	I	ISX2
43	I	XMM	87	I	IFLB	131	O	OFLB1	175	I	ISX1
44	I	IENCON	88	I	IFVDP	132	O	OFVDP1	176	I	ISX0

INPUT

$\overline{\text{CS}}$; CHIP SELECT
EA	; DC TEST
ICK27	; 27 MHz CLOCK
ICPU0, ICPU1	; EXTERNAL DATA
$\overline{\text{IENCON}}$; ENABLE SIGNAL FOR CONTROL DATA
IENVD	; VIDEO DATA ENABLE PULSE
IFLB	; FIFO READ DATA (LAST BYTE)
IFMB	; FIFO READ DATA (MB SYNC)
IFRD0 - IFRD7	; FIFO READ DATA
IFSY	; FIFO READ DATA (SYSTEM DATA INSERT)
IFVDP	; FIFO READ DATA (PARITY)
IINTVD	; VIDEO DATA INTERRUPT PULSE
IOE	; VIDEO DATA OUTPUT CONTROL
IRDFSL1, IRDFSL2	; READ FIFO SELECT
IREFV	; REFERENCE V
IRESET	; POWER ON RESET
ISX0 - ISX7	; SX ENCODER INPUT DATA
ISXMB	; SX ENCODER MB SYNC
ISXP	; SX ENCODER PARITY
IVD10 - IVD17	; OUTER 1 DATA
IVD20 - IVD27	; OUTER 2 DATA
IVDMB1, IVDMB2	; OUTER MB SYNC
IVDP1, IVDP2	; OUTER PARITY
STAT0, STAT1	; STATUS
STRB	; CPU STROBE
TCKX	; FOR RAM TEST
$\overline{\text{XMM}}$; RAM TEST MODE SELECT
$\overline{\text{XSM}}$; MAX-DATA TEST MODE
$\overline{\text{XTST}}$; MAX-DATA TEST MODE
$\overline{\text{XWE}}$; FOR RAM TEST

OUTPUT

OBYP1, OBYP2	; FOR MONITORING
OBYPMD	; FOR MONITORING
OCPU0, OCPU1	; CPU REGISTER OUTPUT
OEMD	; FOR MONITORING
OENDVD	; VIDEO DATA END PULSE
OEXIST1, OEXIST2	; FOR MONITORING
OFIE1	; FIFOs 3, 4 WRITE DATA INPUT ENABLE
OFIE2	; FIFOs 1, 2 WRITE DATA INPUT ENABLE
OFLB1	; FIFOs 3, 4 WRITE DATA (LAST BYTE)
OFLB2	; FIFOs 1, 2 WRITE DATA (LAST BYTE)
OFMB1	; FIFOs 3, 4 WRITE DATA (MB SYNC)
OFMB2	; FIFOs 1, 2 WRITE DATA (MB SYNC)
OFOE1 - OFOE4	; FIFOs 1 TO 4 OUTPUT ENABLE
OPERR	; FIFO INPUT PARITY ERROR
OFRCCK27	; 27 MHz MAIN CLOCK
OFRE	; CONTROL FIFO READ ENABLE
OFRSTR	; FIFO READ COUNTER RESET
OFIRSTW1	; FIFOs 1, 2 RESET WRITE POINTER
OFIRSTW2	; FIFOs 1, 2 RESET WRITE POINTER
OFSY1	; FIFOs 3, 4 WRITE DATA (SYSTEM DATA INSERT)
OFSY2	; FIFOs 1, 2 WRITE DATA (SYSTEM DATA INSERT)
OFTErr1	; FOR MONITORING (OUTER 1 FRAME HEADER MONITOR)
OFTErr2	; FOR MONITORING (OUTER 2 FRAME HEADER MONITOR)
OFVDP1	; FIFOs 3, 4 WRITE DATA (PARITY)
OFVDP2	; FIFOs 1, 2 WRITE DATA (PARITY)
OFWE11	; FIFO 3 WRITE ENABLE
OFWE12	; FIFO 4 WRITE ENABLE
OFWE21	; FIFO 1 WRITE ENABLE
OFWE22	; FIFO 2 WRITE ENABLE
OFWR10 - OFWR17	; FIFOs 3, 4 WRITE DATA
OFWR20 - OFWR27	; FIFOs 1, 2 WRITE DATA
OGFTOP1, OGFTOP2	; FOR MONITORING (GOP OR FRAME TOP ADDRESS MONITORING)
OGTErr1	; FOR MONITORING (OUTER 1 GOP HEADER ERROR)
OGTErr2	; FOR MONITORING (OUTER 2 GOP HEADER ERROR)
OLACHMD	; FOR MONITORING
OLBERR1	; FOR MONITORING (OUTER 1 LAST BYTE DET. ERROR)
OLBERR2	; FOR MONITORING (OUTER 2 LAST BYTE DET. ERROR)
OMBERR	; FOR MONITORING
OMBVAL	; FOR MONITORING
OOE	; VIDEO DATA OUTPUT ENABLE
OPACKMD	; FOR MONITORING
OPERR1	; FOR MONITORING
OPERR2	; FOR MONITORING
OSHUTLE	; FOR MONITORING
OSTATE1, OSTATE2	; FOR MONITORING
OTRANS1, OTRANS2	; FOR MONITORING
OVD0 - OVD7	; VIDEO OUTPUT DATA
OVDMB	; VIDEO MB SYNC DATA
OVDP	; VIDEO PARITY DATA
OWRFSL1, OWRFSL2	; WRITE FIFO SELECT

INPUT/OUTPUT

SYSIO0 - SYSIO7	; CPU BUS
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