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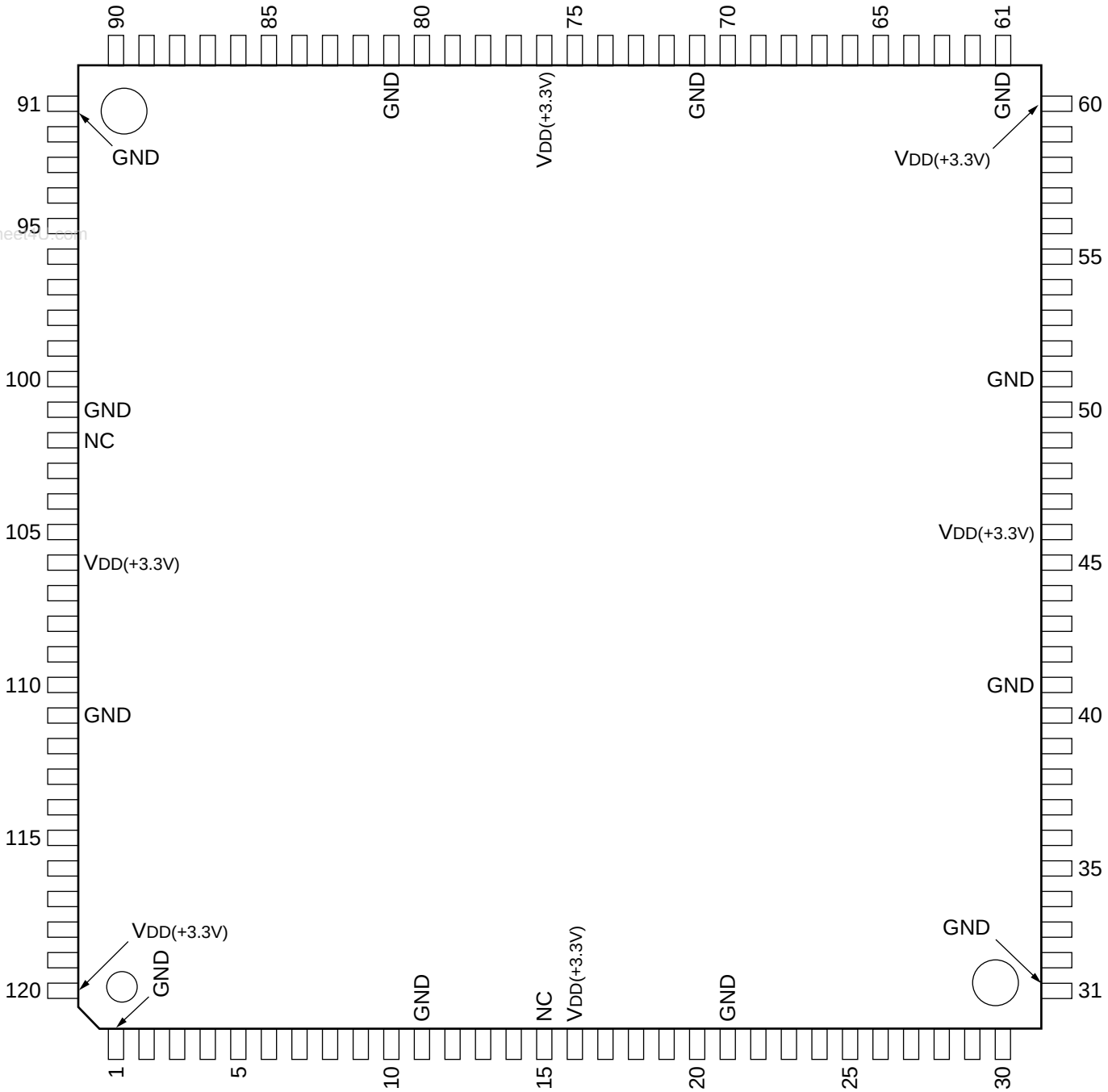
IL08

C-MOS SDDI AUDIO PACKING

–TOP VIEW–



(V_{DD} = +3.3V)

PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	—	GND	31	—	GND	61	—	GND	91	—	GND
2	I	TESTPI	32	O	AD8	62	I	RD5	92	O	OE1
3	I	TESTFCNT	33	O	AD7	63	I	RD6	93	O	WE2
4	I	$\overline{XSM}$	34	O	AD6	64	I	RD7	94	O	RE2
5	I	XTST	35	O	AD5	65	O	NGOPSTV	95	O	WE1
6	I	$\overline{TEST0}$	36	O	AD4	66	O	NEWDRT	96	O	RE1
7	I	$\overline{TEST1}$	37	O	AD3	67	O	O3WD7	97	O	O1WD3
8	I	$\overline{TEST2}$	38	O	AD2	68	O	O3WD6	98	O	O1WD2
9	I	EA	39	O	AD1	69	O	O3WD5	99	O	O1WD1
10	I	$\overline{RESET}$	40	O	AD0	70	O	O3WD4	100	O	O1WD0
11	—	GND	41	—	GND	71	—	GND	101	—	GND
12	O	BS1	42	O	PARITY	72	O	OE4	102	—	NC
13	O	FP1	43	O	OEPOUT	73	O	OE3	103	I	EMPHSEL
14	O	FEEDTEST	44	I	$\overline{INT2}$	74	O	WE4	104	I	I12CH
15	—	NC	45	I	CK27	75	O	RE4	105	I	I34CH
16	—	V_{DD}	46	—	V_{DD}	76	—	V_{DD}	106	—	V_{DD}
17	I/O	SYSIO0	47	I	$\overline{EN2}$	77	O	WE3	107	I	I2CH
18	I/O	SYSIO1	48	O	DATAEND	78	O	RE3	108	I	I3CH
19	I/O	SYSIO2	49	O	FCNT0	79	O	O3WD3	109	I	I4CH
20	I/O	SYSIO3	50	O	FCNT1	80	O	O3WD2	110	I	I64FS128
21	—	GND	51	—	GND	81	—	GND	111	—	GND
22	I/O	SYSIO4	52	O	PCHK12	82	O	O3WD1	112	I	AFRAID0
23	I/O	SYSIO5	53	O	PCHK34	83	O	O3WD0	113	I	AFRAID1
24	I/O	SYSIO6	54	I	RD0	84	O	O1WD7	114	I	AFRAID2
25	I/O	SYSIO7	55	I	RD1	85	O	O1WD6	115	I	STATUS12
26	I	STAT0	56	I	RD2	86	O	O1WD5	116	I	STATUS34
27	I	STAT1	57	I	RD3	87	O	O1WD4	117	I	$\overline{WRITEEN}$
28	I	$\overline{CS}$	58	O	RCK	88	O	RRST	118	I	$\overline{GOPST}$
29	I	STRB	59	I	RD4	89	O	WRST	119	I	FS4FS
30	I	REFV	60	—	V_{DD}	90	O	OE2	120	—	V_{DD}

INPUT

AFRAID0 - AFRAID2	;	AUDIO FRAME ID
CK27	;	27MHz CLOCK
$\overline{CS}$	;	CHIP SELECT
EA	;	IC TEST
EMPHSEL	;	EMPHASIS SELECT
EN2	;	READ ENABLE PULSE
FS4FS	;	AUDIO SYNC
$\overline{GOPST}$	;	GOP DATA START
I12CH	;	SERIAL AUDIO FOR CH-1/CH-2
I34CH	;	SERIAL AUDIO FOR CH-3/CH-4
I2CH	;	SERIAL AUDIO FOR CH-2
I3CH	;	SERIAL AUDIO FOR CH-3
I4CH	;	SERIAL AUDIO FOR CH-4
I64FS128	;	AUDIO CLOCK
$\overline{INT2}$	;	READ START PULSE OF FIFO MEMORY
RD0 - RD7	;	DATA INPUTS FROM FIFO MEMORY
REFV	;	REFERENCE V (FIELD) PULSE
RESET	;	RESET
STAT0, STAT1	;	CPU BUS STATUS
STATUS12	;	CH-1/CH-2 STATUS
STATUS34	;	CH-3/CH-4 STATUS
STRB	;	STROBE
$\overline{TEST0}$ - $\overline{TEST2}$	;	IC TEST
TESTFCNT	;	FRAME COUNTER TEST
TESTPI	;	FIFO MEMORY TEST
$\overline{WRITEEN}$	;	AUDIO DATA WRITE ENABLE
$\overline{XSM}$	;	SCAN TEST
XTST	;	SCAN TEST

OUTPUT

AD0 - AD8	;	AUDIO DATA
BS1	;	BLOCK START PULSE MONITOR
DATAEND	;	AUDIO DATA STREAM END PULSE
FCNT0, FCNT1	;	FRAME COUNTER
FEEDTEST	;	FEED MODE OR PARITY TEST MONITOR
FP1	;	FRAME START PULSE MONITOR
NEWDRT	;	READ PROHIBITIVE PULSE OF NEW FIFO DATA
NGOPSTV	;	GOP START DISCRIMINATION
O1WD0 -O1WD7	;	DATA OUTPUTS TO CH-1/CH-2 FIFO
O3WD0 -O3WD7	;	DATA OUTPUTS TO CH-3/CH-4 FIFO
OE1	;	OUTPUT ENABLE TO CH-1 FIFO
OE2	;	OUTPUT ENABLE TO CH-2 FIFO
OE3	;	OUTPUT ENABLE TO CH-3 FIFO
OE4	;	OUTPUT ENABLE TO CH-4 FIFO
OEPOUT	;	AD0 - AD8 STATUS SIGNAL
PARITY	;	PARITY
PCHK12	;	AUDIO CH-1/CH-2 INPUT PARITY CHECK
PCHK34	;	AUDIO CH-3/CH-4 INPUT PARITY CHECK
RCK	;	READ CLOCK (27 MHz) FOR FIFO MEMORY
RE1	;	READ ENABLE TO CH-1 FIFO
RE2	;	READ ENABLE TO CH-2 FIFO
RE3	;	READ ENABLE TO CH-3 FIFO
RE4	;	READ ENABLE TO CH-4 FIFO
RRST	;	READ RESET
WE1	;	WRITE ENABLE TO CH-1 FIFO
WE2	;	WRITE ENABLE TO CH-2 FIFO
WE3	;	WRITE ENABLE TO CH-3 FIFO
WE4	;	WRITE ENABLE TO CH-4 FIFO
WRST	;	WRITE RESET

INPUT/OUTPUT

SYSIO0 - SYSIO7	;	ADDRESS/DATA BUS