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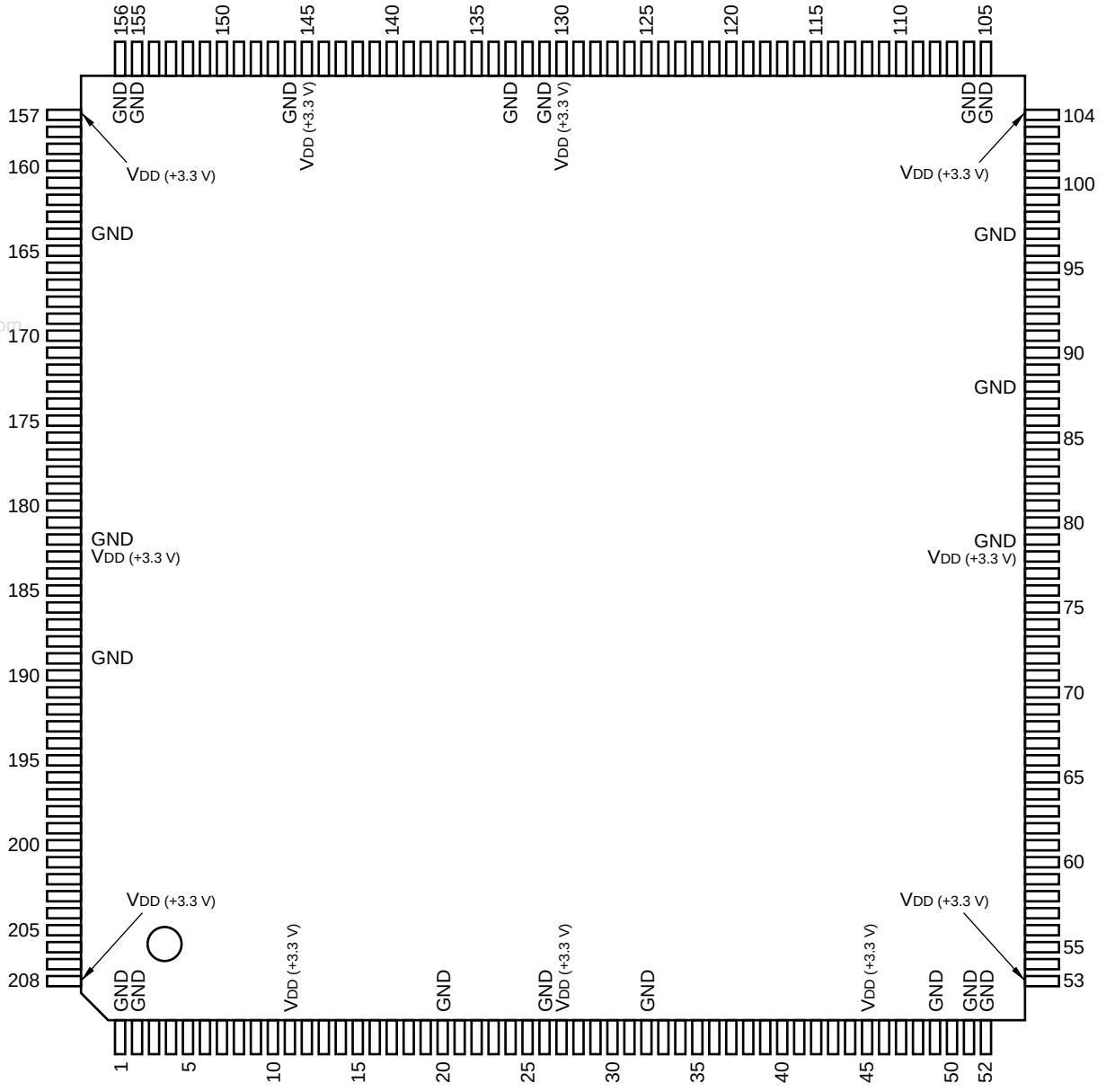
IL11

C-MOS SDDI AUDIO DEPACKING (GATE ARRAY)

- TOP VIEW -



(V_{DD} = +3.3 V)

PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	—	GND	43	I	$\overline{\text{DPRSTRB}}$	85	O	DOUT1	127	I	FRDIN7	169	O	DADDO9
2	—	GND	44	I	$\overline{\text{DPRCS}}$	86	O	DOUT2	128	I	DGATEI	170	I	DWFCSGI
3	O	MONIOUT0	45	—	V_{DD}	87	O	DOUT3	129	O	DGATEO	171	O	DWFCSGO
4	O	MONIOUT1	46	I	FREINS	88	—	GND	130	—	V_{DD}	172	I	DWFCSDI
5	O	MONIOUT2	47	I	$\overline{\text{RSTI}}$	89	O	DOUT4	131	—	GND	173	O	DWFCSDO
6	O	MONIOUT3	48	O	OUTP0	90	O	DOUT5	132	I	CK256FS	174	I	REF5F0
7	O	MONIOUT4	49	—	GND	91	O	DOUT6	133	—	GND	175	I	REF5F1
8	O	MONIOUT5	50	I	CK27M	92	O	DOUT7	134	I	FRDIN8	176	I	REF5F2
9	O	MONIOUT6	51	—	GND	93	O	NLSRF0	135	I	FRDIN9	177	I	$\overline{\text{FRAME}}$
10	O	MONIOUT7	52	—	GND	94	O	FWDTGT	136	I	FRDIN10	178	I	$\overline{\text{BLKP}}$
11	—	V_{DD}	53	—	V_{DD}	95	O	FWFNO0	137	I	FRDIN11	179	O	RPTFLAG
12	O	SIMOUT0	54	O	$\overline{\text{DFRST}}$	96	O	FWOE	138	I	FSIN	180	O	JMPFLAG1
13	O	SIMOUT1	55	I	NECFIFO	97	—	GND	139	I/O	DDATIO0	181	O	JMPFLAG2
14	O	SIMOUT2	56	I	STDSEL	98	O	NLSRF1	140	I/O	DDATIO1	182	—	GND
15	O	SIMOUT3	57	I	CHSEL	99	O	FWGOPF	141	I/O	DDATIO2	183	—	V_{DD}
16	O	SIMOUT4	58	I	SWDET	100	O	FWFNO1	142	I/O	DDATIO3	184	O	JMPFLAG3
17	O	SIMOUT5	59	I	PCERDI	101	O	FWVTRO	143	I/O	DDATIO4	185	O	JMPFLAG4
18	O	SIMOUT6	60	I	PRTYI	102	O	NLSRF2	144	I/O	DDATIO5	186	O	BRRDIR
19	O	SIMOUT7	61	I	$\overline{\text{AINTB}}$	103	O	FWFRMF	145	—	V_{DD}	187	O	SADO12
20	—	GND	62	I	$\overline{\text{ADENA}}$	104	—	V_{DD}	146	—	GND	188	O	SADO34
21	O	SIMOUT8	63	I	$\overline{\text{AINTA}}$	105	—	GND	147	I/O	DDATIO6	189	—	GND
22	O	SIMOUT9	64	I	SDDIH	106	—	GND	148	I/O	DDATIO7	190	I	SIMIN0
23	O	SIMOUT10	65	I	SDDIV	107	O	FWFNO2	149	I/O	DDATIO8	191	I	SIMIN1
24	O	SIMOUT11	66	I	SDDIF	108	O	FWFJPO	150	I/O	DDATIO9	192	I	SIMIN2
25	I	MDLSEL0	67	I	DIN0	109	O	NLSRF3	151	I/O	DDATIO10	193	I	SIMIN3
26	—	GND	68	I	DIN1	110	O	FWNLSR	152	I/O	DDATIO11	194	I	SIMIN4
27	—	V_{DD}	69	I	DIN2	111	O	FWFNO3	153	O	$\overline{\text{DRMRW}}$	195	I	SIMIN5
28	I	MDLSEL1	70	I	DIN3	112	O	FWFWDO	154	O	$\overline{\text{DRMRAS}}$	196	I	SIMIN6
29	I	MDLSEL2	71	I	DIN4	113	I	FRSTENI	155	—	GND	197	I	SIMIN7
30	I	MDLSEL3	72	I	DIN5	114	O	FRSTENO	156	—	GND	198	I	SIMIN8
31	I	SIMMODE	73	I	DIN6	115	O	FIFO RSTR	157	—	V_{DD}	199	I	SIMIN9
32	—	GND	74	I	DIN7	116	O	FIFORE1	158	O	$\overline{\text{DRMCAS}}$	200	I	SIMIN10
33	I	DPRST0	75	I	DIN8	117	O	FIFORE2	159	O	DADDO0	201	I	SIMIN11
34	I	DPRST1	76	I	DIN9	118	O	FIFORE3	160	O	DADDO1	202	I	SIMIN12
35	I/O	DPRD0	77	O	FIFORSTW	119	O	FIFORE4	161	O	DADDO2	203	I	SIMIN13
36	I/O	DPRD1	78	—	V_{DD}	120	I	FRDIN0	162	O	DADDO3	204	I	SIMIN14
37	I/O	DPRD2	79	—	GND	121	I	FRDIN1	163	O	DADDO4	205	I	SIMIN15
38	I/O	DPRD3	80	O	FIFOWE1	122	I	FRDIN2	164	—	GND	206	I	SIMIN16
39	I/O	DPRD4	81	O	FIFOWE2	123	I	FRDIN3	165	O	DADDO5	207	I	$\overline{\text{POR}}$
40	I/O	DPRD5	82	O	FIFOWE3	124	I	FRDIN4	166	O	DADDO6	208	—	V_{DD}
41	I/O	DPRD6	83	O	FIFOWE4	125	I	FRDIN5	167	O	DADDO7			
42	I/O	DPRD7	84	O	DOUT0	126	I	FRDIN6	168	O	DADDO8			

INPUT

$\overline{\text{ADENA}}$	; SDDI AUDIO ENABLE IN
$\overline{\text{AINTA}}$	; SDDI AUDIO INTERRUPT IN
$\overline{\text{AINTB}}$	; SDDI ATTRIBUTE INTERRUPT IN
$\overline{\text{BLKP}}$	; AUDIO BRR BLOCK
CHSEL	; CH1-4/5-8 SELECTION
CK27M	; SDDI 27 MHz CLOCK
CK256FS	; AUDIO 256 fs CLOCK
DGATEI	; FIFO READ DATA ACTIVE IN
DIN0 - DIN9	; SDDI DATA IN 0 - 9
$\overline{\text{DPRCS}}$	; DPR CHIP SELECT
DPRST0, DPRST1	; DPR STATUS 0, 1
$\overline{\text{DPRSTRB}}$	; DPR BUS STROBE
DWFCSDI	; DRAM WRITE FNO. IN
DWFCSGI	; DRAM WRITE FNO. GATE IN
$\overline{\text{FRAME}}$	; AUDIO FRAME
FRDIN0 - FRDIN11	; FIFO READ DATA 0 - 11
FREINS	; FIFO RE INSERTION
FRSTENI	; FIFO RSTW ENABLE IN
FSIN	; AUDIO FS IN
MDLSEL0 - MDLSEL3	; SIMULATION MODULE SELECT 0 - 3
NECFIFO	; FIFO SELECTION
PCERDI	; SDDI CRC ERROR
$\overline{\text{POR}}$	; POWER ON RESET
PRTYI	; SDDI PARITY
REF5F0 - REF5F2	; AUDIO 5F SEQUENCE 0 - 2
$\overline{\text{RSTI}}$	; SYSTEM RESET
SDDIF	; SDDI F IN
SDDIH	; SDDI H IN
SDDIV	; SDDI V IN
SIMIN0 - SIMIN16	; SIMULATION IN 0 - 16
SIMMODE	; SIMULATION MODE
STDSEL	; 525/625 SELECTION
SWDET	; SDDI SOURCE SWITCHING

OUTPUT

BRRDIR	; AUDIO BRR DIRECTION
DADDO0 - DADDO9	; DRAM ADDRESS 0 - 9
$\overline{\text{DFRST}}$	; INPUT DELAY CONTROL
DGATEO	; FIFO READ DATA ACTIVE OUT
$\overline{\text{DRMCAS}}$	; DRAM CAS
$\overline{\text{DRMRAS}}$	; DRAM RAS
$\overline{\text{DRMRW}}$	; DRAM R/W
DWFCSDO	; DRAM WRITE FNO. OUT
DWFCSGO	; DRAM WRITE FNO. GATE OUT
DOUT0 - DOUT7	; FIFO WRITE DATA 0 - 7
FIFORE1 - FIFORE4	; FIFO READ ENABLE 1 - 4
FIFORSTR	; FIFO RSTR
FIFORSTW	; FIFO RSTW
FIFOWE1 - FIFOWE4	; FIFO WRITE ENABLE 1 - 4
FWDTGT	; FIFO WRITE DATA ACTIVE
FWFNO0 - FWFNO3	; FIFO WRITE FRAMES 0 - 3
FWFJPO	; FIFO WRITE FRAME JUMP
FWFRMF	; FIFO WRITE FRAME FLAG
FWFWDO	; FIFO WRITE FWD/REV
FWGOPF	; FIFO WRITE GOP FLAG
FWNLSR	; FIFO WRITE OVERLAP EDIT FLAG
FWOE	; FIFO WRITE SAMPLE ODD/EVEN
FWVTRO	; FIFO WRITE DISK/VTR
FRSTENO	; FIFO RSTW ENABLE OUT
JMPFLAG1 - JMPFLAG4	; FRAME JUMP FLAG 1 - 4
MONIOUT0 - MONIOUT7	; MONITOR OUT 0 - 7
NLSRF0 - NLSRF3	; FIFO WRITE OVERLAP EDIT FRAMES 0 - 3
OUTP0	; OUTPUT PORT 0
RPTFLAG	; FRAME REPEAT FLAG
SADO12	; AUDIO DATA OUTPUT 12
SADO34	; AUDIO DATA OUTPUT 34
SIMOUT0 - SIMOUT11	; SIMULATION OUT 0 - 11

INPUT/OUTPUT

DDATIO0 - DDATIO11	; DRAM DATA IN/OUT 0 - 11
DPRD0 - DPRD7	; DPR DATA BUS IN/OUT 0 - 7