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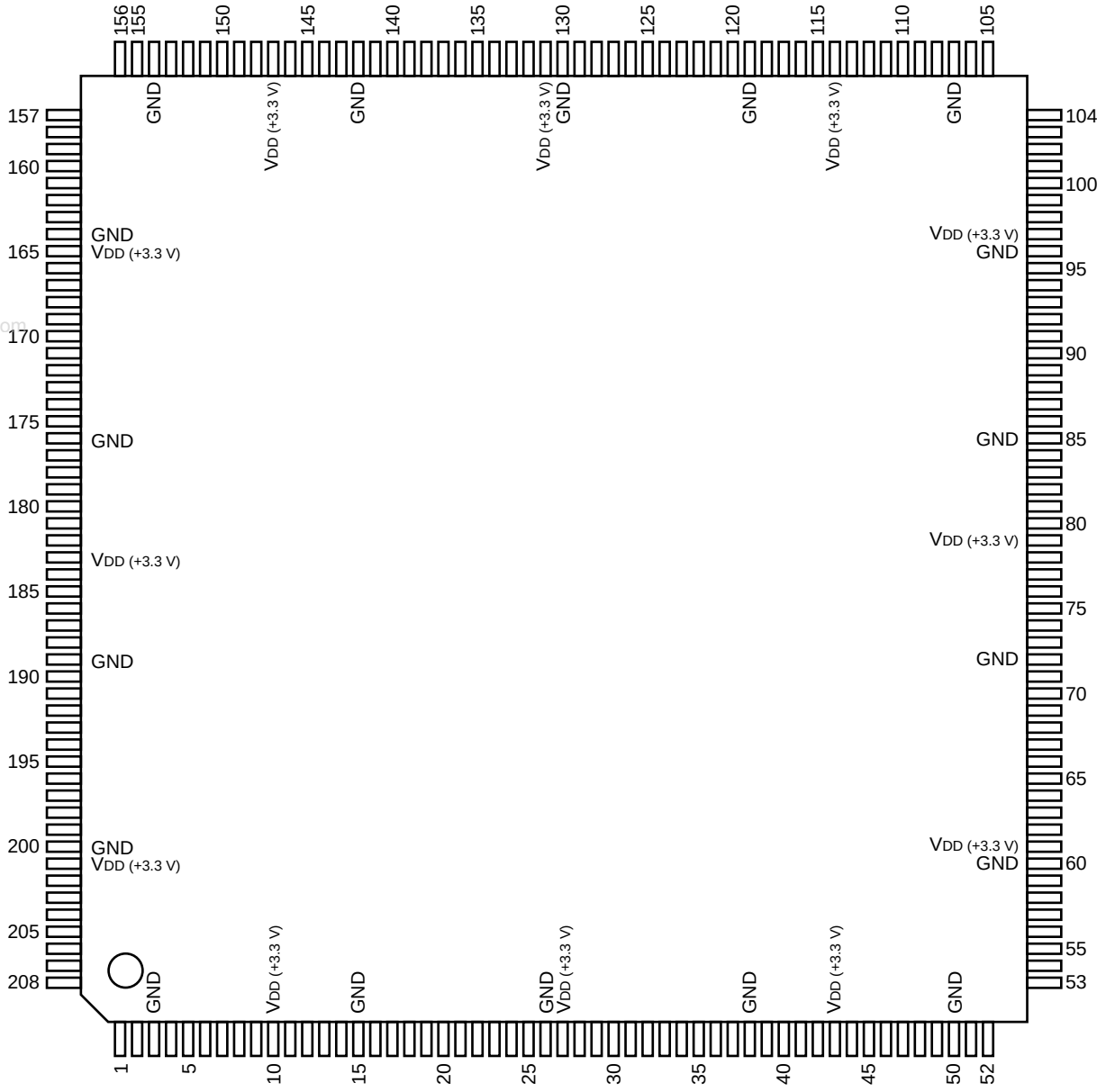
IL11

C-MOS SDDI VIDEO DEPACKING (GATE ARRAY)

- TOP VIEW -



(V_{DD} = +3.3 V)

PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	I	DIN9	43	—	V_{DD}	85	—	GND	127	O	$\overline{REB13}$	169	O	OUTFRM
2	I	DIN8	44	O	$\overline{INT}$	86	O	$\overline{WEA22}$	128	O	$\overline{REB12}$	170	O	DEC17
3	—	GND	45	O	$\overline{ATWRST}$	87	O	$\overline{WEA21}$	129	O	$\overline{REB11}$	171	O	DEC16
4	I	DIN7	46	O	$\overline{SYSWRST}$	88	O	$\overline{WEA20}$	130	—	GND	172	O	DEC15
5	I	DIN6	47	O	$\overline{ATWE}$	89	O	$\overline{WEB23}$	131	—	V_{DD}	173	O	DEC14
6	I	DIN5	48	O	$\overline{SYSWE}$	90	O	$\overline{WEB22}$	132	O	$\overline{REB10}$	174	O	DEC13
7	I	DIN4	49	O	$\overline{VEXIST}$	91	O	$\overline{WEB21}$	133	O	$\overline{RSTR1B}$	175	O	DEC12
8	I	DIN3	50	—	GND	92	O	$\overline{WEB20}$	134	I	MD27	176	—	GND
9	I	DIN2	51	O	$\overline{AEXIST}$	93	O	BSELH2	135	I	MD26	177	O	DEC11
10	—	V_{DD}	52	O	CPUCF	94	O	OBANK1	136	I	MD25	178	O	DEC10
11	I	DIN1	53	O	D1SEL	95	I	BANK1	137	I	MD24	179	O	$\overline{DEC1SYNC}$
12	I	DIN0	54	I	INCLK	96	—	GND	138	I	MD23	180	O	DEC1PTY
13	I	INF	55	O	MDOUT7	97	—	V_{DD}	139	I	MD22	181	O	DEC1ERR
14	I	INV	56	O	MDOUT6	98	O	OBANK2	140	I	MD21	182	O	ASELH2
15	—	GND	57	O	MDOUT5	99	I	BANK2	141	I	MD20	183	—	V_{DD}
16	I	$\overline{INH}$	58	O	MDOUT4	100	I	MD17	142	—	GND	184	I	XACK
17	I	INPTY	59	O	MDOUT3	101	I	MD16	143	I	$\overline{MSYNC2}$	185	I	BCK
18	I	$\overline{VINT}$	60	—	GND	102	I	MD15	144	I	MERR2	186	I	XTCK
19	I	$\overline{VEN}$	61	—	V_{DD}	103	I	MD14	145	I	MPTY2	187	O	DEC27
20	I	$\overline{AINT}$	62	O	MDOUT2	104	I	MD13	146	O	$\overline{OEA23}$	188	O	DEC26
21	I	$\overline{AEN}$	63	O	MDOUT1	105	I	MD12	147	—	V_{DD}	189	—	GND
22	I	$\overline{PCERD}$	64	O	MDOUT0	106	I	MD11	148	O	$\overline{OEA22}$	190	O	DEC25
23	I	$\overline{SWDET}$	65	O	$\overline{MDOSYNC}$	107	—	GND	149	O	$\overline{OEA21}$	191	O	DEC24
24	I	$\overline{LNEC}$	66	O	MDOERR	108	I	MD10	150	O	$\overline{OEA20}$	192	O	DEC23
25	O	ASELH1	67	O	MDOPTY	109	I	$\overline{MSYNC1}$	151	O	$\overline{REA23}$	193	O	DEC22
26	—	GND	68	O	$\overline{WRA}$	110	I	MERR1	152	O	$\overline{REA22}$	194	O	DEC21
27	—	V_{DD}	69	O	$\overline{WRB}$	111	I	MPTY1	153	O	$\overline{REA21}$	195	O	DEC20
28	I	$\overline{RST}$	70	O	$\overline{WEA13}$	112	O	$\overline{OEA13}$	154	—	GND	196	O	$\overline{DEC2SYNC}$
29	I/O	SYSI07	71	O	$\overline{WEA12}$	113	O	$\overline{OEA12}$	155	O	$\overline{REA20}$	197	O	DEC2PTY
30	I/O	SYSI06	72	—	GND	114	—	V_{DD}	156	O	$\overline{RSTR2A}$	198	O	DEC2ERR
31	I/O	SYSI05	73	O	$\overline{WEA11}$	115	O	$\overline{OEA11}$	157	O	$\overline{OEB23}$	199	O	BSELH1
32	I/O	SYSI04	74	O	$\overline{WEA10}$	116	O	$\overline{OEA10}$	158	O	$\overline{OEB22}$	200	—	GND
33	I/O	SYSI03	75	O	$\overline{WEB13}$	117	O	$\overline{REA13}$	159	O	$\overline{OEB21}$	201	—	V_{DD}
34	I/O	SYSI02	76	O	$\overline{WEB12}$	118	O	$\overline{REA12}$	160	O	$\overline{OEB20}$	202	I	OUTCLK
35	I/O	SYSI01	77	O	$\overline{WEB11}$	119	—	GND	161	O	$\overline{REB23}$	203	I	$\overline{TEST0}$
36	I/O	SYSI00	78	O	$\overline{WEB10}$	120	O	$\overline{REA11}$	162	O	$\overline{REB22}$	204	I	TEST1
37	I	STATE1	79	—	V_{DD}	121	O	$\overline{REA10}$	163	O	$\overline{REB21}$	205	I	TEST2
38	—	GND	80	I	XSM	122	O	$\overline{RSTR1A}$	164	—	GND	206	I	$\overline{REFHD}$
39	I	STATE0	81	I	XTST	123	O	$\overline{OEB13}$	165	—	V_{DD}	207	I	$\overline{REFVD}$
40	I	$\overline{STRB}$	82	I	SDI0	124	O	$\overline{OEB12}$	166	O	$\overline{REB20}$	208	I	REFCFI
41	I	$\overline{CS}$	83	O	SDO0	125	O	$\overline{OEB11}$	167	O	$\overline{RSTR2B}$			
42	O	$\overline{HRST}$	84	O	$\overline{WEA23}$	126	O	$\overline{OEB10}$	168	I	OSDRW			

INPUT

$\overline{\text{AEN}}$	; ATTRIBUTE DATA ENABLE
$\overline{\text{AINT}}$	; ATTRIBUTE DATA INTERRUPT
BANK1, BANK2	; FIFO MEMORY BANK SELECT1, 2
BCK	; TEST
$\overline{\text{CS}}$	; CPU I/F (CHIP SELECT)
DIN0 - DIN9	; SDDI DATA
INCLK	; INPUT CLOCK
INF	; INPUT FRAME PULSE
$\overline{\text{INH}}$	; INPUT H PULSE
INPTY	; INPUT PARITY
INV	; INPUT V PULSE
$\overline{\text{LNEC}}$	; FIFO MEMORY SELECT
MD10 - MD17	; FIFO MEMORY INPUT DATA1
MD20 - MD27	; FIFO MEMORY INPUT DATA2
MERR1, MERR2	; FIFO MEMORY INPUT ERROR1, 2
MPTY1, MPTY2	; FIFO MEMORY INPUT PARITY1, 2
$\overline{\text{MSYNC1}}$, $\overline{\text{MSYNC2}}$	; FIFO MEMORY INPUT SYNC1, 2
OSDRW	; EXTERNAL LOCK
OUTCLK	; OUTPUT CLOCK
$\overline{\text{PCERD}}$	; SDDI ERROR
REFCFI	; REFERENCE CF INFORMATION
$\overline{\text{REFHD}}$	; REFERENCE HD
$\overline{\text{REFVD}}$	; REFERENCE VD
$\overline{\text{RST}}$	; RESET
SDI0	; TEST
STATE0, STATE1	; CPU I/F (MODE SELECT)
$\overline{\text{STRB}}$	; CPU I/F (STROBE)
$\overline{\text{SWDET}}$	; SDDI SWITCHING DETECT
$\overline{\text{TEST0}}$ - TEST2	; TEST
$\overline{\text{VEN}}$	; VIDEO DATA ENABLE
$\overline{\text{VINT}}$	; VIDEO DATA INTERRUPT
XACK	; TEST
XSM	; TEST
XTCK	; TEST
XTST	; TEST

OUTPUT

$\overline{\text{AEXIST}}$	; ATTRIBUTE EXIST
ASELH1, ASELH2	; FIFO MEMORY READ SELECT (A)
$\overline{\text{ATWE}}$	; FIFO MEMORY WRITE ENABLE (ATTRIBUTE)
$\overline{\text{ATWRST}}$	; FIFO MEMORY WRITE RESET (ATTRIBUTE)
BSELH1, BSELH2	; FIFO MEMORY READ SELECT (B)
CPUCF	; INPUT CF PULSE
D1SEL	; DECODER SELECT
DEC0 - DEC17	; VIDEO STREAM DATA1
DEC1ERR	; STREAM ERROR1
DEC1PTY	; STREAM PARITY1
$\overline{\text{DEC1SYNC}}$	; STREAM SYNC1
DEC0 - DEC27	; VIDEO STREAM DATA2
DEC2ERR	; STREAM ERROR2
DEC2PTY	; STREAM PARITY2
$\overline{\text{DEC2SYNC}}$	; STREAM SYNC2
$\overline{\text{HRST}}$	; FIFO MEMORY WRITE RESET (1H DELAY)
$\overline{\text{INT}}$	; CPU INTERRUPT
MDOERR	; FIFO MEMORY OUTPUT ERROR
MDOPTY	; FIFO MEMORY OUTPUT PARITY
$\overline{\text{MDOSYNC}}$	; FIFO MEMORY OUTPUT SYNC
MDOUT0 - MDOUT7	; FIFO MEMORY OUTPUT DATA
OBANK1, OBANK2	; FIFO MEMORY BANK SELECT1, 2
$\overline{\text{OEA10}}$ - $\overline{\text{OEA13}}$	; FIFO MEMORY OUTPUT ENABLE (1A)
$\overline{\text{OEA20}}$ - $\overline{\text{OEA23}}$	; FIFO MEMORY OUTPUT ENABLE (2A)
$\overline{\text{OEB10}}$ - $\overline{\text{OEB13}}$	; FIFO MEMORY OUTPUT ENABLE (1B)
$\overline{\text{OEB20}}$ - $\overline{\text{OEB23}}$	; FIFO MEMORY OUTPUT ENABLE (2B)
OUTFRM	; OUTPUT FRAME PULSE
$\overline{\text{REA10}}$ - $\overline{\text{REA13}}$	; FIFO MEMORY READ ENABLE (1A)
$\overline{\text{REA20}}$ - $\overline{\text{REA23}}$	; FIFO MEMORY READ ENABLE (2A)
$\overline{\text{REB10}}$ - $\overline{\text{REB13}}$	; FIFO MEMORY READ ENABLE (1B)
$\overline{\text{REB20}}$ - $\overline{\text{REB23}}$	; FIFO MEMORY READ ENABLE (2B)
$\overline{\text{RSTR1A}}$	; FIFO MEMORY READ RESET (1A)
$\overline{\text{RSTR1B}}$	; FIFO MEMORY READ RESET (1B)
$\overline{\text{RSTR2A}}$	; FIFO MEMORY READ RESET (2A)
$\overline{\text{RSTR2B}}$	; FIFO MEMORY READ RESET (2B)
SDO0	; TEST
$\overline{\text{SYSWE}}$	; FIFO MEMORY WRITE ENABLE (SYS)
$\overline{\text{SYSWRST}}$	; FIFO MEMORY WRITE RESET (SYS)
$\overline{\text{VEXIST}}$	; VIDEO DATA EXIST
$\overline{\text{WEA10}}$ - $\overline{\text{WEA13}}$	; FIFO MEMORY WRITE ENABLE (1A)
$\overline{\text{WEA20}}$ - $\overline{\text{WEA23}}$	; FIFO MEMORY WRITE ENABLE (2A)
$\overline{\text{WEB10}}$ - $\overline{\text{WEB13}}$	; FIFO MEMORY WRITE ENABLE (1B)
$\overline{\text{WEB20}}$ - $\overline{\text{WEB23}}$	; FIFO MEMORY WRITE ENABLE (2B)
$\overline{\text{WRA}}$	; FIFO MEMORY WRITE RESET (A)
$\overline{\text{WRB}}$	; FIFO MEMORY WRITE RESET (B)

INPUT/OUTPUT

SYSIO0 - SYSIO7	; CPU I/F (ADDRESS & DATA)