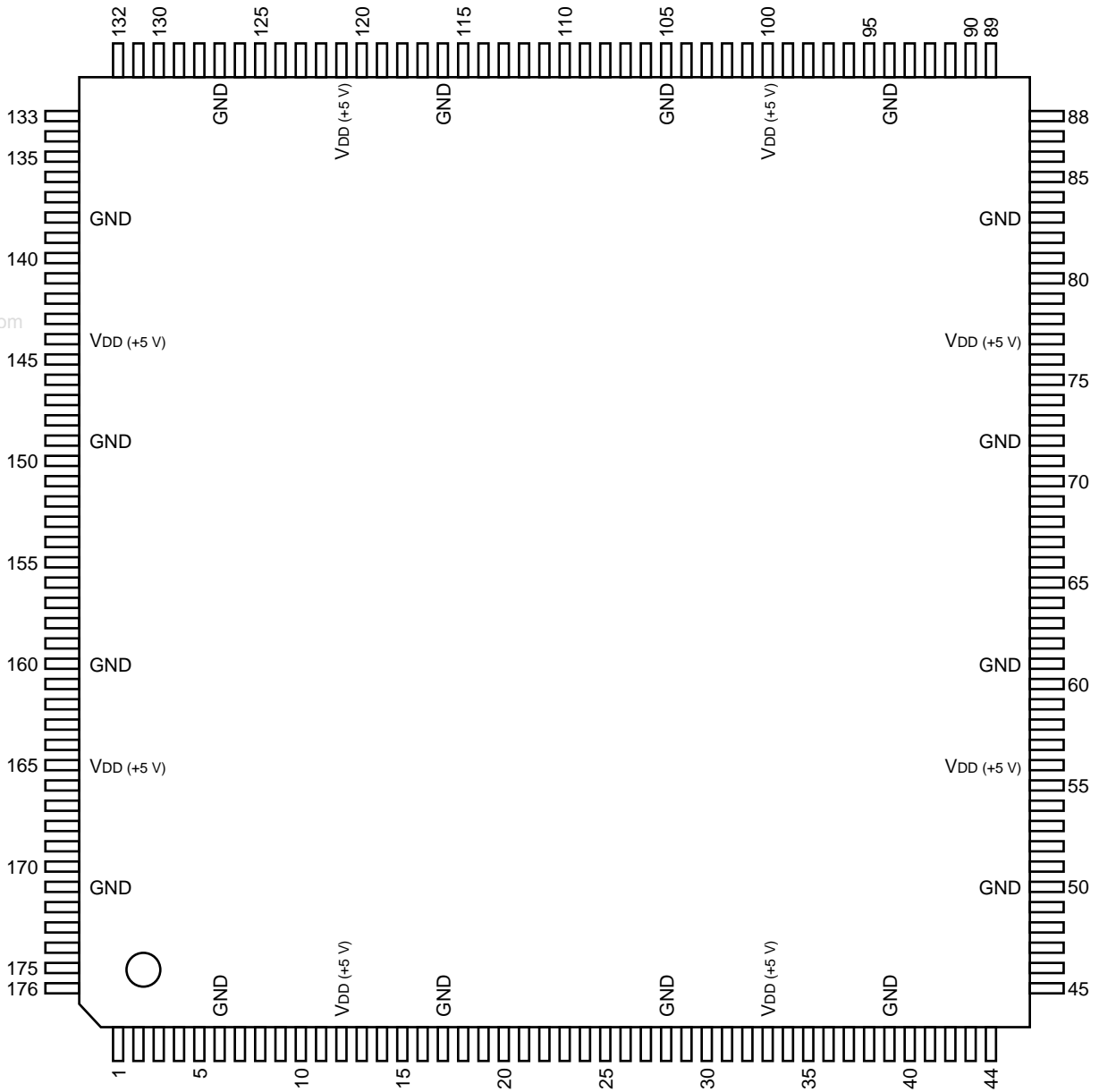

C-MOS A/V DATA REC PROCESS (GATE ARRAY) - TOP VIEW -



www.DataSheet4U.com

(VDD = +5 V)

PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	O	DIAG	45	O	GWDATA5	89	I	CADRS5	133	I	R_DAT5
2	I	AINT0	46	O	GWDATA6	90	I	CADRS6	134	I	R_DAT6
3	I	AINT1	47	O	GWDATA7	91	I	CADRS7	135	I	R_DAT7
4	I	PAY_EN	48	O	GWSYNC	92	I	CRD	136	I	I_PORT0
5	I	AINT2	49	O	GWSTART	93	I	CWR	137	I	I_PORT1
6	—	GND	50	—	GND	94	—	GND	138	—	GND
7	I	ADEN2	51	O	GWEND	95	I	CCS	139	O	TEST_R
8	I	SW_DET	52	O	WE_V	96	I/O	CDATA0	140	O	PINT_RE0
9	I	PCERD	53	O	WE_A	97	I/O	CDATA1	141	O	PINT_RE1
10	I	IN_FP	54	O	WE_T	98	I/O	CDATA2	142	O	PINT_RE2
11	O	RX_INIT	55	O	RSTW_V	99	I/O	CDATA3	143	O	PINT_RE3
12	—	VDD	56	—	VDD	100	—	VDD	144	—	VDD
13	O	DIAGRE	57	O	RSTW_A	101	I/O	CDATA4	145	O	PINT_RE4
14	O	DIAGRST	58	O	RSTW_T	102	I/O	CDATA5	146	O	PINT_RE5
15	O	ATRIWE	59	O	W_CKO	103	I/O	CDATA6	147	O	PINT_RE6
16	O	ATRIRSTW	60	I	W_CK	104	I/O	CDATA7	148	O	PINT_RE7
17	—	GND	61	—	GND	105	—	GND	149	—	GND
18	I	S_DAT0	62	I	GRDATA0	106	O	DMA_DAT0	150	O	W_DAT0
19	I	S_DAT1	63	I	GRDATA1	107	O	DMA_DAT1	151	O	W_DAT1
20	I	S_DAT2	64	I	GRDATA2	108	O	DMA_DAT2	152	O	W_DAT2
21	I	S_DAT3	65	I	GRDATA3	109	O	DMA_DAT3	153	O	W_DAT3
22	I	S_DAT4	66	I	GRDATA4	110	O	DMA_DAT4	154	O	W_DAT4
23	I	S_DAT5	67	I	GRDATA5	111	O	DMA_DAT5	155	O	W_DAT5
24	I	S_DAT6	68	I	GRDATA6	112	O	DMA_DAT6	156	O	W_DAT6
25	I	S_DAT7	69	I	GRDATA7	113	O	DMA_DAT7	157	O	W_DAT7
26	I	S_DAT8	70	I	GRSYNC	114	O	DFWE1	158	O	O_PORT0
27	I	S_DAT9	71	I	GRSTART	115	O	DFWE2	159	O	O_PORT1
28	—	GND	72	—	GND	116	—	GND	160	—	GND
29	O	WCCONT0	73	I	GREND	117	O	DFWE3	161	O	MAIN_RE
30	O	WCCONT1	74	O	RE_V	118	O	DFWE4	162	O	P_INIT
31	O	WCCONT2	75	O	RSTR_V	119	O	DFRSTW	163	O	M_RSTW
32	O	WCCONT3	76	I	XSM	120	I	DMA_DREQ	164	I	XACK
33	—	VDD	77	—	VDD	121	—	VDD	165	—	VDD
34	O	WCCONT4	78	I	XTST	122	O	RCCONT0	166	I	BCK
35	O	MAIN_WE	79	I	SDI	123	O	RCCONT1	167	I	XTCK
36	O	W_INIT	80	O	SDO	124	O	RCCONT2	168	O	TEST_W
37	O	M_RSTW	81	O	RE_A	125	O	RCCONT3	169	O	WCCONT5
38	O	H_REC	82	O	RSTR_A	126	O	RCCONT4	170	O	RCCONT5
39	—	GND	83	—	GND	127	—	GND	171	—	GND
40	O	GWDATA0	84	I	CADRS0	128	I	R_DAT0	172	O	EXT_CS0
41	O	GWDATA1	85	I	CADRS1	129	I	R_DAT1	173	O	EXT_CS1
42	O	GWDATA2	86	I	CADRS2	130	I	R_DAT2	174	I	R_CK
43	O	GWDATA3	87	I	CADRS3	131	I	R_DAT3	175	I	SG_FP
44	O	GWDATA4	88	I	CADRS4	132	I	R_DAT4	176	I	SYS_RST

INPUT

$\overline{\text{ADEN2}}, \overline{\text{PAY_EN}}$; DATA ENABLE (SDDI RX)
$\overline{\text{AINT0}}$; VIDEO/NON-AV INTERRUPT (SDDI RX)
$\overline{\text{AINT1}}$; AUDIO INTERRUPT (SDDI RX)
$\overline{\text{AINT2}}$; ATTRIBUTE INTERRUPT (SDDI RX)
BCK, XACK, XTCK	; IC TEST PIN
CADRS0 - CADRS7	; CPU ADDRESS BUS
CCS	; CPU CHIP SELECT
CRD	; CPU READ PULSE
CWR	; CPU WRITE PULSE
$\overline{\text{DMA_DREQ}}$; DMA FIFO WRITE REQUEST
GRDATA0 - GRDATA7	; GOP DELAY READ DATA IN
GREND	; GOP DELAY END PULSE
$\overline{\text{GRSTART}}$; GOP DELAY START PULSE
$\overline{\text{GRSYNC}}$; GOP DELAY SYNC
$\overline{\text{I_PORT0}}, \overline{\text{I_PORT1}}$; IN PORT
$\overline{\text{IN_FP}}, \overline{\text{SG_FP}}$; FRAME PULSE IN
$\overline{\text{PCERD}}$; PAYLOAD CRCC ERROR (SDDI RX)
R_CK	; READ PROCESS CLOCK
R_DATA0 - R_DAT7	; MAIN FIFO READ DATA IN
S_DATA0 - S_DAT10	; DATA IN (SDDI RX)
SDI, XSM, XTST	; IC TEST PIN
$\overline{\text{SW_DET}}$; SWITCHING DETECT (SDDI RX)
$\overline{\text{SYS_RST}}$; POWER ON RESET
W_CK	; WRITE PROCESS CLOCK

OUTPUT

<u>ATRIRSTW</u>	; ATTRIBUTE FIFO RSTW
<u>ATRIWE</u>	; ATTRIBUTE FIFO WRITE ENABLE
<u>DFRSTW</u>	; DMA FIFO RSTW
<u>DFWE1</u> - <u>DFWE4</u>	; DMA FIFO WRITE ENABLE
<u>DIAG</u>	; DIAG MODE SEL (H: DIAG MODE)
<u>DIAGRE</u>	; DIAG FIFO READ ENABLE
<u>DIAGRST</u>	; DIAG FIFO RSTR
<u>DMA_DAT0</u> - <u>DMA_DAT7</u>	; DMA FIFO WRITE DATA OUT
<u>EXT_CS0</u> , <u>EXT_CS1</u>	; CHIP SELECT OUT
<u>GWDATA0</u> - <u>GWDATA7</u>	; GOP DELAY WRITE DATA OUT
<u>GWEND</u>	; GOP DELAY END PULSE OUT
<u>GWSTART</u>	; GOP DELAY START PULSE OUT
<u>GWSYNC</u>	; GOP DELAY SYNC OUT
<u>H_REC</u>	; REC LED DRIVE (H: REC)
<u>M_RSTR</u>	; MAIN FIFO RSTR
<u>M_RSTW</u>	; MAIN FIFO RSTW
<u>MAIN_RE</u>	; MAIN FIFO READ ENABLE
<u>MAIN_WE</u>	; MAIN FIFO WRITE ENABLE
<u>O_PORT0</u> , <u>O_PORT1</u>	; OUT PORT
<u>P_INIT</u>	; MAIN FIFO POWER ON INITIAL PULSE
<u>PINT_RE0</u> - <u>PINT_RE7</u>	; MAIN FIFO POWER ON INITIAL CHIP SELECT
<u>RCCOUNT0</u> - <u>RCCOUNT5</u>	; MAIN FIFO READ CHIP COUNTER OUT
<u>RE_A</u>	; AUDIO FIFO READ ENABLE
<u>RE_V</u>	; VIDEO FIFO READ ENABLE
<u>RSTR_A</u>	; AUDIO FIFO RSTR
<u>RSTR_V</u>	; VIDEO FIFO RSTR
<u>RSTW_A</u>	; AUDIO FIFO RSTW
<u>RSTW_T</u>	; TIME CODE FIFO RSTW
<u>RSTW_V</u>	; VIDEO FIFO RSTW
<u>RX_INIT</u>	; CPU INTERRUPT
<u>SDO</u>	; IC TEST PIN
<u>TEST_R</u>	; IC TEST
<u>TEST_W</u>	; IC TEST
<u>W_CKO</u>	; WRITE PROCESS CLOCK OUT
<u>W_DAT0</u> - <u>W_DAT7</u>	; MAIN FIFO WRITE DATA OUT
<u>W_INIT</u>	; MAIN FIFO POWER ON INITIAL PULSE
<u>WCCOUNT0</u> - <u>WCCOUNT5</u>	; MAIN FIFO WRITE CHIP COUNTER OUT
<u>WE_A</u>	; AUDIO FIFO WRITE ENABLE
<u>WE_T</u>	; TIME CODE FIFO WRITE ENABLE
<u>WE_V</u>	; VIDEO FIFO WRITE ENABLE

INPUT/OUTPUT

<u>CDATA0</u> - <u>CDATA7</u>	; CPU DATA BUS 0 - 7
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