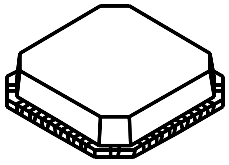
SONY

CXG1131ER

High Power 3 × 5 Antenna Switch MMIC with Integrated Control Logic

24 pin VQFN (Plastic)



Description

The CXG1131ER is a high power antenna switch MMIC for PDC full packet 1.5GHz handsets. This IC is suited to connect Tx/Rx/duplexer to one of 4 antennas. The CXG1131ER has on-chip logic circuit for operation with 4 CMOS inputs. The Sony's GaAs J-FET process is used for low insertion loss and low voltage operation.

Features

- Low insertion loss: 1.0dB @1.5GHz
- High linearity: Harmonic < – 65dBc
- CMOS compatible input control
- Small package: 24-pin VQFN (4.0mm × 4.0mm)

Applications

3 × 5 antenna switch for digital cellular such as PDC handsets

Structure

GaAs J-FET MMIC

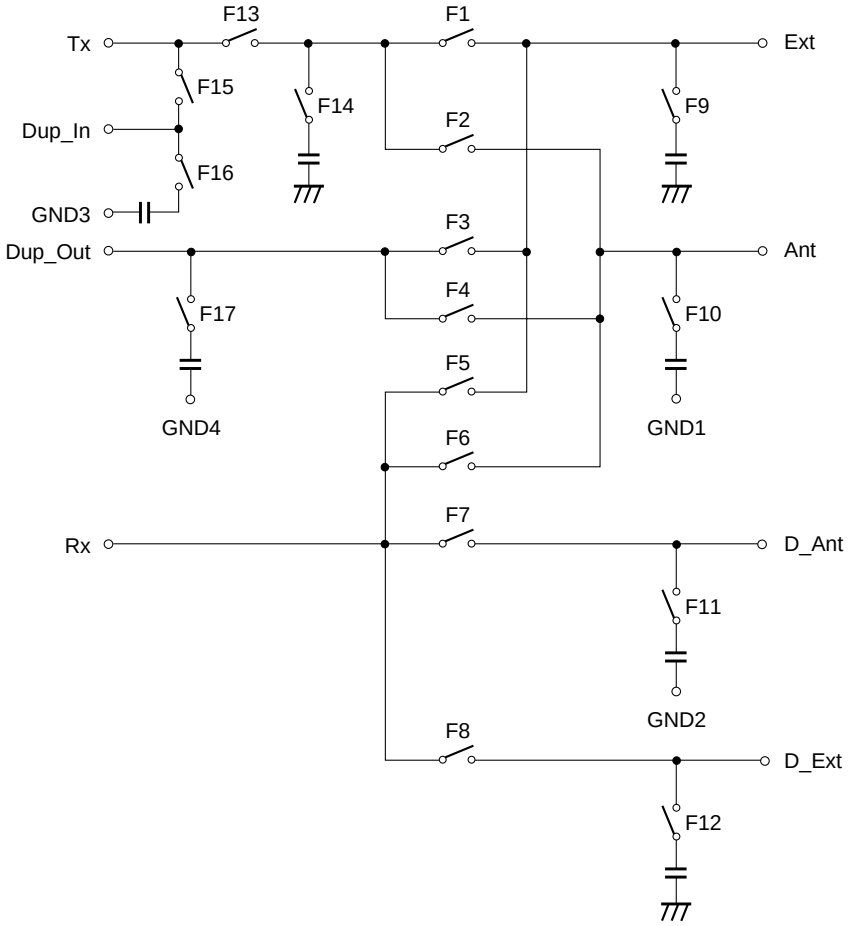
Absolute Maximum Ratings (Ta = 25°C)

• Bias voltage	V_{DD}	7	V
• Control voltage	Vctl	5	V
• Operating temperature	Topr	–35 to +85	°C
• Storage temperature	Tstg	–65 to +150	°C

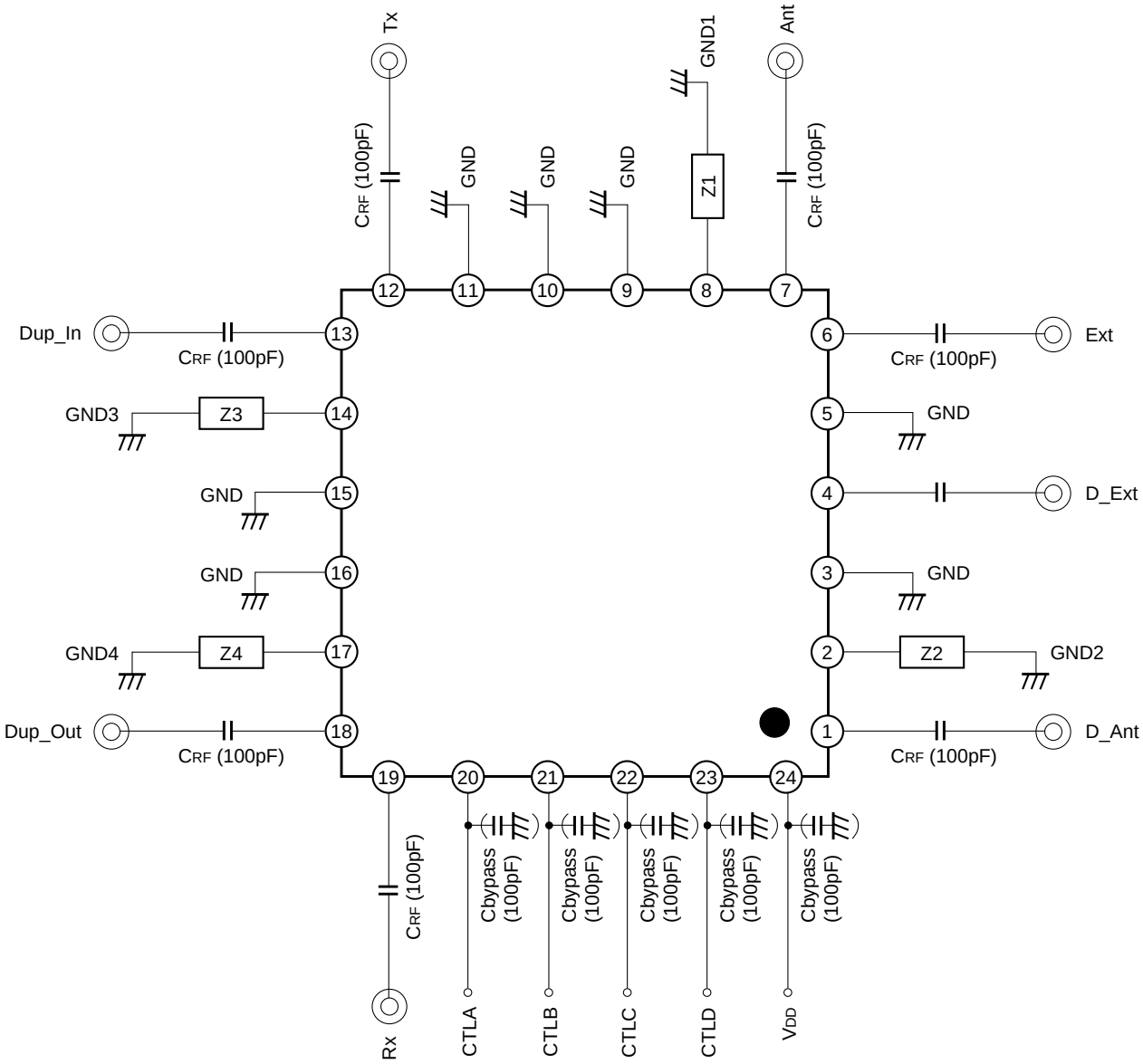
GaAs MMICs are ESD sensitive devices. Special handling precautions are required.

E02110-PS

Block Diagram



Pin Configuration/Recommended Circuit



When using this IC, the following external components should be used:

C_{RF}: This capacitor is used for RF de-coupling and must be used for all applications. 100pF is recommended.

Cbypass: This capacitor is used for DC line filtering. 100pF is recommended.

Z1 to Z4: It is recommended that these pins be directly grounded.

Truth Table

A: Rx/Tx
B: Main/diversity
C: External/antenna
D: TDMA/28.8k

State	On Pass	A	B	C	D	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10	F11	F12	F13	F14	F15	F16	F17
1	Tx – Ext	H	—	L	L	H	L	L	L	L	L	L	L	L	H	H	H	H	L	L	H	H
2	Tx – Ant	H	—	H	L	L	H	L	L	L	L	L	L	H	L	H	H	H	L	L	H	H
3	Rx – Ext	L	L	L	L	L	L	L	L	H	L	L	L	L	H	H	H	L	H	L	H	H
4	Rx – Ant	L	L	H	L	L	L	L	L	L	H	L	L	H	L	H	H	L	H	L	H	H
5	Rx – D_Ext	L	H	L	L	L	L	L	L	L	L	L	H	H	H	H	L	L	H	L	H	H
6	Rx – D_Ant	L	H	H	L	L	L	L	L	L	L	H	L	H	H	L	H	L	H	L	H	H
7	Dup_Out – Ant Rx – Ant	—	L	H	H	L	L	L	H	L	H	L	L	H	L	H	H	L	H	H	L	L
8	Dup_Out – Ant Rx – D_Ant	—	H	H	H	L	L	L	H	L	L	H	L	H	L	L	H	L	H	H	L	L
9	Dup_Out – Ext Rx – Ext	—	L	L	H	L	L	H	L	H	L	L	L	L	H	H	H	L	H	H	L	L
10	Dup_Out – Ext Rx – D_Ext	—	H	L	H	L	L	H	L	L	L	L	H	L	H	H	L	L	H	H	L	L

DC Bias Condition (Ta = 25°C)

Item	Min.	Typ.	Max.	Unit
V_{DD}	2.7	3.0	3.3	V
Vctl (H)	2.0	3.0	3.6	V
Vctl (L)	0		0.4	V

Electrical Characteristics (Ta = 25°C)

Item	Symbol	Port	Condition	Min.	Typ.	Max.	Unit
Insertion loss	IL	Tx – Ext	*1	—	1.0	1.3	dB
		Tx – Ant	*1	—	1.0	1.3	dB
		Tx – Dup_In	*1	—	0.35	0.65	dB
		Rx – Ext	*2	—	0.85	1.15	dB
		Rx – Ant	*2	—	0.85	1.15	dB
		Rx – D_Ext	*2	—	0.7	1.0	dB
		Rx – D_Ant	*2	—	0.7	1.0	dB
		Dup_Out – Ext	*1, *4	—	1.2	1.5	dB
		Rx – Ext	*2, *5	—	1.2	1.5	dB
		Dup_Out – Ant	*1, *4	—	1.3	1.6	dB
		Rx – Ant	*2, *5	—	1.3	1.6	dB
		Dup_Out – Ext	*1, *4	—	0.75	1.05	dB
		Rx – D_Ext	*2, *5	—	0.75	1.05	dB
		Dup_Out – Ant	*1, *4	—	0.75	1.05	dB
		Rx – D_Ant	*2, *5	—	0.75	1.05	dB
Isolation	ISO.	Tx – Ext	*1	30	33	—	dB
		Tx – Ant	*1	30	33	—	dB
		Tx – Dup_In	*1	26	29	—	dB
		Rx – Ext	*2	35	38	—	dB
		Rx – Ant	*2	35	38	—	dB
		Rx – D_Ext	*2	30	33	—	dB
		Rx – D_Ant	*2	27	30	—	dB
		Dup_Out – Ext	*1, *4	30	33	—	dB
		Rx – Ext	*2, *5	35	38	—	dB
		Dup_Out – Ant	*1, *4	27	30	—	dB
		Rx – Ant	*2, *5	35	38	—	dB
		Dup_Out – Ext	*1, *4	30	33	—	dB
		Rx – D_Ext	*2, *5	30	33	—	dB
		Dup_Out – Ant	*1, *4	30	33	—	dB
		Rx – D_Ant	*2, *5	27	30	—	dB
		Tx – Rx (Full packet)	*1	47	50	—	dB
		Tx – Rx (TDMA)	*1	14	17	—	dB

Item	Symbol	Port	Condition	Min.	Typ.	Max.	Unit
Harmonics	2fo	Tx – Ext	*3	—	–75	–60	dBc
		Tx – Ant	*3	—	–75	–60	dBc
		Tx – Dup_In	*3	—	–80	–60	dBc
		Dup_Out – Ext	*3, *4	—	–75	–60	dBc
		Dup_Out – Ant	*3, *4	—	–75	–60	dBc
	3fo	Tx – Ext	*3	—	–67	–60	dBc
		Tx – Ant	*3	—	–67	–60	dBc
		Tx – Dup_In	*3	—	–75	–60	dBc
		Dup_Out – Ext	*3, *4	—	–67	–60	dBc
		Dup_Out – Ant	*3, *4	—	–67	–60	dBc
ACP	±50kHz	Tx – Ext	*3	—	–65	–57	dBc
		Tx – Ant	*3	—	–65	–57	dBc
		Tx – Dup_In	*3	—	–65	–57	dBc
		Dup_Out – Ext	*3, *4	—	–65	–57	dBc
		Dup_Out – Ant	*3, *4	—	–65	–57	dBc
	±100kHz	Tx – Ext	*3	—	–73	–65	dBc
		Tx – Ant	*3	—	–73	–65	dBc
		Tx – Dup_In	*3	—	–73	–65	dBc
		Dup_Out – Ext	*3, *4	—	–73	–65	dBc
		Dup_Out – Ant	*3, *4	—	–73	–65	dBc
P1dB	P1dB	Tx – Ext	V_{DD} = 3V	33	34	—	dBm
		Tx – Ant	V_{DD} = 3V	33	34	—	dBm
		Tx – Dup_In	V_{DD} = 3V	33	34	—	dBm
		Dup_Out – Ext	V_{DD} = 3V	33	34	—	dBm
		Dup_Out – Ant	V_{DD} = 3V	33	34	—	dBm
Switching speed	TSW	—		—	2	—	µs
Bias current	I_{DD}	—	V_{DD} = 3V	—	350	500	µA
Control current	Ictl	—	Vctl (H) = 3V	—	35	75	µA

*1 Pin = 29.5dBm, 0/3V control, V_{DD} = 2.8V to 3.6V, 1,429MHz to 1,453MHz

*2 Pin = 10dBm, 0/3V control, V_{DD} = 2.8V to 3.6V, 1,477MHz to 1,501MHz

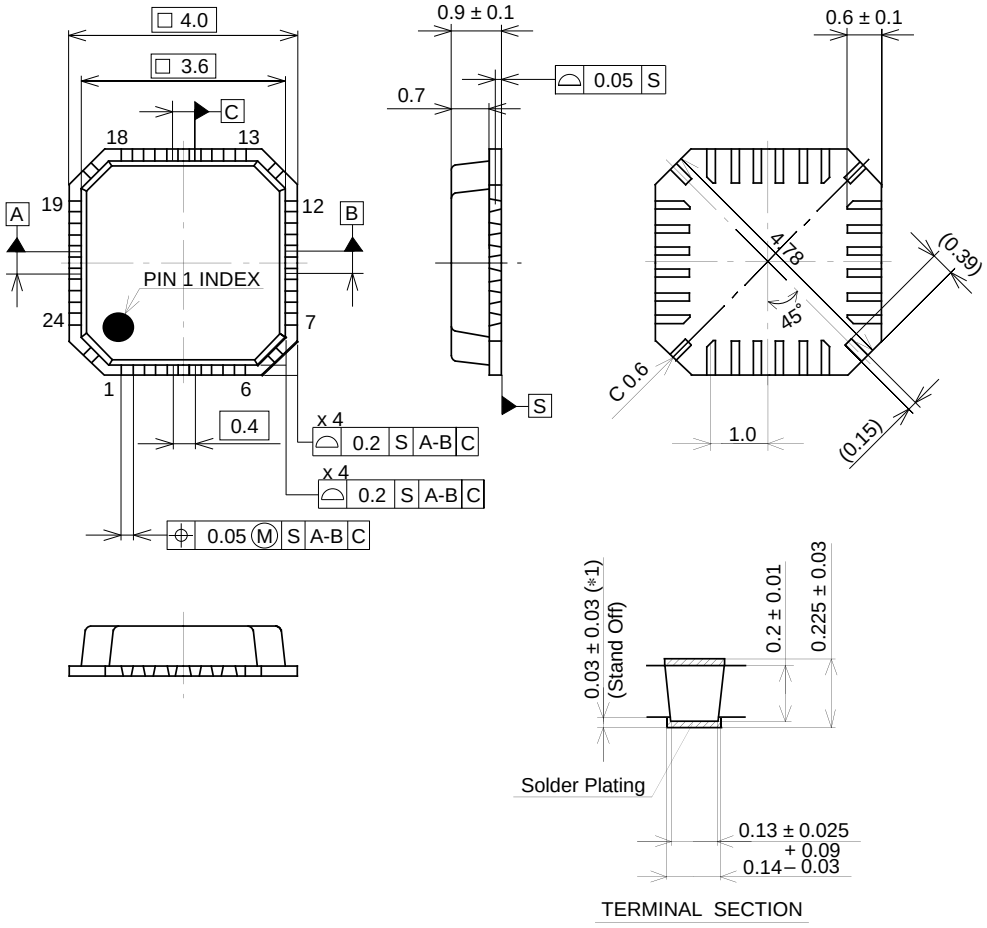
*3 π/4-shifted DQPSK, Pin = 29.5dBm, 0/3V control, V_{DD} = 3.0V, 1,429MHz to 1,453MHz,
ACP (±50kHz) < – 70dBc, ACP (±100kHz) < – 75dBc, 2nd harmonics < – 75dBc, 3rd harmonics < – 75dBc

*4 Rx is open.

*5 Dup_Out is open.

Package Outline Unit: mm

24PIN VQFN(PLASTIC)



SONY CODE	VQFN-24P-03
EIAJ CODE	————
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.04g

LEAD PLATING SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	COPPER ALLOY
SOLDER COMPOSITION	Sn-Bi Bi:1-4wt%
PLATING THICKNESS	5-18µm