

Power Amplifier Module for JCDMA

Description

The CXG1156K is the power amplifier module which operates at a single power supply. This IC is designed using the Sony's original p-Gate HFET process.

Features

- Single power supply operation:
 $V_{DD1} = V_{DD2} = 3.5V$ (High power mode),
 $1.3V$ (Low power mode 1),
 $1.0V$ (Low power mode 2),
 $V_{GG} = 2.7V$
- Small package: 0.065cc (6.2mm × 6.2mm × 1.7mm)
- High efficiency: $\eta_{add} = 40\%$ @ $P_{OUT} = 27.5dBm$ (High power mode),
 $\eta_{add} = 23\%$ @ $P_{OUT} = 15dBm$ (Low power mode 1)
- Output power (high/low power mode switching supported):
 $P_{OUT} = 18$ to 27.5dBm: High power mode,
 $P_{OUT} = 15$ to 18dBm: Low power mode 1,
 $P_{OUT} \leq 15dBm$: Low power mode 2
- Gain: $G_p = 29dB$ (@900MHz)

Applications

Power amplifier for JCDMA system cellular phones

Structure

p-Gate HFET module

Absolute Maximum Ratings (Ta = 25°C)

• Operating case temperature	Tcase	−30 to +90	°C
• Storage temperature	Tstg	−30 to +125	°C
• Bias voltage	VDD1, VDD2	6	V
• Bias voltage	VGG	3.3	V
		(@VDD1 = VDD2 = 3.5V)	
• Input power	PIN	8	dBm

Recommended Operating Conditions*

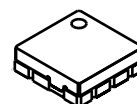
- $V_{DD1} = V_{DD2} = 3.2$ to 4.2V@ $P_{OUT} = 18$ to 27.5dBm,
 1.3 to 2.0V@ $P_{OUT} \leq 18dBm$,
 1.0 to 2.0V@ $P_{OUT} \leq 15dBm$
- $V_{GG} = 2.7V \pm 1\%$

*This recommended operating voltage is the value that specified the supply voltage range where the functional operation was confirmed by the Sony's recommended evaluation board.

GaAs module is ESD sensitive devices. Special handling precautions are required.

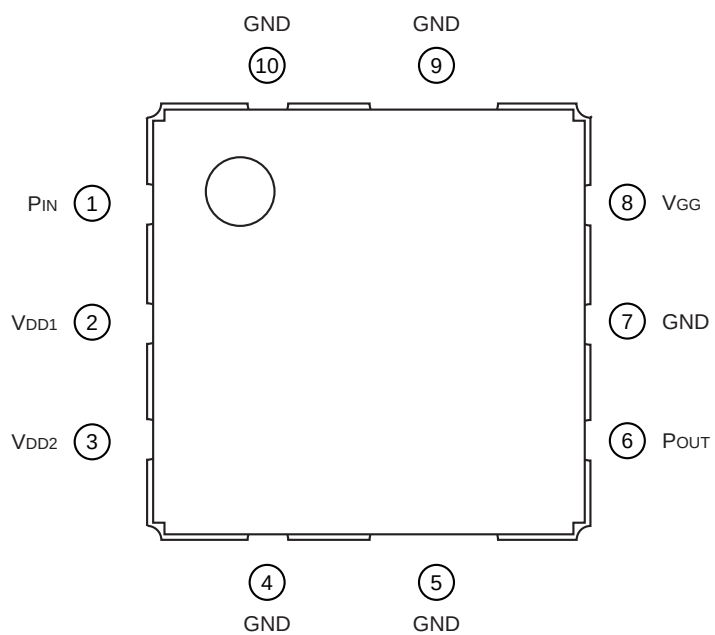
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10 pin LCC (Ceramic)

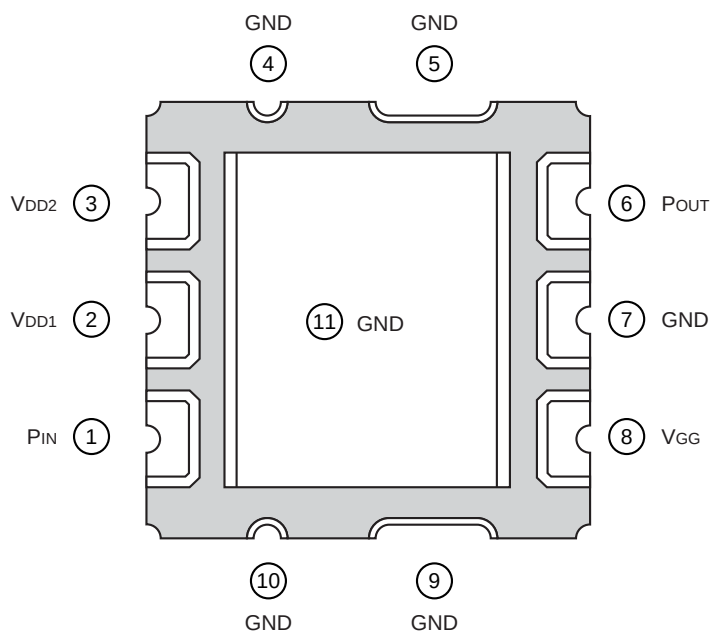


Package Outline/Pin Configuration

Front



Back



Note) Be sure to solder the GND part (11) to the land.

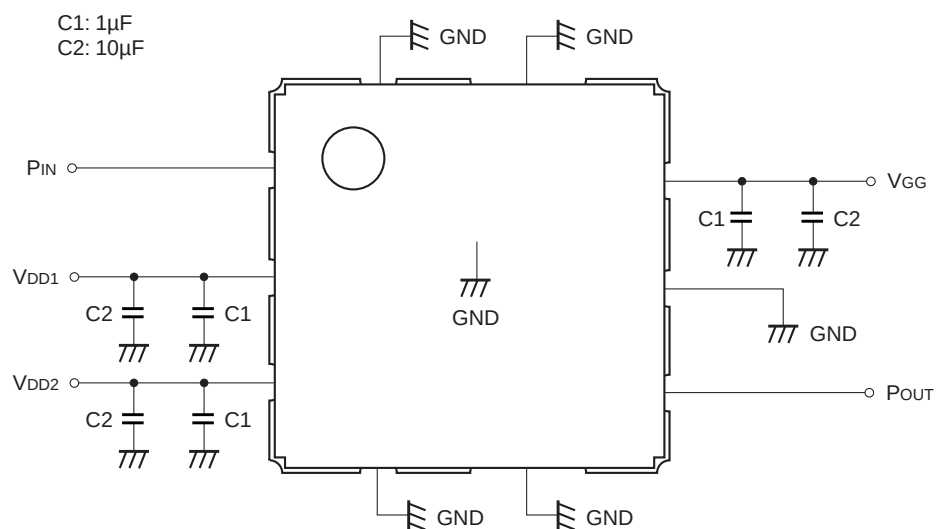
For the land where the GND part (11) is connected, form the GND pattern by making the through holes in the land.

Electrical Characteristics

(ZS = ZL = 50Ω, IS-95 Modulation, Tc = 25°C)

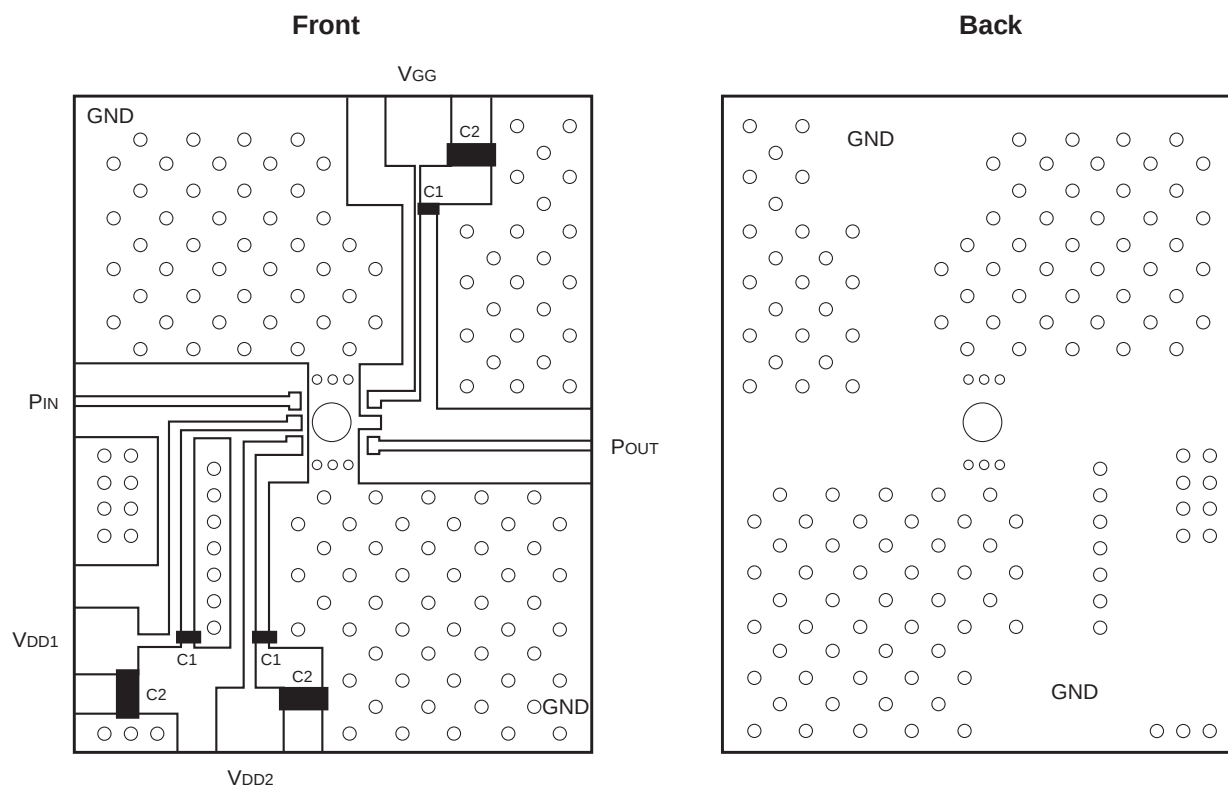
Item	Conditions	Min.	Typ.	Max.	Unit
Frequency		887		925	MHz
Current consumption 1	P _{OUT} = 27.5dBm, V _{DD} = 3.5V, V _{GG} = 2.7V		405	420	mA
Current consumption 2	P _{OUT} = 15dBm, V _{DD} = 1.3V, V _{GG} = 2.7V		105	110	mA
Current consumption 3	P _{OUT} = 12dBm, V _{DD} = 1.0V, V _{GG} = 2.7V		79	90	mA
Gain 1	P _{OUT} = 27.5dBm, V _{DD} = 3.5V, V _{GG} = 2.7V	25	29		dB
Gain 2	P _{OUT} = 18dBm, V _{DD} = 1.3V, V _{GG} = 2.7V	22	24		dB
Gain 3	P _{OUT} = 15dBm, V _{DD} = 1.0V, V _{GG} = 2.7V	20	22		dB
ACPR1 (High power mode)	P _{OUT} = 27.5dBm, V _{DD} = 3.5V, V _{GG} = 2.7V, ±900kHz offset, 30kHz band width		−54	−47	dBc
ACPR2 (High power mode)	P _{OUT} = 27.5dBm, V _{DD} = 3.5V, V _{GG} = 2.7V, ±1.98MHz offset, 30kHz band width		−64	−58	dBc
ACPR1 (Low power mode 1)	P _{OUT} = 18dBm, V _{DD} = 1.3V, V _{GG} = 2.7V, ±900kHz offset, 30kHz band width		−56	−50	dBc
ACPR2 (Low power mode 1)	P _{OUT} = 18dBm, V _{DD} = 1.3V, V _{GG} = 2.7V, ±1.98MHz offset, 30kHz band width		−63	−58	dBc
ACPR1 (Low power mode 2)	P _{OUT} = 15dBm, V _{DD} = 1.0V, V _{GG} = 2.7V, ±900kHz offset, 30kHz band width		−56	−50	dBc
ACPR2 (Low power mode 2)	P _{OUT} = 15dBm, V _{DD} = 1.0V, V _{GG} = 2.7V, ±1.98MHz offset, 30kHz band width		−63	−58	dBc
2nd, 3rd harmonics	P _{OUT} = 27.5dBm, V _{DD} = 3.5V, V _{GG} = 2.7V		−27	−23	dBc
Input VSWR	V _{DD} = 3.5V, V _{GG} = 2.7V		1.3	2	
Gate current	V _{GG} = 2.7V, P _{OUT} ≤ 27.5dBm		1.7	2.5	mA

Recommended External Circuit



Recommended Evaluation Board

Board material: Glass fabric-base epoxy
Size: 40mm $\times$ 50mm $\times$ 0.6mm
Relative dielectric constant: 4.6



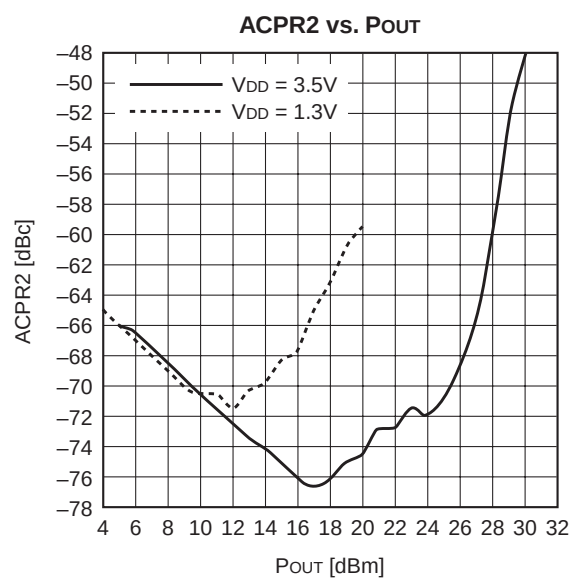
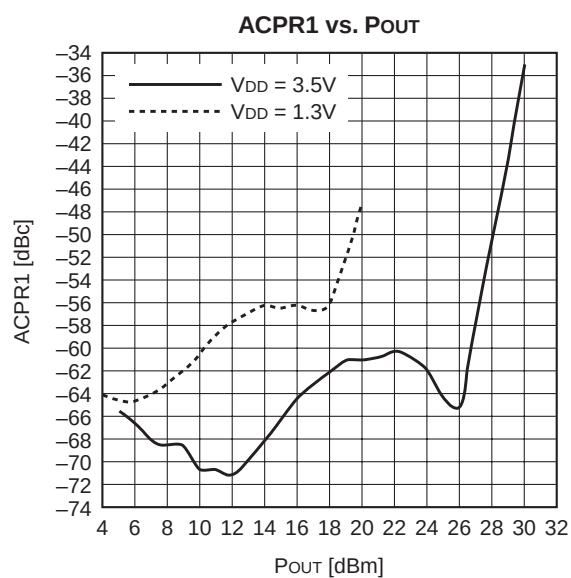
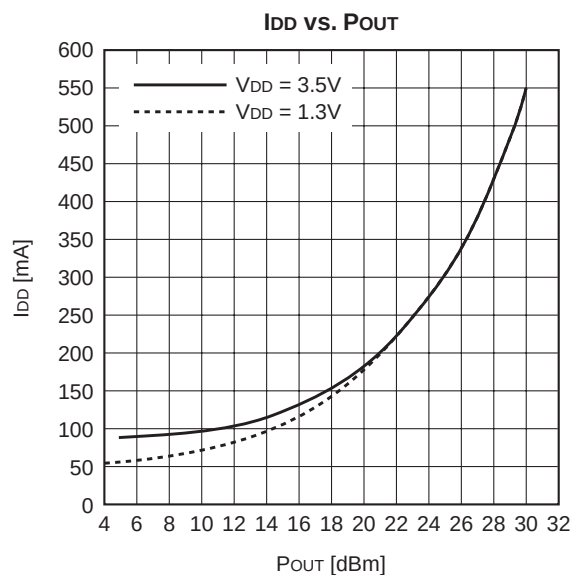
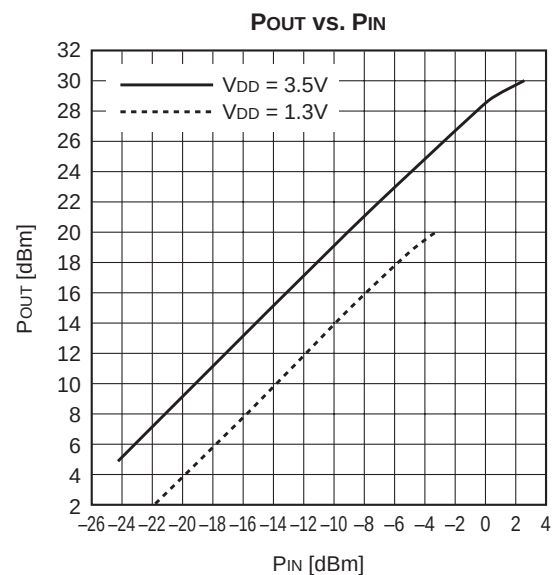
Example of Representative Characteristics

Conditions: $f = 900\text{MHz}$

$V_{DD1} = V_{DD2} = 3.5\text{V}$, $V_{GG} = 2.7\text{V}$ (High power mode)

$V_{DD1} = V_{DD2} = 1.3\text{V}$, $V_{GG} = 2.7\text{V}$ (Low power mode 1)

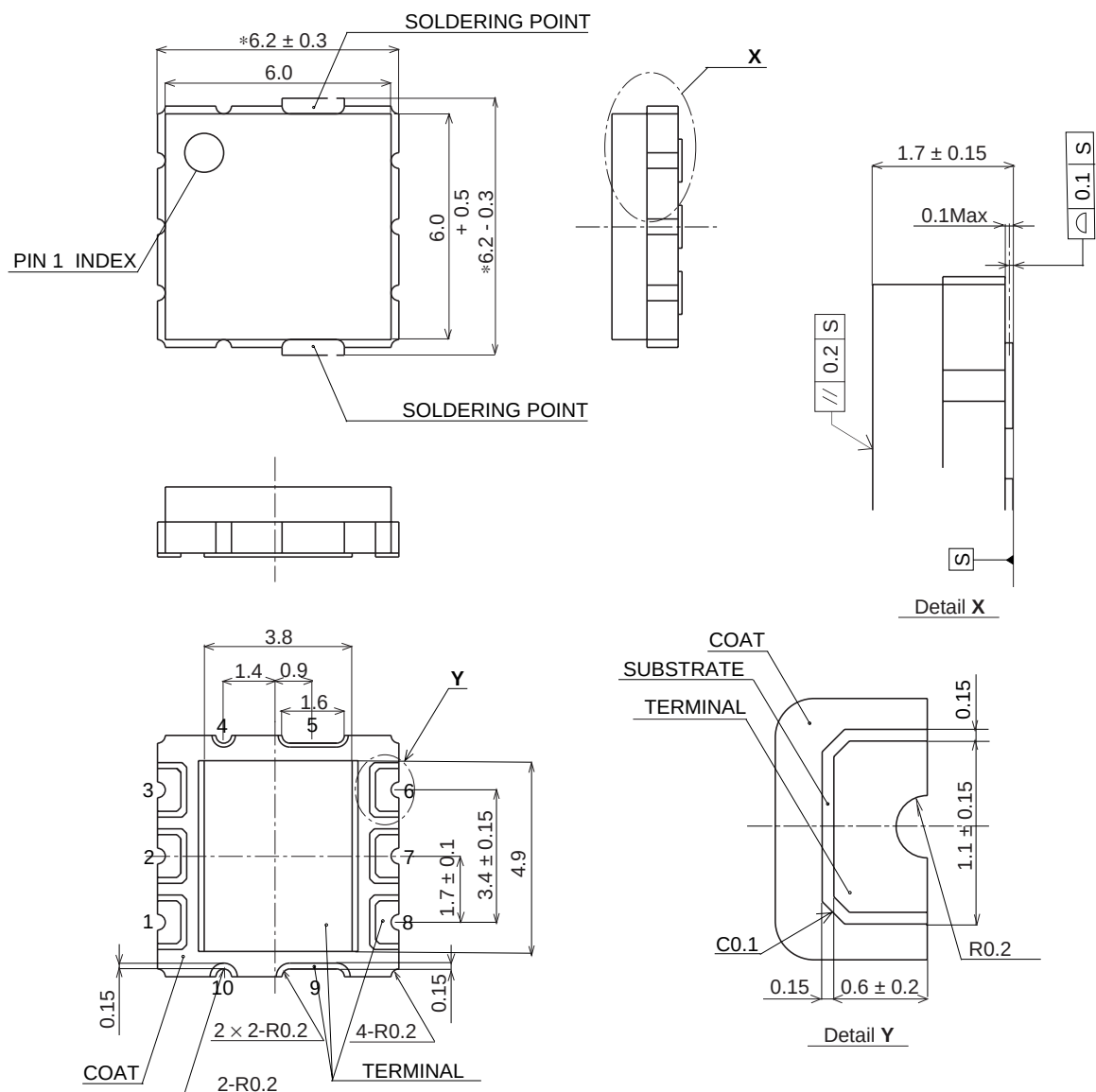
$T_a = 25^\circ\text{C}$



Package Outline

Unit: mm

10PIN LCC



NOTE: Dimension "*" does not include cutting burr.

SONY CODE	LCC-10C-03
JEITA CODE	—
JEDEC CODE	—

PACKAGE STRUCTURE

PACKAGE MATERIAL	CERAMIC SUBSTRATE
TERMINAL TREATMENT	GOLD PLATING
TERMINAL MATERIAL	NICKEL PLATING
PACKAGE MASS	0.8g