SONY

High Power DPDT Switch with Logic Control

Preliminary

CXG1175UR

Description

This IC can be used in wireless communication systems, for example, W-CDMA handsets.
The IC has on-chip logic for operation with 2 CMOS control inputs.
The Sony JPHEMT process is used for low insertion loss and on-chip logic circuit.
(Applications: Antenna switch for cellular handsets, Dual-band W-CDMA)

Features

- ◆ Low insertion loss
- ◆ 2 CMOS compatible control line

Package

Small package size: 20-pin UQFN

Structure

GaAs JPHEMT MMIC

Absolute Maximum Ratings

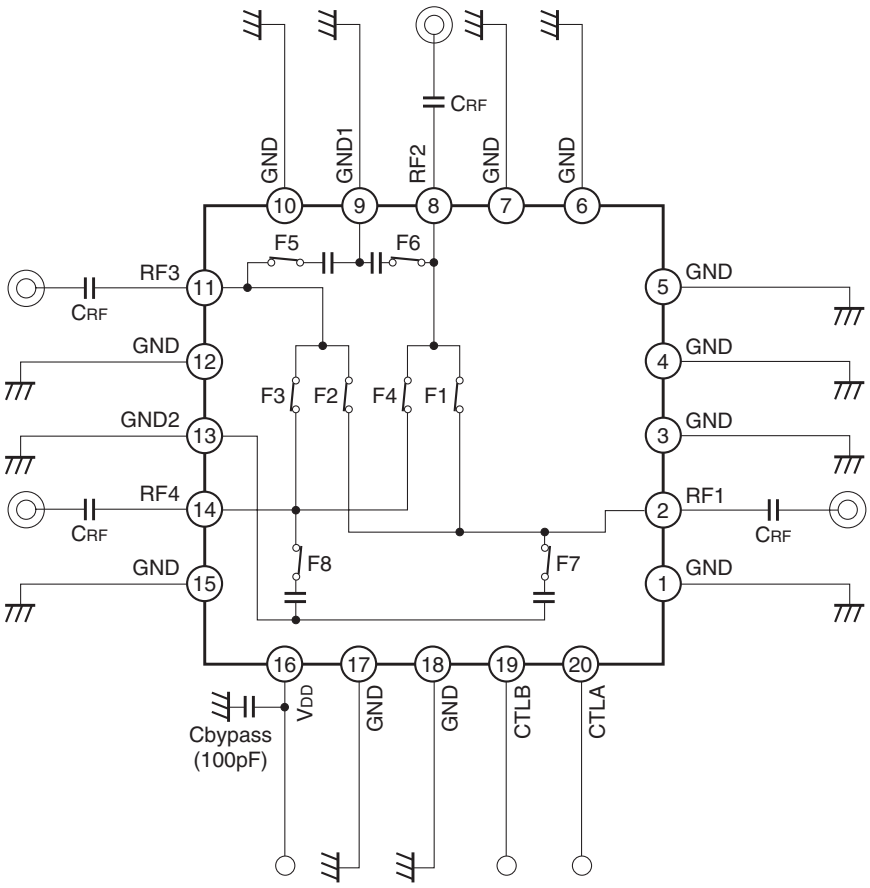
(Ta = 25℃)

◆ Bias voltage	V_{DD}	7	V
◆ Control voltage	Vctl	5	V
◆ Operating temperature	Topr	–35 to +85	℃
◆ Storage temperature	Tstg	–60 to +150	℃

This IC is ESD sensitive device. Special handling precautions are required.

RE05327-PS

Block Diagram and Recommended Circuit



When using this IC, the following external components should be used:

C_{RF}: This capacitor is used for RF decoupling and must be used for all applications.

Cbypass: This capacitor is used for DC line filtering.

Truth Table

State	CTLA	CTLB	ON state	F1	F2	F3	F4	F5	F6	F7	F8
1	H	L	RF1 – RF2	ON	OFF	OFF	OFF	ON	OFF	OFF	ON
2	L	L	RF1 – RF3	OFF	ON	OFF	OFF	OFF	ON	OFF	ON
3	H	H	RF4 – RF2	OFF	OFF	OFF	ON	ON	OFF	ON	OFF
4	L	H	RF4 – RF3	OFF	OFF	ON	OFF	OFF	ON	ON	OFF

DC Bias Conditions

(Ta = 25℃)

Item	Min.	Typ.	Max.	Unit
Vctl (H)	2.2	2.85	3.2	V
Vctl (L)	0	—	0.4	V
V_{DD}	2.6	2.85	3.2	V

Electrical Characteristics

(Ta = 25℃)

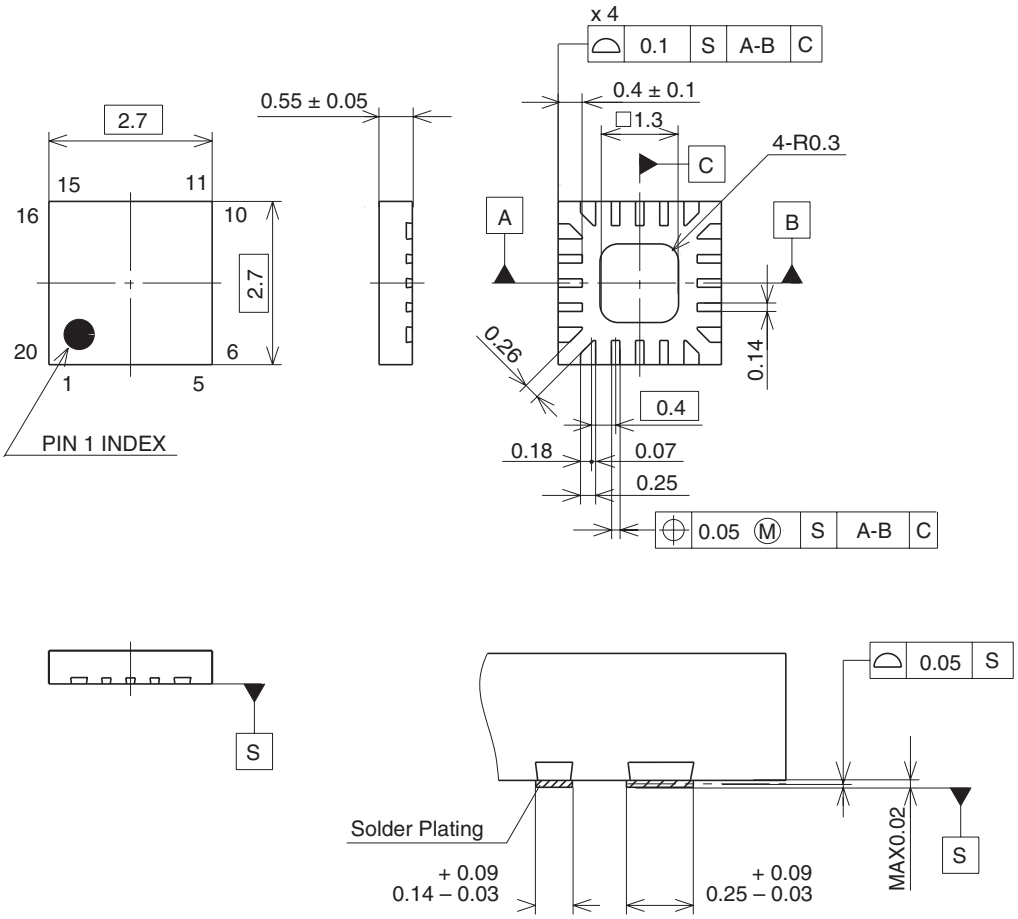
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Insertion loss	IL	830 to 890MHz		0.35	0.60	dB
		1920 to 1980MHz		0.45	0.75	dB
		2110 to 2170MHz		0.50	0.80	dB
Isolation	ISO.	830 to 890MHz	25	30		dB
		1920 to 2170MHz	20	25		dB
VSWR	VSWR	50Ω		1.2		—
Switching speed	TSW			4	10	μs
1dB compression input power	P1dB	V_{DD} = 2.85V		32		dBm
ACLR	ACLR1	±5MHz, 3.84MHz BW *1		–60	–50	dBc
	ACLR2	±10MHz, 3.84MHz BW *1		–65	–55	dBc
Harmonics	2fo	*1		–80	–65	dBc
	3fo	*1		–80	–65	dBc
Bias current	I_{DD}	V_{DD} = 2.85V		120	220	μA
Control current	Ictl	Vctl (H) = 2.85V		15	35	μA

*1 Pin = 25dBm, 0/2.85V control, V_{DD} = 2.85V, 830 to 840MHz, 1920 to 1980MHz

Package Outline

(Unit: mm)

20PIN UQFN (PLASTIC)



TERMINAL SECTION

Note:Cutting burr of lead are 0.05mm MAX.

SONY CODE	UQFN-20P-01
EIAJ CODE	————
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.02g

LEAD PLATING SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	COPPER ALLOY
SOLDER COMPOSITION	Sn-Bi Bi:1-4wt%
PLATING THICKNESS	5-18µm