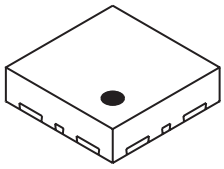
SONY

CXG1176UR

High Power DPDT Switch with Logic Control

12 pin UQFN (Plastic)



Description

This IC can be used in wireless communication systems, for example, W-CDMA handsets.

The IC has on-chip logic for operation with 2 CMOS control inputs.

The Sony JPHEMT process is used for low insertion loss and on-chip logic circuit.

Features

- Low insertion loss
- 2 CMOS compatible control line
- Small package size: 12-pin UQFN

Applications

- Antenna switch for cellular handsets
- Dual-Band W-CDMA

Structure

GaAs JPHEMT MMIC

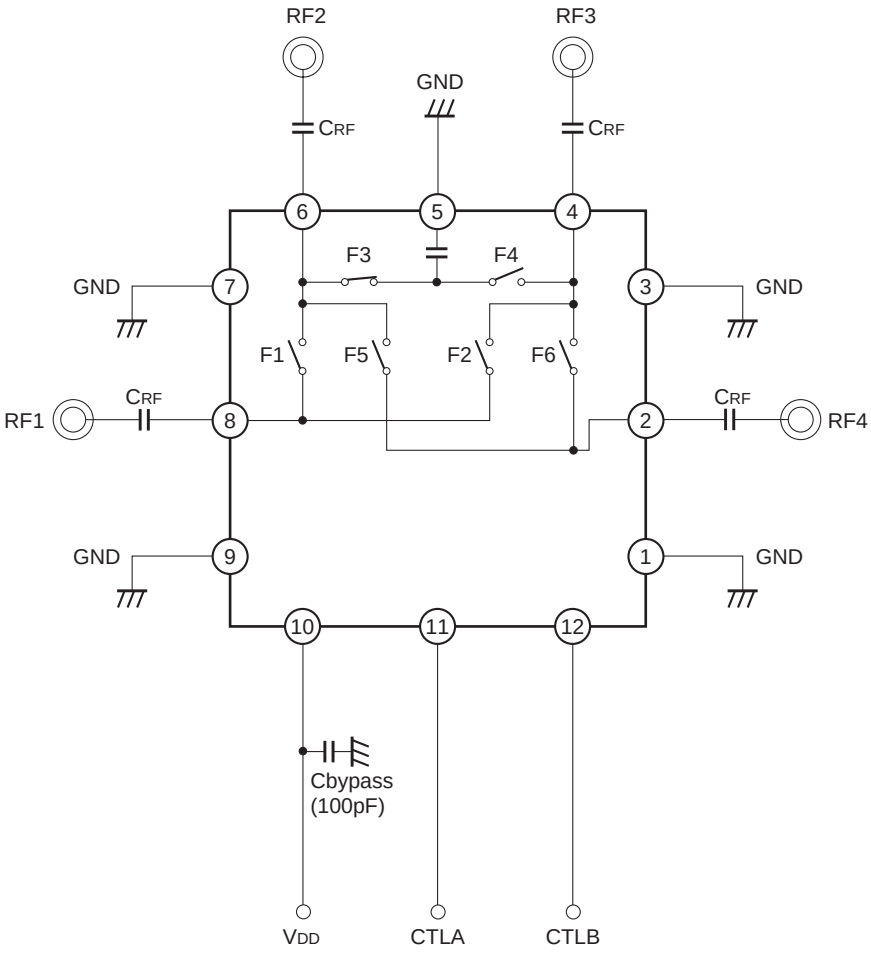
Absolute Maximum Ratings (Ta = 25°C)

• Bias voltage	V_{DD}	7	V
• Control voltage	Vctl	5	V
• Operating temperature	Topr	–35 to +85	°C
• Storage temperature	Tstg	–65 to +150	°C

GaAs MMICs are ESD sensitive devices. Special handling precautions are required.

E04910-PS

Block Diagram and Recommended Circuit



When using this IC, the following external components should be used:

C_{RF}: This capacitor is used for RF decoupling and must be used for all applications.

Cbypass: This capacitor is used for DC line filtering. 100pF is recommended.

Truth Table

State	CTLA	CTLB	ON State	F1	F2	F3	F4	F5	F6
1	L	L	RF4 – RF3	OFF	OFF	ON	OFF	OFF	ON
2	L	H	RF4 – RF2	OFF	OFF	OFF	ON	ON	OFF
3	H	L	RF1 – RF3	OFF	ON	ON	OFF	OFF	OFF
4	H	H	RF1 – RF2	ON	OFF	OFF	ON	OFF	OFF

DC Bias Conditions (Ta = 25°C)

Item	Min.	Typ.	Max.	Unit
Vctl (H)	2.0	2.85	3.6	V
Vctl (L)	0	—	0.4	V
V_{DD}	2.5	2.85	3.6	V

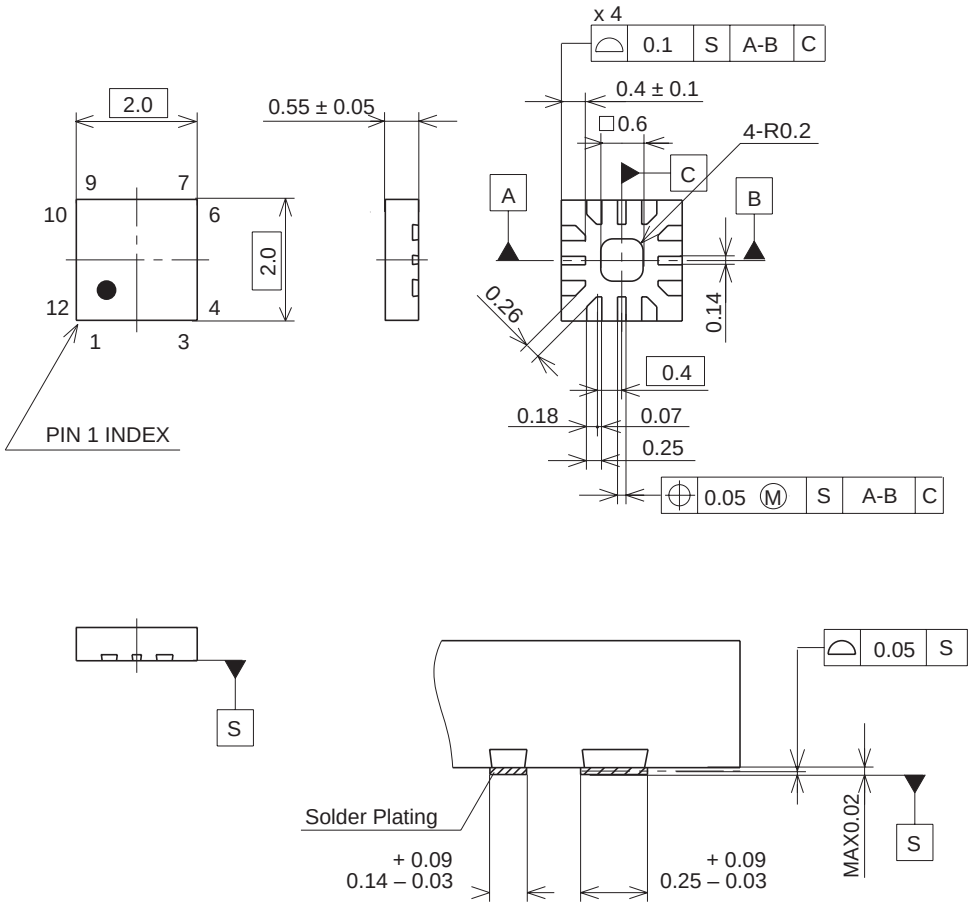
Electrical Characteristics (Ta = 25°C)

Item	Symbol	State	Condition	Min.	Typ.	Max.	Unit
Insertion loss	IL		830 to 885MHz		0.25	0.45	dB
			1920 to 2170MHz		0.35	0.55	dB
Isolation	ISO.		830 to 885MHz	20	25		dB
			1920 to 2170MHz	15	20		dB
VSWR	VSWR		50Ω		1.2	1.5	—
Switching speed	TSW				5	10	µs
ACLR	ACLR1	±5MHz	*1		–60	–50	dBc
	ACLR2	±10MHz	*1		–65	–55	dBc
Harmonics	2fo		*1		–75	–60	dBc
	3fo		*1		–75	–60	dBc
Bias current	I_{DD}		V_{DD} = 2.85V		80	150	µA
Control current	Ictl		Vctl (H) = 2.85V		15	25	µA

*1 Pin = 25dBm, 0/2.85V control, V_{DD} = 2.85V, 830 to 840MHz, 1920 to 1980MHz
Measurement system noise level: ACLR (±5MHz) < –60dBc, (±10MHz) < –65dBc, 2nd Harmonics < –90dBc, 3rd Harmonics < –90dBc

Package Outline Unit: mm

12PIN UQFN (PLASTIC)



TERMINAL SECTION

Note:Cutting burr of lead are 0.05mm MAX.

SONY CODE	UQFN-12P-01
EIAJ CODE	————
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.01g

LEAD PLATING SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	COPPER ALLOY
SOLDER COMPOSITION	Sn-Bi Bi:1-4wt%
PLATING THICKNESS	5-18µm