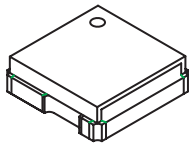
SONY

# CXG1178K

## Power Amplifier Module for JCDMA

8 pin LCC (Ceramic)



### Description

The CXG1178K is the power amplifier module which operates at a single power supply. This IC is designed using the Sony's original p-Gate HFET process.

### Features

- Single power supply operation:
  $V_{DD1}$ = $V_{DD2}$ = 3.5V (High mode),
  1.5V (Mid mode),
  1.0V (Low mode),
  $V_{GG}$ = 2.8V
- Ultrasmall package: 0.027cc (4.5mm × 4.5mm × 1.35mm)
- High efficiency: ηadd = 40.5%@$P_{OUT}$ = 27.5dBm (High mode),
  ηadd = 17.6%@$P_{OUT}$ = 14dBm (Mid mode)
- Output power (High/Mid/Low mode switching supported):
  $P_{OUT}$ = 18 to 27.5dBm: High mode,
  $P_{OUT}$ = 14 to 18dBm: Mid mode,
  $P_{OUT}$ ≤ 14dBm: Low mode
- Gain (High mode): Gp = 28.5dB (@900MHz)

### Applications

Power amplifier for JCDMA system cellular phones

### Structure

p-Gate HFET module

### Absolute Maximum Ratings (Ta = 25°C)

| | | | |
|---|---|---|---|
| • Operating case temperature | Tcase | –30 to +110 | °C |
| • Storage temperature | Tstg | –30 to +125 | °C |
| • Bias voltage | $V_{DD1}$, $V_{DD2}$ | 6 | V |
| • Bias voltage | $V_{GG}$ | 3.3 | V |
| | | (@$V_{DD1}$ = $V_{DD2}$ ≤ 3.5V) | |
| • Input power | $P_{IN}$ | 8 | dBm |

### Recommended Bias Voltage Conditions

- $V_{DD1}$ = $V_{DD2}$ = 1.0 to 4.2V
- $V_{GG}$ = 2.8V ± 1%

Descriptions in this specification are specified for the Sony's recommended evaluation board .
GaAs module is ESD sensitive devices. Special handling precautions are required.

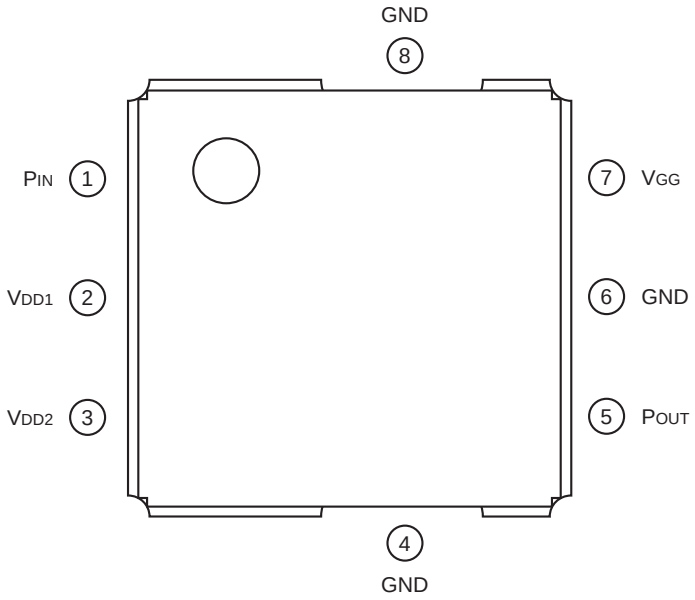




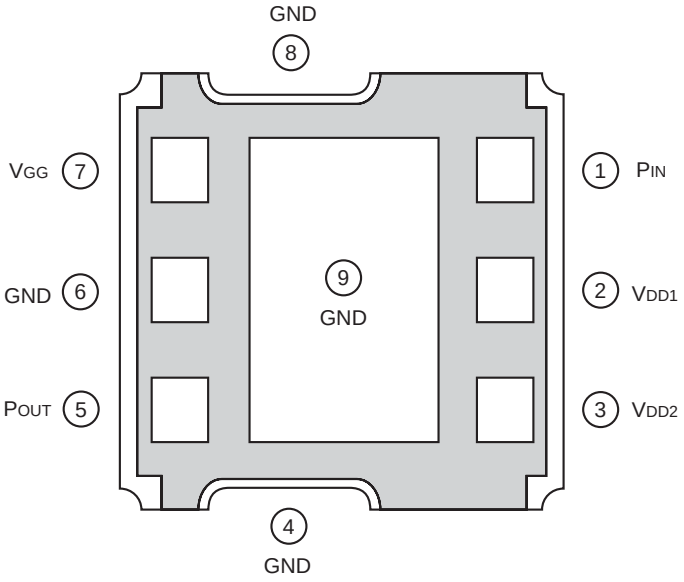
E04660-PS

## Package Outline/Pin Configuration

### Front




### Back

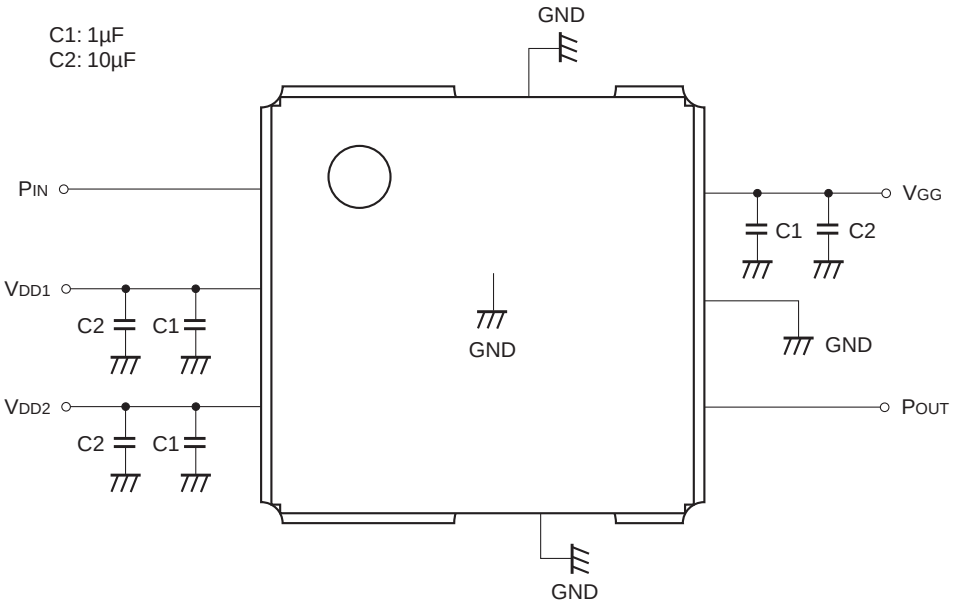



**Note)** Pin 4, 8 and 9 should be soldered on the land of the board.
For the land to which Pin 9 is connected, make the through holes in the land and form the GND pattern.

**Electrical Characteristics** (ZS = ZL = 50Ω, IS-95 Modulation, Ta = 25°C)

| Item | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Frequency | | 887 | | 925 | MHz |
| Current consumption 1 | $P_{OUT}$ = 27.5dBm, $V_{DD1}$ = $V_{DD2}$ = 3.5V, $V_{GG}$ = 2.8V | | 397 | 412 | mA |
| Current consumption 2 | $P_{OUT}$ = 14dBm, $V_{DD1}$ = $V_{DD2}$ = 1.5V, $V_{GG}$ = 2.8V | | 95 | 102 | mA |
| Current consumption 3 | $P_{OUT}$ = 9dBm, $V_{DD1}$ = $V_{DD2}$ = 1.0V, $V_{GG}$ = 2.8V | | 59 | 66 | mA |
| Gain 1 | $P_{OUT}$ = 27.5dBm, $V_{DD1}$ = $V_{DD2}$ = 3.5V, $V_{GG}$ = 2.8V | 26.5 | 28.5 | | dB |
| Gain 2 | $P_{OUT}$ = 18dBm, $V_{DD1}$ = $V_{DD2}$ = 1.5V, $V_{GG}$ = 2.8V | 20.5 | 22.5 | | dB |
| Gain 3 | $P_{OUT}$ = 14dBm, $V_{DD1}$ = $V_{DD2}$ = 1.0V, $V_{GG}$ = 2.8V | 17.5 | 19.5 | | dB |
| ACPR1 (High mode) | $P_{OUT}$ = 27.5dBm, $V_{DD1}$ = $V_{DD2}$ = 3.5V, $V_{GG}$ = 2.8V, ±900kHz offset, 30kHz band width | | –52 | –47 | dBc |
| ACPR2 (High mode) | $P_{OUT}$ = 27.5dBm, $V_{DD1}$ = $V_{DD2}$ = 3.5V, $V_{GG}$ = 2.8V, ±1.98MHz offset, 30kHz band width | | –62 | –57 | dBc |
| ACPR1 (Mid mode) | $P_{OUT}$ = 18dBm, $V_{DD1}$ = $V_{DD2}$ = 1.5V, $V_{GG}$ = 2.8V, ±900kHz offset, 30kHz band width | | –55 | –47 | dBc |
| ACPR2 (Mid mode) | $P_{OUT}$ = 18dBm, $V_{DD1}$ = $V_{DD2}$ = 1.5V, $V_{GG}$ = 2.8V, ±1.98MHz offset, 30kHz band width | | –62 | –57 | dBc |
| ACPR1 (Low mode) | $P_{OUT}$ = 14dBm, $V_{DD1}$ = $V_{DD2}$ = 1.0V, $V_{GG}$ = 2.8V, ±900kHz offset, 30kHz band width | | –54 | –47 | dBc |
| ACPR2 (Low mode) | $P_{OUT}$ = 14dBm, $V_{DD1}$ = $V_{DD2}$ = 1.0V, $V_{GG}$ = 2.8V, ±1.98MHz offset, 30kHz band width | | –63 | –57 | dBc |
| 2nd harmonics | $P_{OUT}$ = 27.5dBm, $V_{DD1}$ = $V_{DD2}$ = 3.5V, $V_{GG}$ = 2.8V | | –41 | –30 | dBc |
| 3rd harmonics | $P_{OUT}$ = 27.5dBm, $V_{DD1}$ = $V_{DD2}$ = 3.5V, $V_{GG}$ = 2.8V | | –57 | –30 | dBc |
| Gate current | $P_{OUT}$ ≤ 27.5dBm, $V_{GG}$ = 2.8V | | 1.8 | 2.5 | mA |
| Idle current 1 | $P_{IN}$, $P_{OUT}$ = None, $V_{DD1}$ = $V_{DD2}$ = 3.5V, $V_{GG}$ = 2.8V | | 85 | 110 | mA |
| Idle current 2 | $P_{IN}$, $P_{OUT}$ = None, $V_{DD1}$ = $V_{DD2}$ = 1.5V, $V_{GG}$ = 2.8V | | 51 | 66 | mA |
| Idle current 3 | $P_{IN}$, $P_{OUT}$ = None, $V_{DD1}$ = $V_{DD2}$ = 1.0V, $V_{GG}$ = 2.8V | | 40 | 52 | mA |

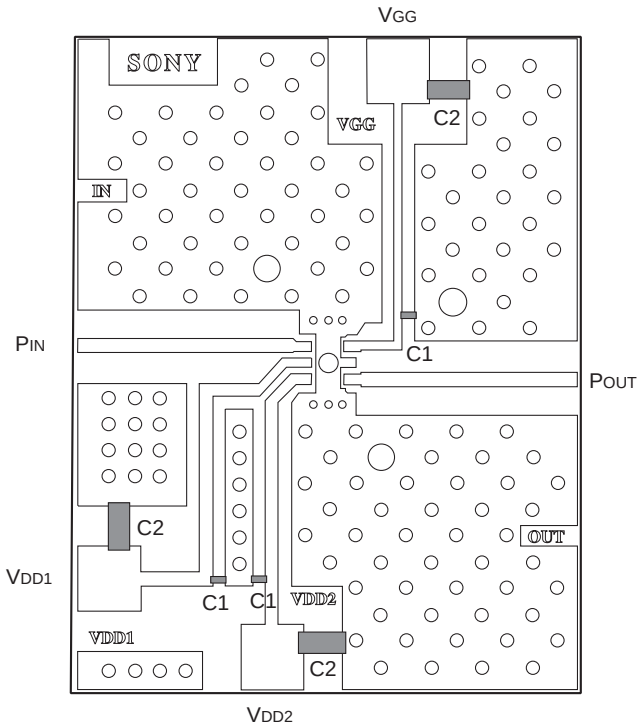
## Recommended External Circuit



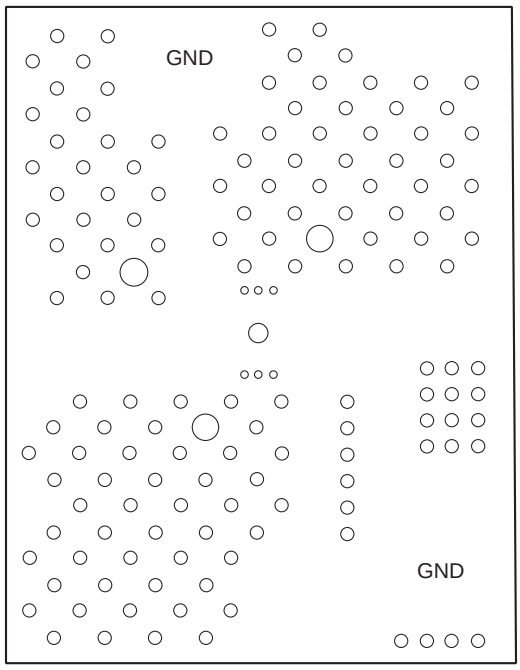

## Recommended Evaluation Board

Board material: Glass fabric-base epoxy
Size: 40mm × 50mm × 0.6mm
Relative dielectric constant: 4.6

**Front**




**Back**



**Example of Representative Characteristics**

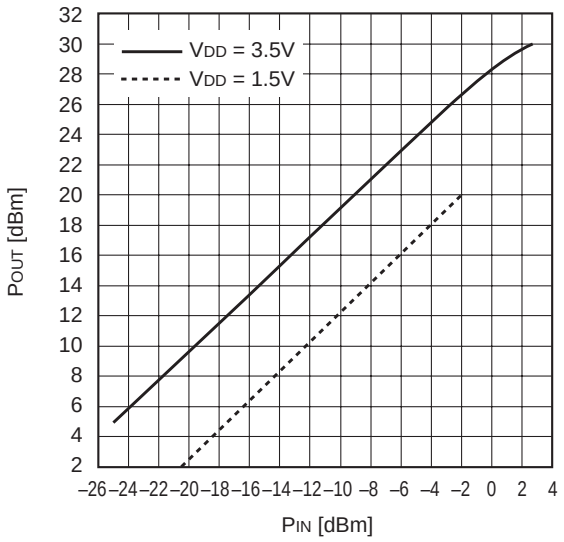
Conditions: f = 900MHz

$V_{DD1} = V_{DD2} = 3.5V$, $V_{GG} = 2.8V$ (High mode)

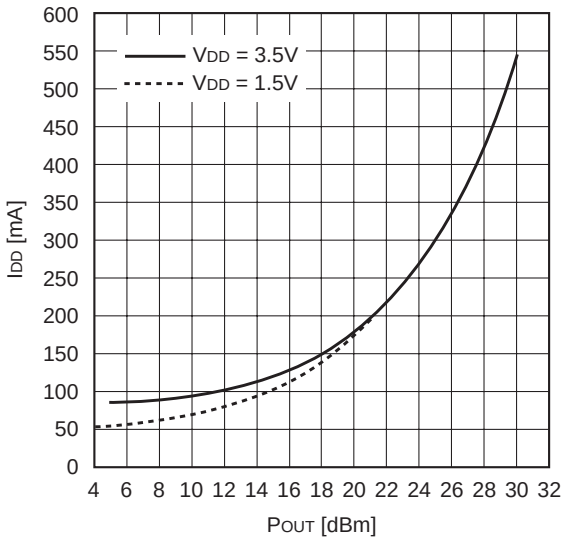
$V_{DD1} = V_{DD2} = 1.5V$, $V_{GG} = 2.8V$ (Mid mode)

Ta = 25°C

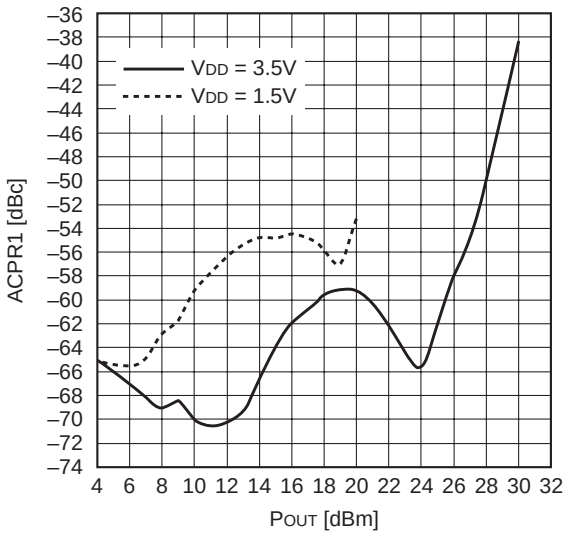
**POUT vs. PIN**



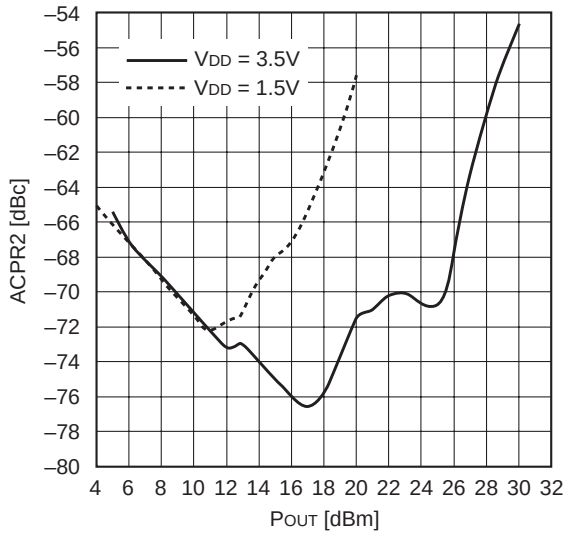

**IDD vs. POUT**




**ACPR1 vs. POUT**

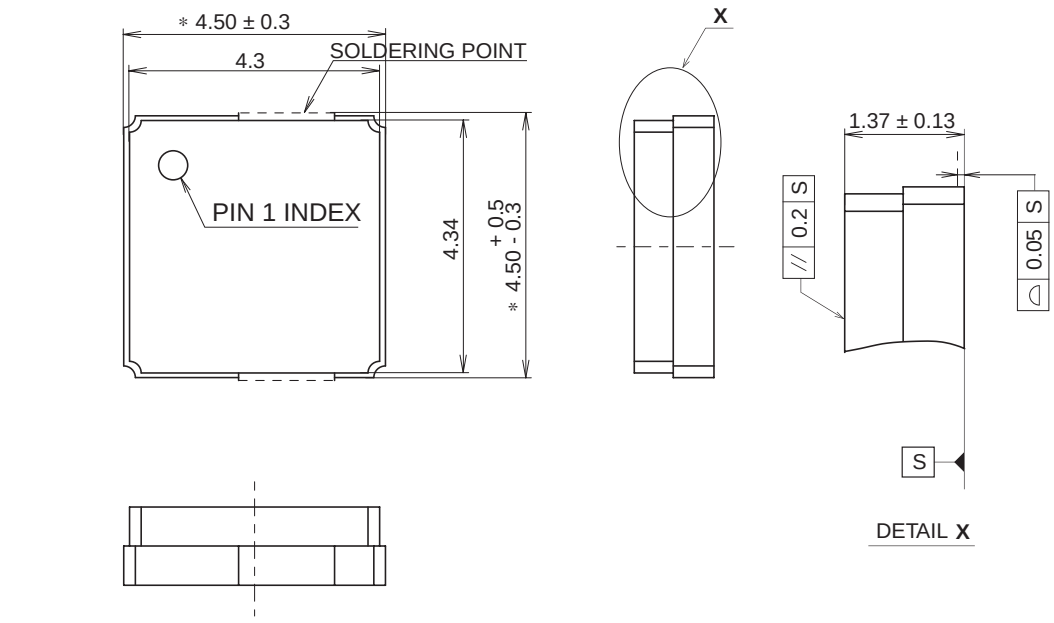


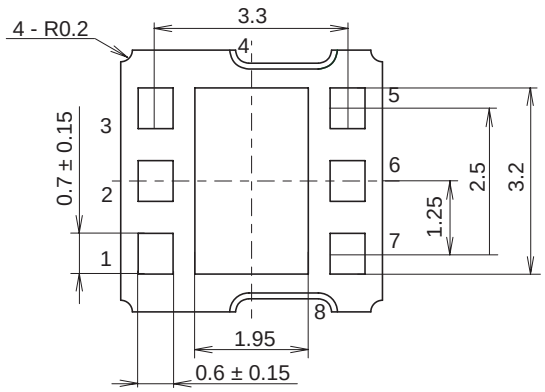

**ACPR2 vs. POUT**



**Package Outline** Unit: mm

8PIN LCC




NOTE: Dimension "∗" does not include cutting burr.

| | |
|---|---|
| SONY CODE | LCC-8C-371 |
| EIAJ CODE | ———— |
| JEDEC CODE | ———— |

PACKAGE STRUCTURE

| | |
|---|---|
| PACKAGE MATERIAL | CERAMIC SUBSTRATE |
| TERMINAL TREATMENT | GOLD PLATING |
| TERMINAL MATERIAL | NICKEL PLATING |
| PACKAGE MASS | 0.08g |