SONY

High Power 3P3T Switch with Logic Control

CXG1210UR

Description

This IC can be used in wireless communication systems, for example, CDMA EV-DO handsets.
The IC has on-chip logic for operation with 3 CMOS control inputs.
The Sony JPHEMT process is used for low insertion loss and on-chip logic circuit.
(Applications: Antenna switch for cellular handsets, CDMA, EVDO)

Features

- ◆ Low insertion loss: 0.3dB@900MHz
- ◆ 3 CMOS compatible control line

Package

Small package size: 20-pin UQFN

Structure

GaAs JPHEMT MMIC

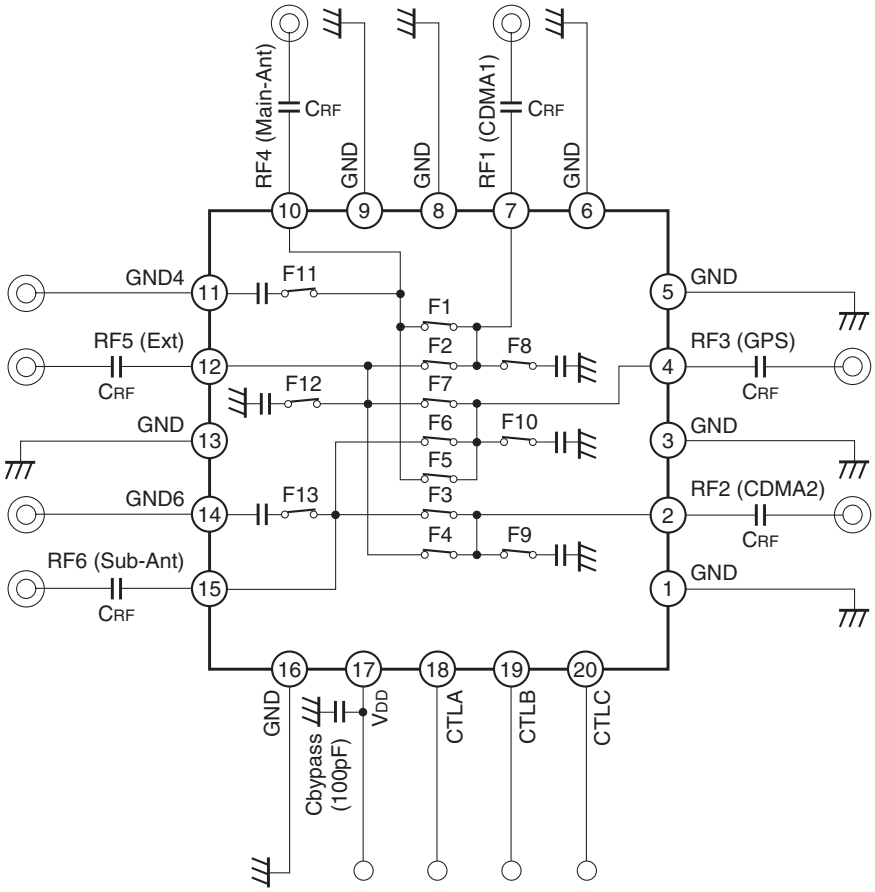
Absolute Maximum Ratings

(Ta = 25℃)

◆ Bias voltage	V_{DD}	7	V
◆ Control voltage	Vctl	5	V
◆ Operating temperature	Topr	–35 to +85	℃
◆ Storage temperature	Tstg	–60 to +150	℃
◆ RF input power	Pin = 37dBm		

This IC is ESD sensitive device. Special handling precautions are required.

Block Diagram and Recommended Circuit



When using this IC, the following external components should be used:

CRF: This capacitor is used for RF decoupling and must be used for all applications.

Cbypass: This capacitor is used for DC line filtering.

Truth Table

State	CTLA	CTLB	CTLC	Mode	ON state	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10	F11	F12	F13
1	L	L	L	CDMA1 Ext	RF1 – RF5	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON	ON	OFF	ON
2	L	L	H	CDMA1 Ext CDMA2 Sub	RF1 – RF5 RF2 – RF6	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON	OFF	OFF
3	H	L	L	CDMA1 Main	RF1 – RF4	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON	OFF	ON	ON
4	H	L	H	CDMA1 Main CDMA2 Sub	RF1 – RF4 RF2 – RF6	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	ON	OFF
5	L	H	L	GPS Ext	RF3 – RF5	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON	ON	OFF	ON	OFF	ON
6	L	H	H	CDMA2 Ext	RF2 – RF5	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF	ON	ON	OFF	ON
7	H	H	L	GPS Main	RF3 – RF4	OFF	OFF	OFF	OFF	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON
8	H	H	H	GPS Sub	RF3 – RF6	OFF	OFF	OFF	OFF	OFF	ON	OFF	ON	ON	OFF	ON	ON	OFF

DC Bias Conditions

(Ta = 25℃)

Item	Min.	Typ.	Max.	Unit
Vctl (H)	2.0	2.85	3.2	V
Vctl (L)	0	—	0.5	V
V_{DD}	2.6	2.85	3.2	V

Pin Description

Pin No.	Symbol	Pin No.	Symbol
1	GND	11	GND4
2	RF2 (CDMA2)	12	RF5 (EXT)
3	GND	13	GND
4	RF3 (GPS)	14	GND6
5	GND	15	RF6 (Sub-Ant)
6	GND	16	GND
7	RF1 (CDMA1)	17	V_{DD}
8	GND	18	CTLA
9	GND	19	CTLB
10	RF4 (Main-Ant)	20	CTLC

Electrical Characteristics

(Ta = 25°C, V_{DD} = 2.85V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Insertion loss	IL	900MHz		0.30	0.55	dB
		1.5GHz		0.40	0.65	dB
		1.9GHz		0.50	0.75	dB
Isolation	ISO.	900MHz	18	30		dB
		1.5GHz	15	30		dB
		1.9GHz	12	25		dB
VSWR	VSWR	50Ω		1.2		—
Harmonics	2fo	*1		–75	–60	dBc
		*3		–75	–60	dBc
	3fo	*1		–75	–60	dBc
		*3		–75	–60	dBc
Input IP3	IIP3	*2	55	65		dBm
		*4	55	65		dBm
1dB compression input power	P1dB	V_{DD} = 2.85V		32		dBm
Switching speed	TSW			4	10	μs
Bias current	I_{DD}	V_{DD} = 2.85V		300	420	μA
Control current	Ictl	Vctl (H) = 2.85V		15	30	μA

*1 Pin = 25dBm, 0/2.85V control, V_{DD} = 2.85V, 900MHz

*2 Pin = 25dBm (900MHz) + 25dBm (901MHz), 0/2.85V control, V_{DD} = 2.85V

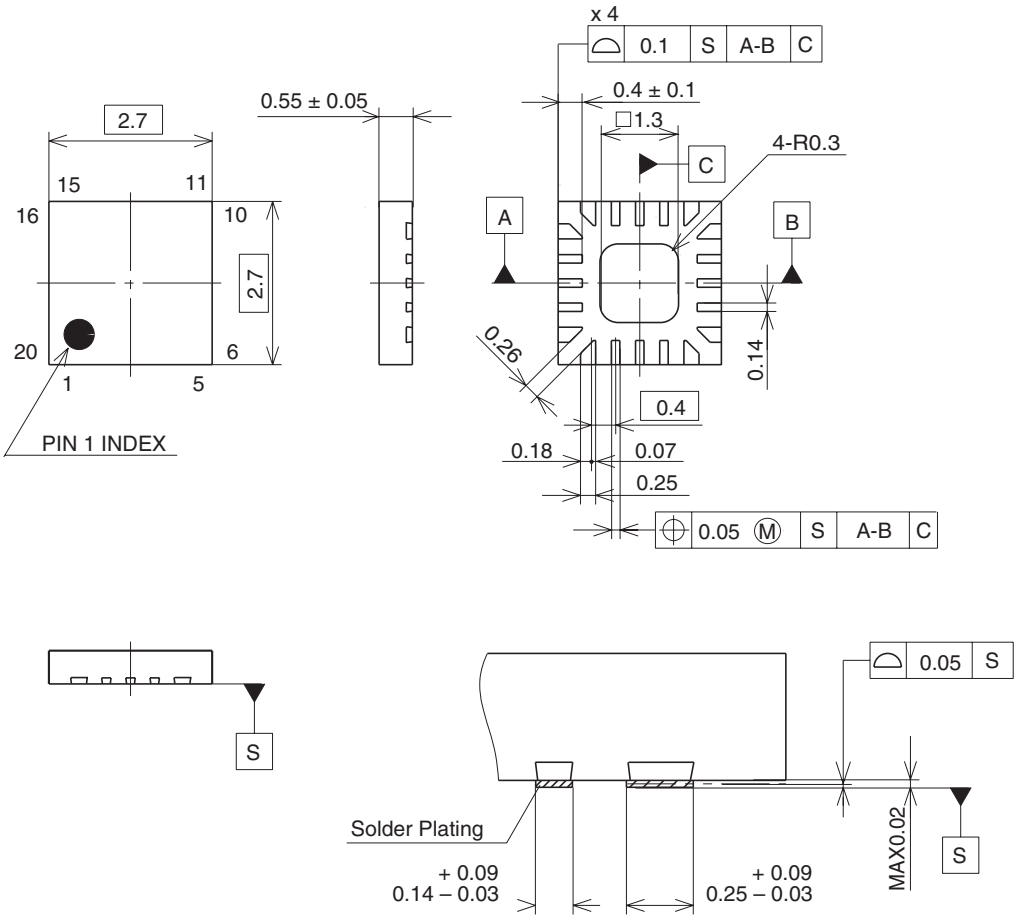
*3 Pin = 25dBm, 0/2.85V control, V_{DD} = 2.85V, 1.9GHz

*4 Pin = 25dBm (1.9GHz) + 25dBm (1.901GHz), 0/2.85V control, V_{DD} = 2.85V

Package Outline

(Unit: mm)

20PIN UQFN (PLASTIC)



TERMINAL SECTION

Note:Cutting burr of lead are 0.05mm MAX.

SONY CODE	UQFN-20P-01
EIAJ CODE	————
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.02g

LEAD PLATING SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	COPPER ALLOY
SOLDER COMPOSITION	Sn-Bi Bi:1-4wt%
PLATING THICKNESS	5-18µm