SONY

CXG7002FN

Power Amplifier/Antenna Switch + Low Noise Amplifier/Down Conversion Mixer for PHS

Description

The CXG7002FN is an MMIC consisting of the power amplifier, antenna switch, low noise amplifier and down conversion mixer.

This IC is designed using the Sony's GaAs J-FET process featuring a single positive power supply operation.

Features

- Operates at a single positive power supply: V_{DD} = 3V
- Small mold package: 26-pin HSOF

<Power amplifier/antenna switch transmitter block >

- Low current consumption: I_{DD} = 150mA
  (P_{OUT} = 20.2dBm, f = 1.9GHz)
- High power gain: Gp = 39dB Typ.
  (P_{OUT} = 20.2dBm, f = 1.9GHz)

<Antenna switch receiver block/ low noise amplifier>

- Low current consumption: I_{DD} = 2.5mA Typ.
  (When no signal)
- Low noise: NF = 2.7mA Typ. (f = 1.9GHz)

<Down conversion mixer>

- High conversion gain: Gc = 9dB Typ. (f = 1.9GHz)
- Low distortion: Input IP3 = +1dBm Typ. (f = 1.9GHz)

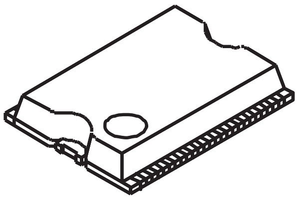
Applications

Digital cordless telephones (PHS)

Structure

GaAs J-FET MMIC

26 pin HSOF (Plastic)



Absolute Maximum Ratings

<Power amplifier block>

• Supply voltage	V_{DD}	6	V
• Voltage between gate and source	V_{GSO}	1.5	V
• Gain control voltage	VP_{CTL}	2.5	V
• Drain current	I_{DD}	550	mA
• Allowable power dissipation	P_D	3	W

<Switch block>

Control voltage	V_{CTL}	6	V

<Front-end block>

• Supply voltage	V_{DD}	6	V
• Input power	P_{RF}	+10	dBm

<Common to each block>

• Channel temperature	Tch	150	°C
• Operating temperature	Topr	–35 to +85	°C
• Storage temperature	Tstg	–65 to +150	°C

Recommended Operating Conditions

<Common to each block>

Supply voltage	V_{DD}	2.7 to 3.3	V

<Power amplifier block>

Gain control voltage	VP_{CTL}	to V_{DD} – 1.0	V

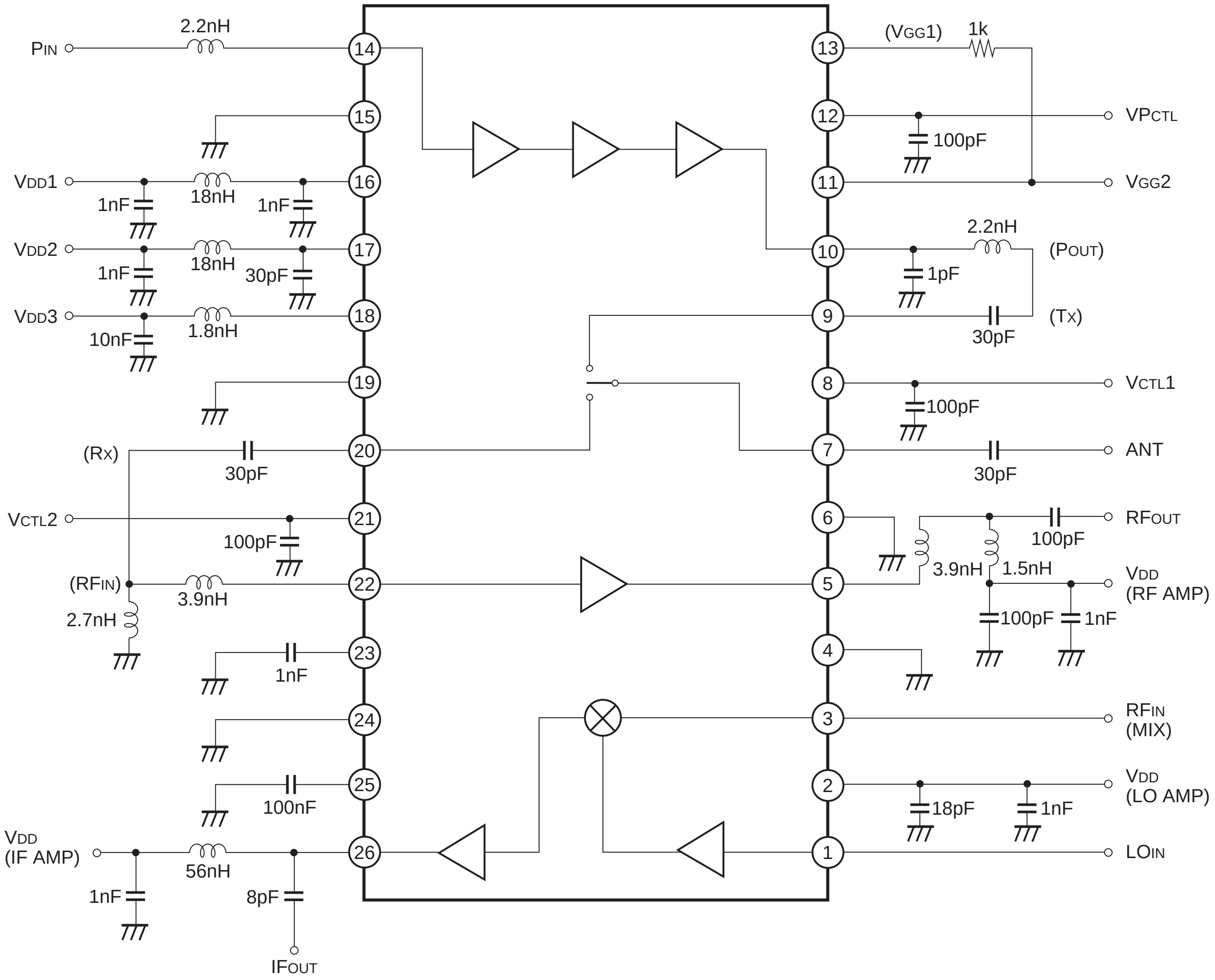
<Switch block>

• Control voltage (H)	V_{CTL} (H)	2.9 to 3.3	V
• Control voltage (L)	V_{CTL} (L)	0 to 0.2	V

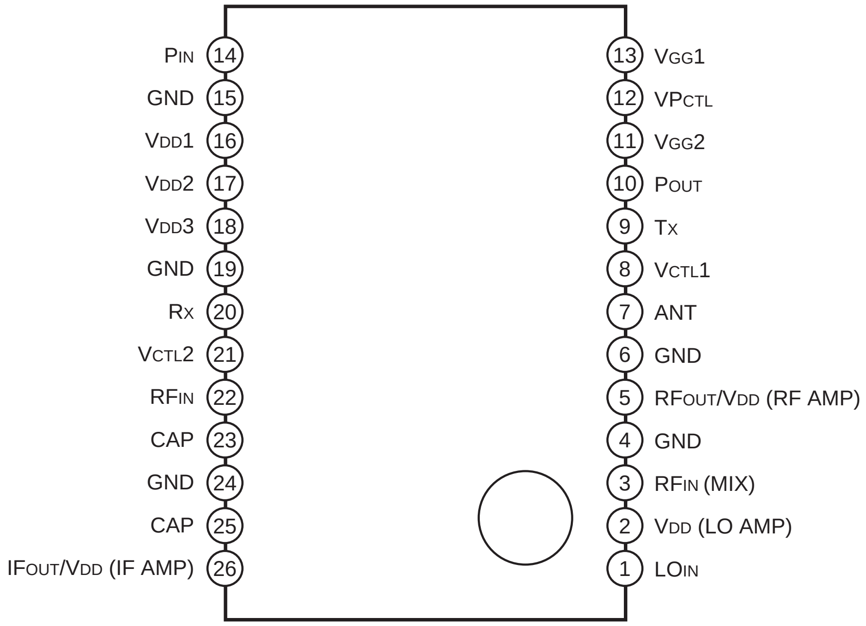
Notes on Handling

GaAs MMICs are ESD sensitive devices. Special handling precautions are required.

Block Diagram and External Circuit



Pin Configuration



Pin Description

Pin No.	Symbol	Description
1	LOIN	Local signal input pin
2	V_{DD} (LO AMP)	V_{DD} pin of local amplifier
3	RF_{IN} (MIX)	RF (MIX) signal input pin
4	GND	GND pin
5	RF_{OUT}/V_{DD} (RF AMP)	RF amplifier output and V_{DD} pin
6	GND	GND pin
7	ANT	Antenna switch pin This pin is ANT-Tx or ANT-Rx by setting of $V_{CTL}1$ and $V_{CTL}2$.
8	$V_{CTL}1$	Antenna switch control pin 1
9	Tx	Tx pin Signal is input to antenna switch during ANT-Tx.
10	P_{OUT}	Power amplifier output pin
11	$V_{GG}2$	Gate voltage adjustment pin of power amplifier (rear-end FET) 2
12	VP_{CTL}	Gain control pin of power amplifier (first stage FET)
13	$V_{GG}1$	Gate voltage adjustment pin of power amplifier (first stage, middle stage FET) 1
14	P_{IN}	Signal input pin to power amplifier
15	GND	GND pin
16	$V_{DD}1$	$V_{DD}1$ pin of power amplifier (first stage FET)
17	$V_{DD}2$	$V_{DD}2$ pin of power amplifier (middle stage FET)
18	$V_{DD}3$	$V_{DD}3$ pin of power amplifier (rear-end FET)
19	GND	GND pin
20	Rx	Rx pin ANT input signal is output to this pin during ANT-Rx.
21	$V_{CTL}2$	Antenna switch control pin 2
22	RF_{IN}	RF signal input pin
23	CAP	External capacitor connection pin This pin is connected to LNA FET source. RF amplifier characteristic is optimized during 1.9GHz by this capacitor (Typ. 1nF).
24	GND	GND pin
25	CAP	External capacitor connection pin IF amplifier distortion is improved by this capacitor.
26	IF_{OUT}/V_{DD} (IF AMP)	IF output and IF amplifier V_{DD} pin

Electrical Characteristics

1. Control Pin Logic for Antenna Switch

Conditions of control pins	ANT-T_X	ANT-R_X
$V_{CTL}1 = 3V$, $V_{CTL}2 = 0V$	ON	OFF
$V_{CTL}1 = 0V$, $V_{CTL}2 = 3V$	OFF	ON

2. Power Amplifier Block + Antenna Switch Transmitter Block

These specifications are when the Sony's recommended evaluation board with the external circuit shown on page 8 is used. Therefore, the power amplifier output pin (P_{OUT}) and the antenna switch transmission input pin (T_X) are connected via an external circuit. The specifications of the power amplifier block are set including the antenna switch transmitter block.

Unless otherwise specified: $V_{DD} = 3V$, $VP_{CTL} = 2V$, $V_{CTL}1 = 3V$, $V_{CTL}2 = 0V$, $I_{DD} = 150mA$,
$P_{OUT} = 20.2dBm$, f = 1.9GHz, Ta = 25°C

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Current consumption	I_{DD}			150		mA
Gate voltage adjustment value	V_{GG}		0	0.25	0.6	V
Output power	P_{OUT}	Measured with the ANT pin	20.2			dBm
Power gain	G_P		36	39		dB
Adjacent channel leak power ratio (600 ± 100kHz)	ACPR600kHz	Measured with the ANT pin		–63	–55	dBc
Adjacent channel leak power ratio (900 ± 100kHz)	ACPR900kHz	Measured with the ANT pin		–70	–60	dBc
Occupied bandwidth	OBW	Measured with the ANT pin		250	275	kHz
2nd-order harmonic level	—	Measured with the ANT pin			–25	dBc
3rd-order harmonic level	—	Measured with the ANT pin			–25	dBc

3. Antenna Switch Receiver Block + Font-end Block

These specifications are when the Sony's recommended evaluation board with the external circuit shown on page 8 is used. Therefore, the antenna switch reception pin (Rx) and the low noise amplifier input pin (RF_{IN_LNA}) are connected via an external circuit. The specifications of the low noise amplifier block are set including the antenna switch reception block.

(a) Antenna switch receiver block + low noise amplifier block

Unless otherwise specified: V_{DD} = 3V, $V_{CTL}1$ = 0V, $V_{CTL}2$ = 3V, RF = 1.9GHz/–30dBm, Ta = 25°C

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Current consumption	I_{DD_LNA}	When no signal		2.5	3.5	mA
Power gain	G_P		12.5	14.5	16.5	dB
Noise figure	NF			2.7	3.5	dB
Input IP3	IIP3	*1	–11	–8		dBm
Isolation	I_{SO}		25	30		dB

*1 Conversion from IM3 compression ratio during RF1 = 1.9000GHz/–30dBm and RF2 = 1.9006GHz/–30dBm input.

(b) Mixer Block

Unless otherwise specified: V_{DD} = 3V, RF = 1.90GHz/–25dBm, LO = 1.66GHz/–12dBm, Ta = 25°C

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
LO block current consumption	I_{DD_LO}	When no signal		1.7	2.5	mA
IF block current consumption	I_{DD_IF}	When no signal		3.3	4.5	mA
Conversion gain	G_C		7	9	11	dB
Noise figure	NF			8.5	11.5	dB
Input IP3	IIP3	*2	–2	+1		dBm
LO to ANT leak	PLK	*3		–43	–38	dBm

*2 Conversion from IM3 compression ratio during RF1 = 1.9000GHz/–25dBm and RF2 = 1.9006GHz/–25dBm input.

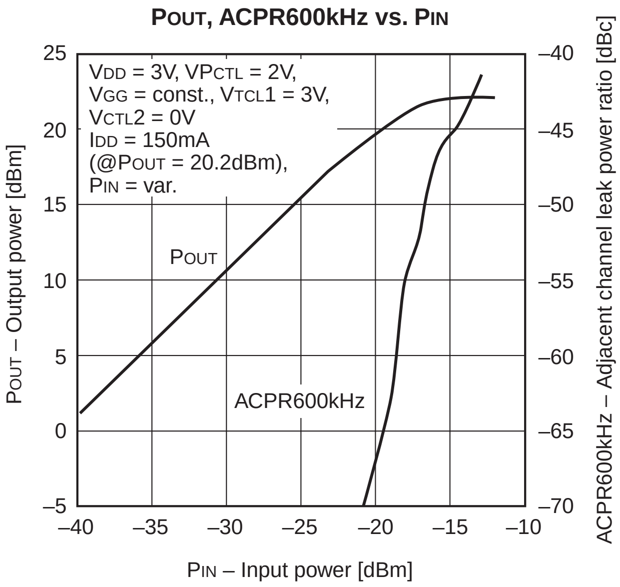
*3 The RF_{OUT} pin of the LNA and the RF_{IN} pin of the MIX block is connected directly with the cable.
And the power supply of the LNA is turned on.

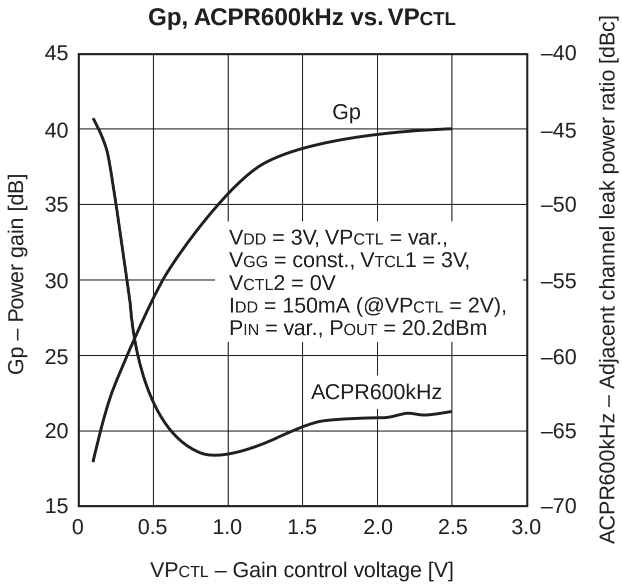
(c) Total of (a) + (b)

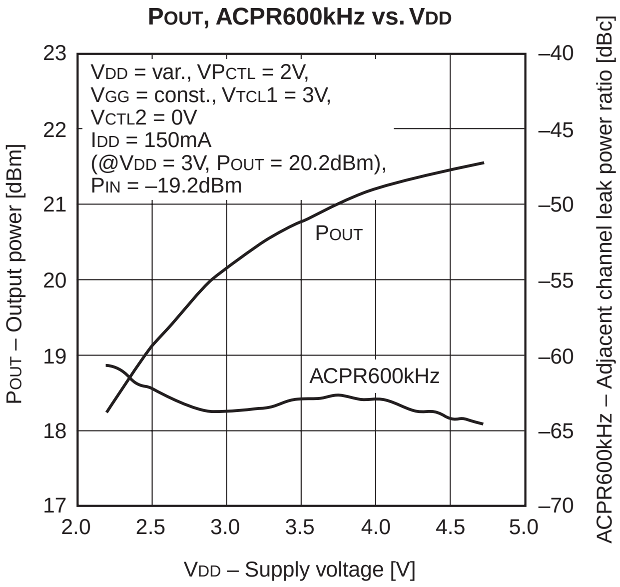
Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Current consumption	I_{DD}_total	When no signal		7.5	10	mA

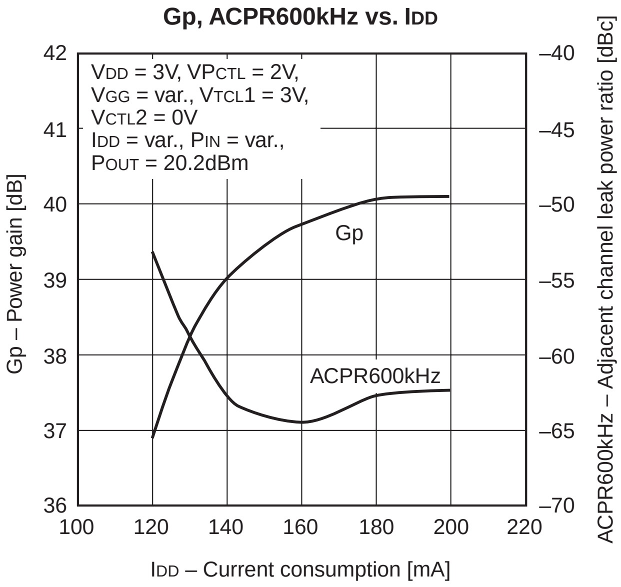
Example of Representative Characteristics

1. Power Amplifier + Antenna Switch Transmitter Block (f = 1.9GHz, Ta = 25°C)

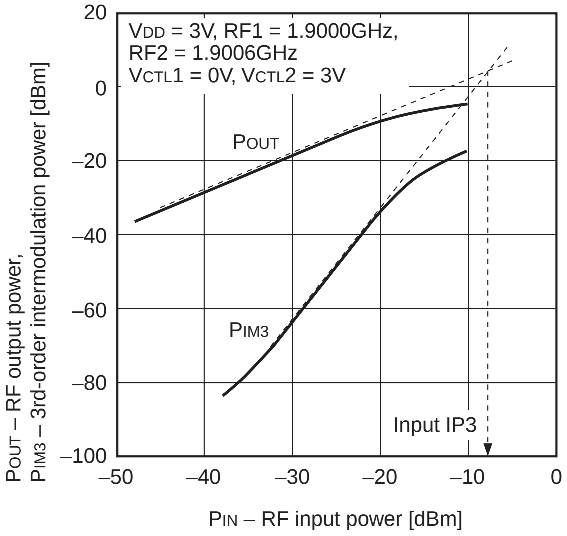

P_{OUT}, ACPR600kHz vs. P_{IN}


Gp, ACPR600kHz vs. VP_{CTL}

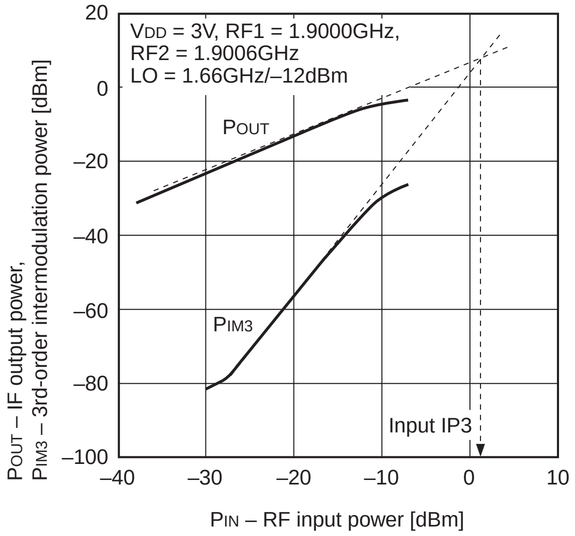

P_{OUT}, ACPR600kHz vs. V_{DD}


Gp, ACPR600kHz vs. I_{DD}

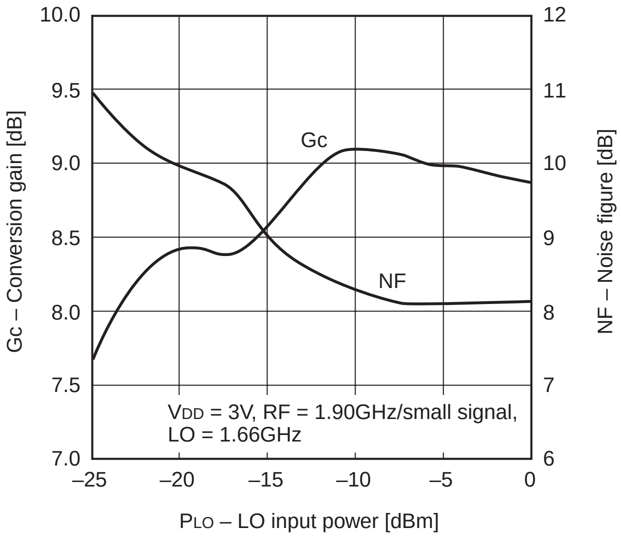
2. Antenna Switch Receiver Block + Low Noise Amplifier, Down Conversion Mixer (Ta = 25°C)



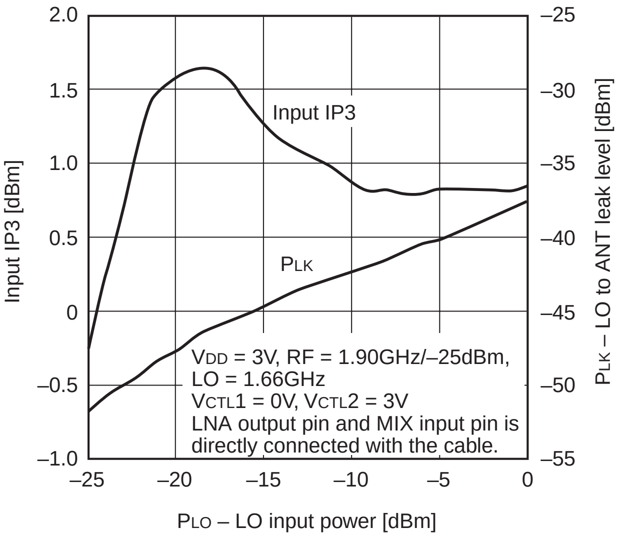
SW/LNA block: P_{OUT}, P_{IM3} vs. P_{IN}



MIX block: P_{OUT}, P_{IM3} vs. P_{IN}

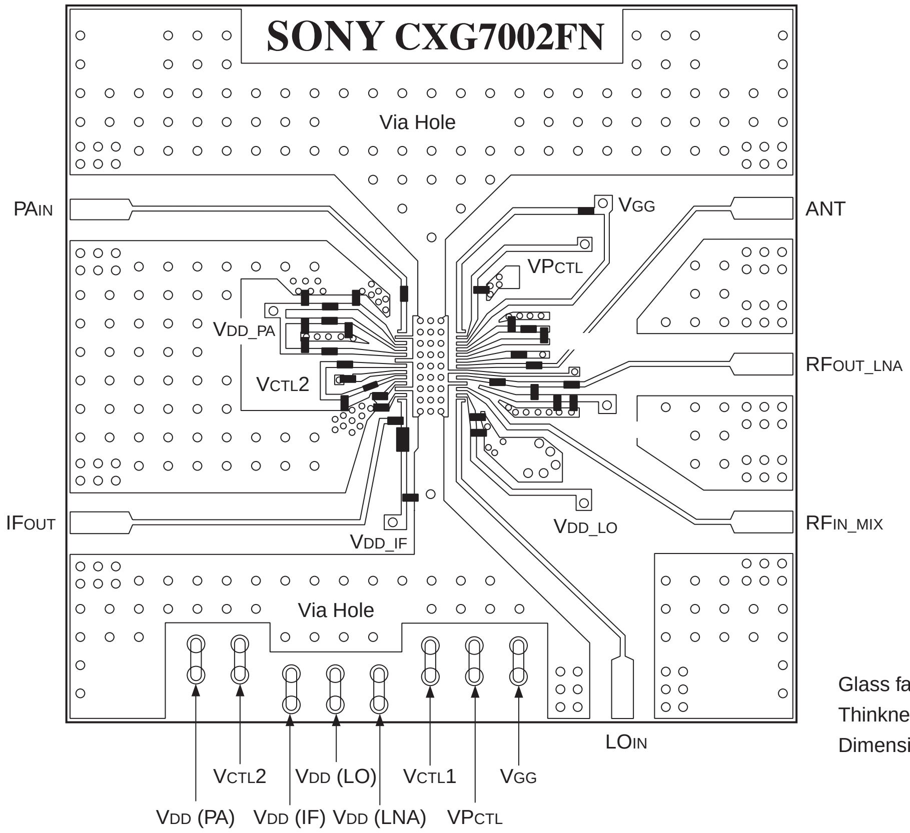


MIX block: Gc, NF vs. P_{LO}



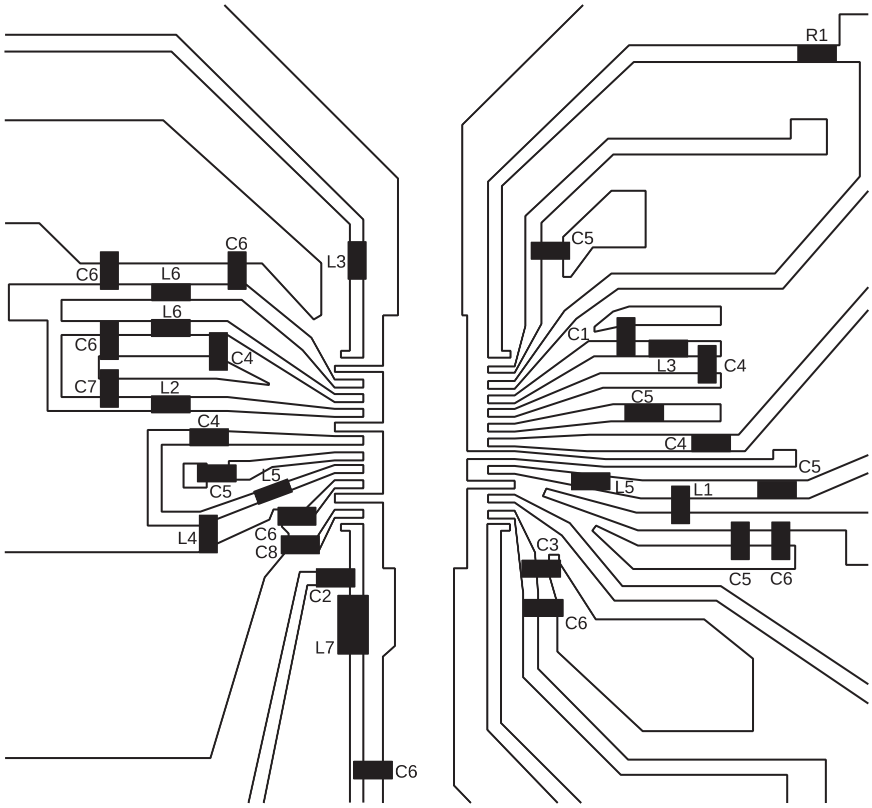
MIX block: Input IP3, P_{LK} vs. P_{LO}

Recommended Evaluation Board



Glass fabric-base epoxy board (4 layers)
Thinkness between layers 1 and 2: 0.2mm
Dimensions: 50mm × 50mm

Enlarged Diagram of External Circuit Block



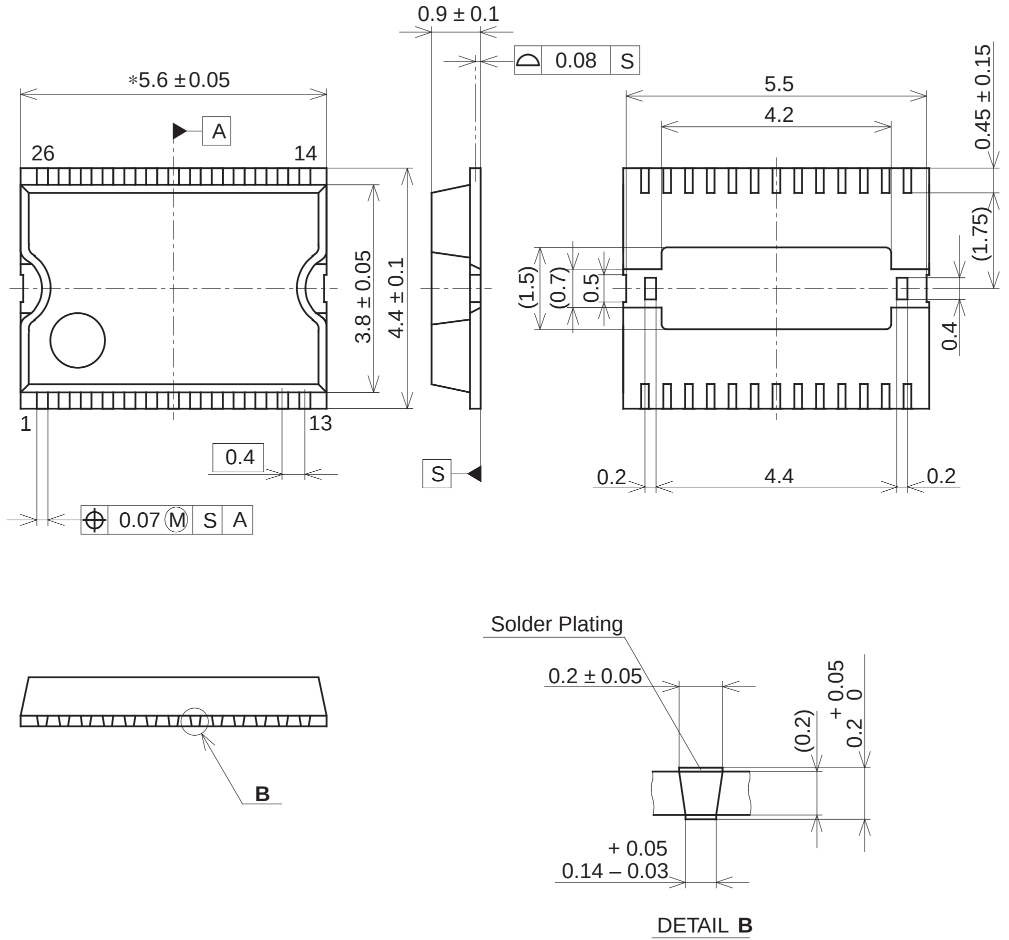
R1 = 1k

L1 = 1.5nH
L2 = 1.8nH
L3 = 2.2nH
L4 = 2.7nH
L5 = 3.9nH
L6 = 18nH
L7 = 56nH

C1 = 1pF
C2 = 8pF
C3 = 18pF
C4 = 30pF
C5 = 100pF
C6 = 1nF
C7 = 10nF
C8 = 100nF

Package Outline Unit: mm

HSOF 26PIN (PLASTIC)



NOTE: Dimension "∗" does not include mold protrusion.

SONY CODE	HSOF-26P-01
EIAJ CODE	————
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.06g

LEAD PLATING SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	COPPER ALLOY
SOLDER COMPOSITION	Sn-Bi Bi:1-4wt%
PLATING THICKNESS	5-18µm