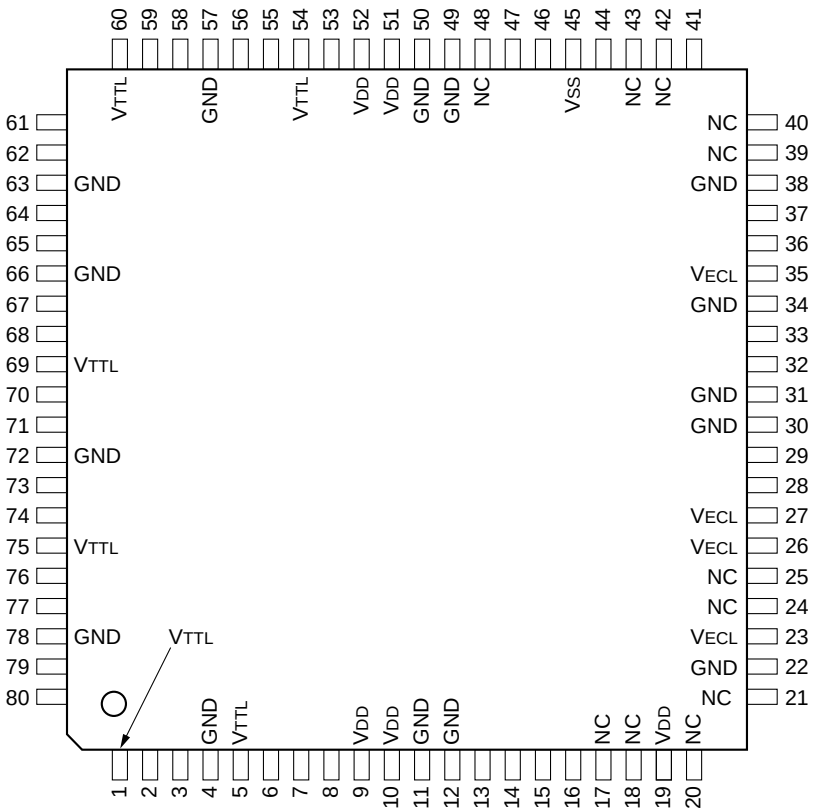
1.5 Gbps RECEIVER

—TOP VIEW—



PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	—	VTTL	21	—	NC	41	O	OLTN	61	O	OD15
2	O	OD01	22	—	GND	42	—	NC	62	O	OD14
3	O	OD00	23	—	VECL	43	—	NC	63	—	GND
4	—	GND	24	—	NC	44	O	OLT	64	O	OD13
5	—	VTTL	25	—	NC	45	—	VSS	65	O	OD12
6	O	OCLK74T	26	—	VECL	46	I	XTEST1	66	—	GND
7	I	XTEST2	27	—	VECL	47	I	XRST	67	O	OD11
8	I	XTEST3	28	O	OCLK74EN	48	—	NC	68	O	OD10
9	—	VDD	29	O	OCLK74E	49	—	GND	69	—	VTTL
10	—	VDD	30	—	GND	50	—	GND	70	O	OD09
11	—	GND	31	—	GND	51	—	VDD	71	O	OD08
12	—	GND	32	I	TCLK148N	52	—	VDD	72	—	GND
13	I	ICNT0	33	I	TCLK148	53	O	TRSFG	73	O	OD07
14	I	ICNT1	34	—	GND	54	—	VTTL	74	O	OD06
15	I	ICNT2	35	—	VECL	55	O	OD19	75	—	VTTL
16	I	ICNT3	36	I	IDN	56	O	OD18	76	O	OD05
17	—	NC	37	I	ID	57	—	GND	77	O	OD04
18	—	NC	38	—	GND	58	O	OD17	78	—	GND
19	—	VDD	39	—	NC	59	O	OD16	79	O	OD03
20	—	NC	40	—	NC	60	—	VTTL	80	O	OD02

INPUTS

ICNT0 - ICNT3	:	PARALLEL CLOCK DELAY CONTROL
ID	:	1.485 Gbps SERIAL DATA
IDN	:	INVERTED 1.485 Gbps SERIAL DATA
TCLK148	:	EXTERNAL CLOCK (1.485 GHz)
TCLK148N	:	INVERTED EXTERNAL CLOCK (1.485 GHz)
XRST	:	RESET
XTEST1	:	NRZI → NRZ CONVERSION AND DESCRAMBLER CONTROL
XTEST2	:	TRS DETECTOR CONTROL
XTEST3	:	CH/YH FLAG DETECTOR CONTROL

OUTPUTS

OD00 - OD19	:	20 BITS PARALLEL SIGNAL
OCLK74E	:	74.25 MHz PARALLEL CLOCK (ECL LEVEL)
OCLK74EN	:	INVERTED 74.25 MHz PARALLEL CLOCK (ECL LEVEL)
OCLK74T	:	4.25 MHz PARALLEL CLOCK (LVTTL LEVEL)
OLT	:	RETIMING DATA OF DISCRIMINATOR
OLTN	:	INVERTED DATA OF DISCRIMINATOR
TRSFG	:	TRS DETECTOR