

SONY**CXK541000J** -25/30/35**262144-word × 4-bit High Speed CMOS Static RAM** *Preliminary***Description**

CXK541000J is a 1048576 bits high speed CMOS static RAM organized as 262144 words by 4 bits and operates from a single 5V supply.

This device is suitable for use in high speed and low power applications.

Features

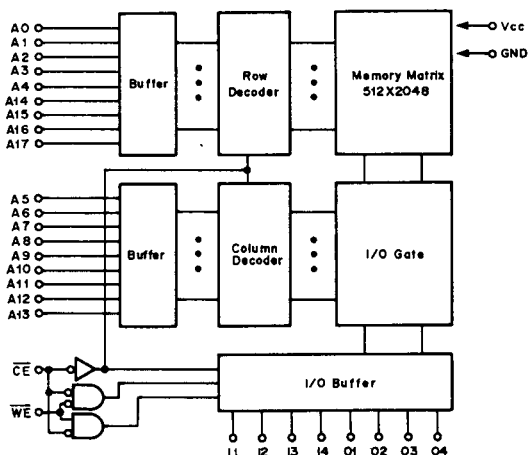
- Fast access time (Access time)
CXK541000J-25 25ns (Max.)
CXK541000J-30 30ns (Max.)
CXK541000J-35 35ns (Max.)
- Low power consumption (operation) : 350mW (Typ.)
- Single +5V power supply: 5V ± 10%
- Fully static memory No clock or timing strobe required.
- Equal access and cycle time.
- Separated data input and output; three-state output
- Directly TTL compatible: All inputs and outputs
- High density: 400 mil 32 pin SOJ plastic package

Function

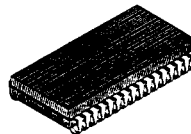
262144-word × 4-bit static RAM

Structure

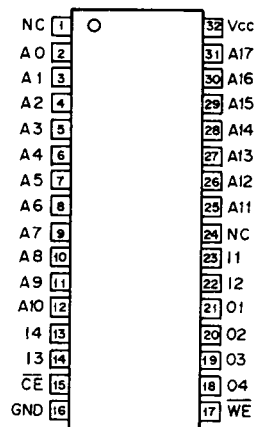
Silicon gate CMOS IC

Block Diagram

32 pin SOJ (Plastic)

**Pin Configuration**

(Top View)

**Pin Description**

Symbol	Description
A0 to A17	Address input
I1 to I4	Data input
O1 to O4	Data output
CE	Chip enable input
WE	Write enable input
Vcc	+5V Power supply
GND	Ground
NC	No connection

Sony reserves the right to change products and specifications without prior notice. This information does not convey any license by any implication or otherwise under any patents or other right. Application circuits shown, if any, are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits.

Absolute Maximum Ratings

(Ta=25°C, GND=0V)

Item	Symbol	Rating	Unit
Supply voltage	V _{CC}	-0.5 * to +7.0	V
Input voltage	V _{IN}	-0.5 * to V _{CC} +0.5	V
Input and output voltage	V _{IO}	-0.5 * to V _{CC} +0.5	V
Allowable power dissipation	P _D	1.0	W
Operating temperature	T _{opr}	-10 to +85	°C
Storage temperature	T _{stg}	-55 to +150	°C
Soldering temperature*time	T _{solder}	260*10	°C*sec

* V_{CC}, V_{IN}, V_{IO}=+7.5V Max. for pulse width less than 10ns.V_{CC}, V_{IN}, V_{IO}=-3.5V Min. for pulse width less than 10ns.**Truth Table**

CE	WE	Mode	Data Output	V _{CC} Current
H	×	Not selected	High Z	I _{SB1} , I _{SB2}
L	H	Read	Data out	I _{CC}
L	L	Write	High Z	I _{CC}

× : "H" or "L"

DC Recommended Operating Conditions

(Ta=0 to +70°C, GND=0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.2	—	V _{CC} +0.5	V
Input low voltage	V _{IL}	-0.5 *	—	0.8	V
Input rise time	t _r	—	5	100	ns
Input fall time	t _f	—	5	100	ns

* V_{IH}=+7.0V Max. for pulse width less than 10ns.V_{IL}=-3.0V Min. for pulse width less than 10ns.

Electrical Characteristics

● DC and operating characteristics

(V_{CC}=5V ± 10%, GND=0V, T_a=0 to +70 °C)

Item	Symbol	Test conditions	Min.	Typ. *	Max.	Unit
Input leak current	I _I	V _{IN} =GND to V _{CC} V _{CC} =5.5V	-1	—	1	μA
Output leak current	I _{LO}	$\overline{CE}=V_{IH}$ or $\overline{WE}=V_{IL}$ V _{OUT} =GND to V _{CC}	-1	—	1	μA
Average operating current	I _{CC}	Cycle=Min, Duty=100% I _{OUT} =0mA	—	70	120	mA
Standby current	I _{SB1}	$\overline{CE} \geq V_{CC}-0.2V$, V _{IN} ≥ V _{CC} -0.2V or V _{IN} ≤ 0.2V	—	—	2	mA
	I _{SB2}	$\overline{CE}=V_{IH}$, V _{IN} =V _{IH} /V _{IL} , min. cycle	—	15	30	mA
Output high voltage	V _{OH}	I _{OH} =-4.0mA	2.4	—	—	V
Output low voltage	V _{OL}	I _{OL} =8.0mA	—	—	0.4	V

* V_{CC}=5V, T_a=25 °C

I/O capacitance

(T_a=25 °C, f=1MHz)

Item	Symbol	Test conditions	Min.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} =0V	—	6	pF
Output capacitance	C _{OUT}	V _{OUT} =0V	—	10	pF

Note) This parameter is sampled and is not 100% tested.

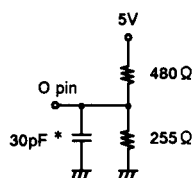
AC characteristics

● AC test conditions

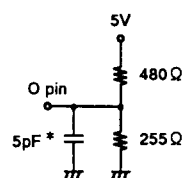
(V_{CC}=5V ± 10%, T_a=0 to +70 °C)

Item	Conditions
Input pulse high level	V _{IH} =3.0V
Input pulse low level	V _{IL} =0V
Input rise time	t _r =5ns
Input fall time	t _f =5ns
Input and output reference level	1.5V
Output load conditions	Fig. 1

Output Load (1)



Output Load (2)**



* including scope and jig

** for t_{LZ}, t_{HZ}, t_{OW}, t_{WHZ}

Fig. 1

● Read cycle

Item	Symbol	-25		-30		-35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t _{RC}	25	—	30	—	35	—	ns
Address access time	t _{AA}	—	25	—	30	—	35	ns
Chip enable access time (CE)	t _{CO}	—	25	—	30	—	35	ns
Output hold from address change	t _{OH}	5	—	5	—	5	—	ns
Chip enable to output in low Z (CE)	t _{LZ} *	5	—	5	—	5	—	ns
Chip disable to output in high Z	t _{HZ} *	0	15	0	15	0	15	ns
Chip enable to power up time	t _{PU}	0	—	0	—	0	—	ns
Chip disable to power down time	t _{PD}	—	25	—	30	—	35	ns

* Transition is measured $\pm 200\text{mV}$ from steady voltage with specified loading in Fig. 1. This parameter is sampled and is not 100% tested.

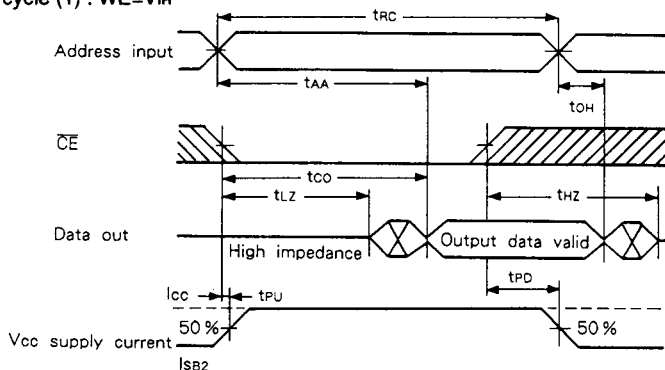
● Write cycle

Item	Symbol	-25		-30		-35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t _{WC}	25	—	30	—	35	—	ns
Address valid to end of write	t _{AW}	18	—	20	—	20	—	ns
Chip enable to end of write	t _{CW}	18	—	20	—	20	—	ns
Data to write time overlap	t _{DW}	12	—	15	—	15	—	ns
Data hold from write time	t _{DH}	0	—	0	—	0	—	ns
Write pulse width	t _{WP}	15	—	18	—	18	—	ns
Address set up time	t _{AS}	0	—	0	—	0	—	ns
Write recovery time	t _{WR}	2	—	2	—	2	—	ns
Output active from end of write	t _{OW} *	5	—	5	—	5	—	ns
Write to output in high Z	t _{WHZ} *	0	15	0	15	0	15	ns

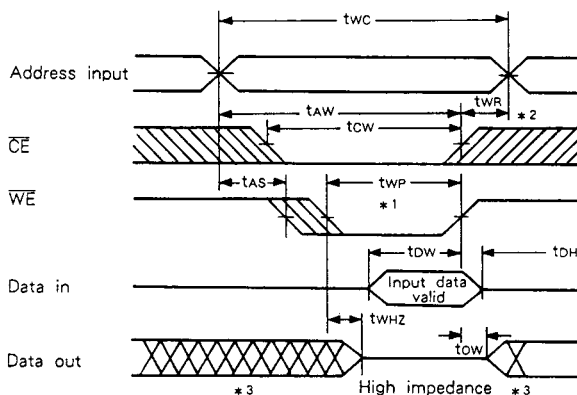
* Transition is measured $\pm 200\text{mV}$ from steady voltage with specified loading in Fig. 1. This parameter is sampled and is not 100% tested.

Timing Waveform

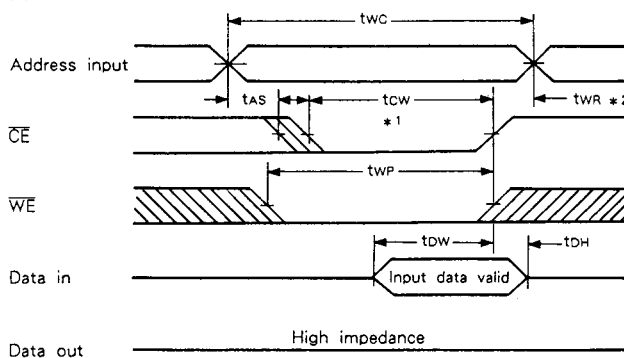
• Read cycle (1) : $\overline{WE}=V_{IH}$



• Write cycle (1) : \overline{WE} control



• Write cycle (2) : \overline{CE} control



*1. A write occurs during the low overlap of \overline{CE} and \overline{WE} .

*2. t_{WR} is measured from the earlier of \overline{CE} or \overline{WE} going high to the end of write cycle.

*3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the output must not be applied.

Package Outline Unit : mm

32pin SOJ (Plastic) 400mil 1.3g

