

**SONY****CXK541020J** -20/25**262144-words x 4-bits High Speed CMOS Static RAM****Description**

The CXK541020J is a high speed CMOS static RAM organized as 262144-words by 4 bits.

It operates at 20ns/25ns access time from 5V single power supply.

The CXK541020J is suitable for use in high speed applications.

**Features**

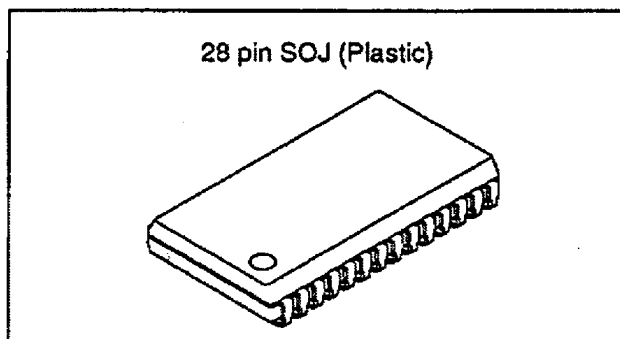
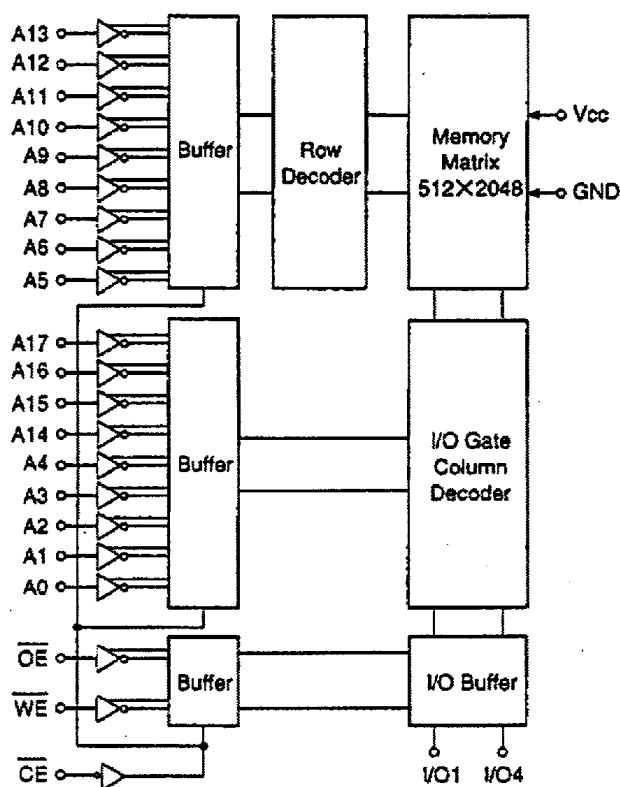
- Fast access time: (Access time)
  - CXK541020J-20 20ns (Max.)
  - CXK541020J-25 25ns (Max.)
- Low power consumption (operation)
  - CXK541020J-20 880mW (Max.)
  - CXK541020J-25 825mW (Max.)
- Single +5V supply:  $5V \pm 10\%$
- Fully static memory ... No clock or timing strobe required
- Equal access and cycle time
- Directly TTL compatible all inputs and outputs
- Package
  - CXK541020J 400mil 28pin SOJ Package

**Function**

262144-words x 4-bits static RAM

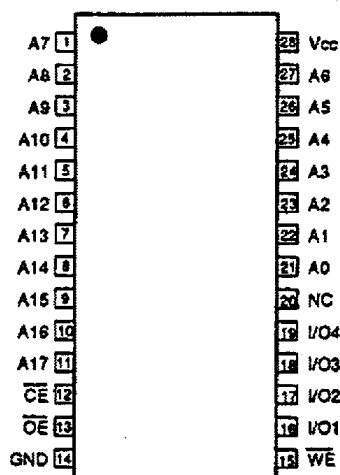
**Structure**

- Silicon gate CMOS IC

**Block Diagram**

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## Pin Configuration (Top View)



## Pin Description

Symbol	Description
A0 to A17	Address input
I/O1 to I/O4	Data input output
$\overline{CE}$	Chip enable input
$\overline{WE}$	Write enable input
$\overline{OE}$	Output enable input
Vcc	+5V Power supply
GND	Ground
NC	No connection

## Absolute Maximum Ratings

(Ta = 25°C, GND = 0V)

Item	Symbol	Rating	Unit
Supply voltage	Vcc	-0.5 to +7.0	V
Input voltage	V <sub>IN</sub>	-0.5* to Vcc + 0.5	V
Input and output voltage	V <sub>IO</sub>	-0.5* to Vcc + 0.5	V
Allowable power dissipation	P <sub>D</sub>	1.0	W
Operating temperature	T <sub>opr</sub>	0 to +70	°C
Storage temperature	T <sub>stg</sub>	-45 to +125	°C
Soldering temperature · time	T <sub>solder</sub>	235 · 10	°C · s

\* Vcc, V<sub>IN</sub>, V<sub>IO</sub> = -3.0V Min. for pulse width less than 5ns.

## Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O pin	Vcc current
H	X	X	Not selected	High Z	I <sub>SB1</sub> , I <sub>SB2</sub>
L	H	H	Output disable	High Z	I <sub>CC</sub>
L	L	H	Read	Data out	I <sub>CC</sub>
L	X	L	Write	Data in	I <sub>CC</sub>

X: "H" or "L"

## DC Recommended Operating Conditions

(Ta = 0 to +70°C, GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Vcc	4.5	5.0	5.5	V
Input high voltage	V <sub>IH</sub>	2.2	—	Vcc + 0.3	V
Input low voltage	V <sub>IL</sub>	-0.3*	—	0.8	V

\* V<sub>IL</sub> = -3.0V Min. for pulse width less than 5ns.

## Electrical Characteristics

## • DC characteristics

(V<sub>CC</sub> = 5V±10%, GND = 0V, T<sub>a</sub> = 0 to +70°C)

Item	Symbol	Test conditions	Min.	Typ.*1	Max.	Unit	
Input leakage current	I <sub>LI</sub>	V <sub>IN</sub> = GND to V <sub>CC</sub>	-2	—	2	μA	
Output leakage current	I <sub>LO</sub>	$\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$ V <sub>VO</sub> = GND to V <sub>CC</sub>	-2	—	2	μA	
Average operating current	I <sub>CC</sub>	Min. cycle duty = 100% *2 I <sub>OUT</sub> = 0mA	Write	20	—	160	mA
				25	—	150	
			Read	20	—	110	
				25	—	100	
Standby current	I <sub>SB1</sub>	$\overline{CE} \geq V_{CC} - 0.2V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> ≤ 0.2V	—	—	2	mA	
	I <sub>SB2</sub>	$\overline{CE} = V_{IH}$ , V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , Min. cycle	20	—	35	mA	
		25	—	30			
Output high voltage	V <sub>OH</sub>	I <sub>OH</sub> = -4.0mA	2.4	—	—	V	
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> = 8.0mA	—	—	0.4	V	

\*1 V<sub>CC</sub> = 5V, T<sub>a</sub> = 25°C

\*2 Address is increased with binary count.

## I/O Capacitance

(T<sub>a</sub> = 25°C, f = 1MHz)

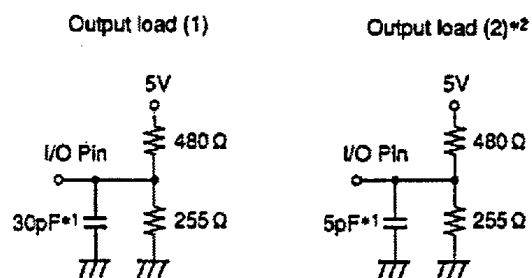
Item	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Input capacitance	C <sub>IN</sub>	V <sub>IN</sub> = 0V	—	—	7	pF
I/O capacitance	C <sub>I/O</sub>	V <sub>VO</sub> = 0V	—	—	7	pF

Note) This parameter is sampled and is not 100% tested.

## AC Characteristics

• AC test conditions (V<sub>CC</sub> = 5V±10%, T<sub>a</sub> = 0 to +70°C)

Item	Conditions
Input pulse high level	V <sub>IH</sub> = 3.0V
Input pulse low level	V <sub>IL</sub> = 0V
Input rise time	t <sub>r</sub> = 3ns
Input fall time	t <sub>f</sub> = 3ns
Input and output reference level	1.5V
Output load conditions	Fig. 1



\*1 This parameter includes scope and jig capacitances.

\*2 For t<sub>LZ</sub>, t<sub>OLZ</sub>, t<sub>HZ</sub>, t<sub>OHZ</sub>, t<sub>OW</sub>, t<sub>WHZ</sub>

Fig. 1.

• Read cycle ( $\overline{WE} = "H"$ )

Item	Symbol	-20		-25		Unit
		Min.	Max.	Min.	Max.	
Read cycle time	t <sub>RC</sub>	20	—	25	—	ns
Address access time	t <sub>AA</sub>	—	20	—	25	ns
Chip enable access time ( $\overline{CE}$ )	t <sub>CO</sub>	—	20	—	25	ns
Output enable to output valid	t <sub>OE</sub>	—	10	—	12	ns
Output hold from address change	t <sub>OH</sub>	5	—	5	—	ns
Chip enable to output in low Z ( $\overline{CE}$ )	t <sub>LZ*</sub>	5	—	5	—	ns
Output enable to output in low Z ( $\overline{OE}$ )	t <sub>OLZ*</sub>	2	—	2	—	ns
Chip disable to output in high Z ( $\overline{CE}$ )	t <sub>HZ*</sub>	—	9	—	10	ns
Output disable to output in high Z ( $\overline{OE}$ )	t <sub>OHZ*</sub>	—	9	—	10	ns
Chip enable to power up time	t <sub>PU</sub>	0	—	0	—	ns
Chip disable to power down time	t <sub>PD</sub>	—	20	—	25	ns

\* Transition is measured  $\pm 200\text{mV}$  from steady voltage with specified loading in Fig. 1-(2).  
This parameter is sampled and is not 100% tested.

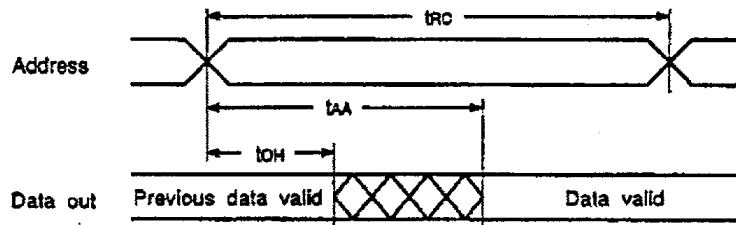
## • Write cycle

Item	Symbol	-20		-25		Unit
		Min.	Max.	Min.	Max.	
Write cycle time	t <sub>WC</sub>	20	—	25	—	ns
Address valid to end of write	t <sub>AW</sub>	15	—	20	—	ns
Chip enable to end of write	t <sub>CW</sub>	15	—	20	—	ns
Data to write time overlap	t <sub>DW</sub>	10	—	12	—	ns
Data hold from write time	t <sub>DH</sub>	0	—	0	—	ns
Write pulse width	t <sub>WP</sub>	15	—	20	—	ns
Address setup time	t <sub>AS</sub>	0	—	0	—	ns
Write recovery time ( $\overline{WE}$ )	t <sub>WR</sub>	0	—	0	—	ns
Write recovery time ( $\overline{CE}$ )	t <sub>WR1</sub>	0	—	0	—	ns
Output active from end of write	t <sub>OW*</sub>	5	—	5	—	ns
Write to output in high Z	t <sub>WHZ*</sub>	—	9	—	10	ns

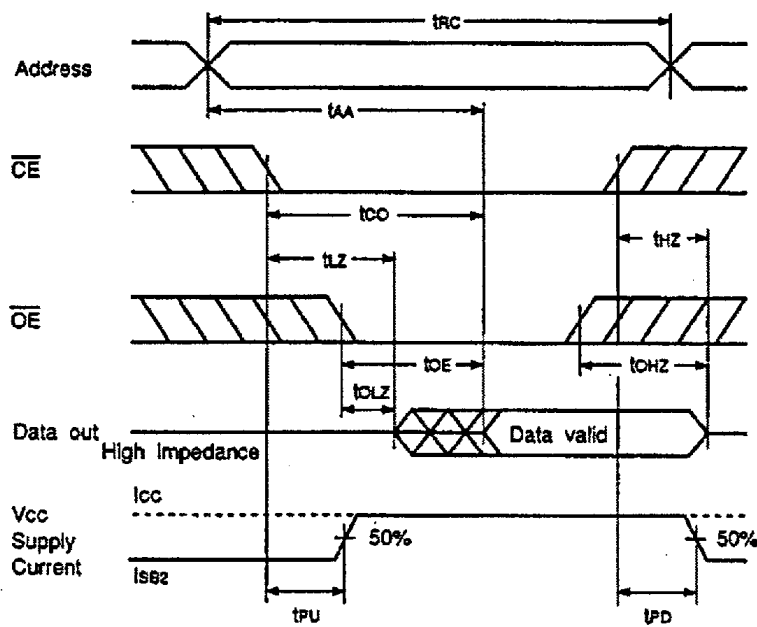
\* Transition is measured  $\pm 200\text{mV}$  from steady voltage with specified loading in Fig. 1-(2).  
This parameter is sampled and is not 100% tested.

## Timing Waveform

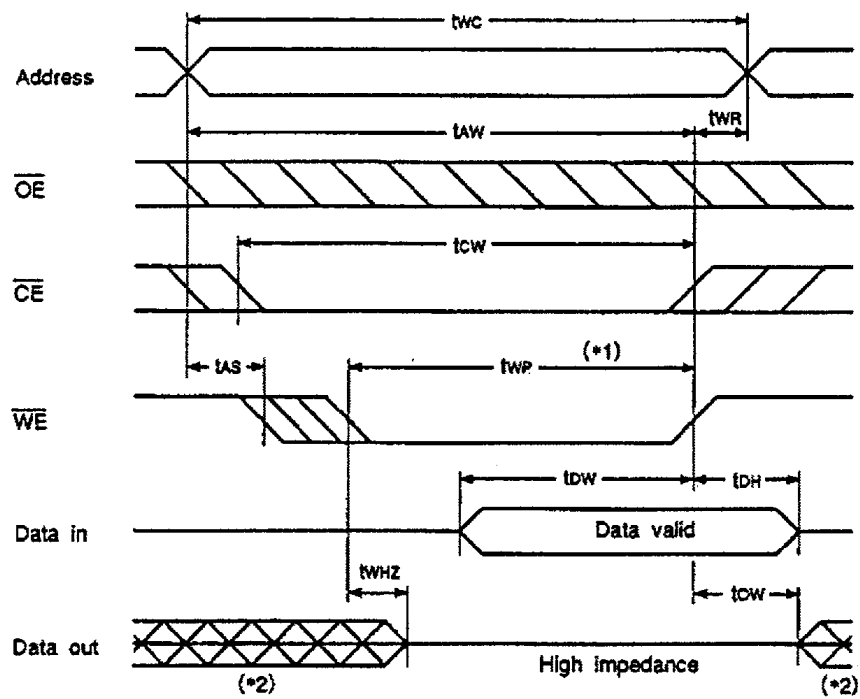
- Read cycle (1) :  $\overline{CE} = \overline{OE} = V_{IL}$ ,  $\overline{WE} = V_{IH}$



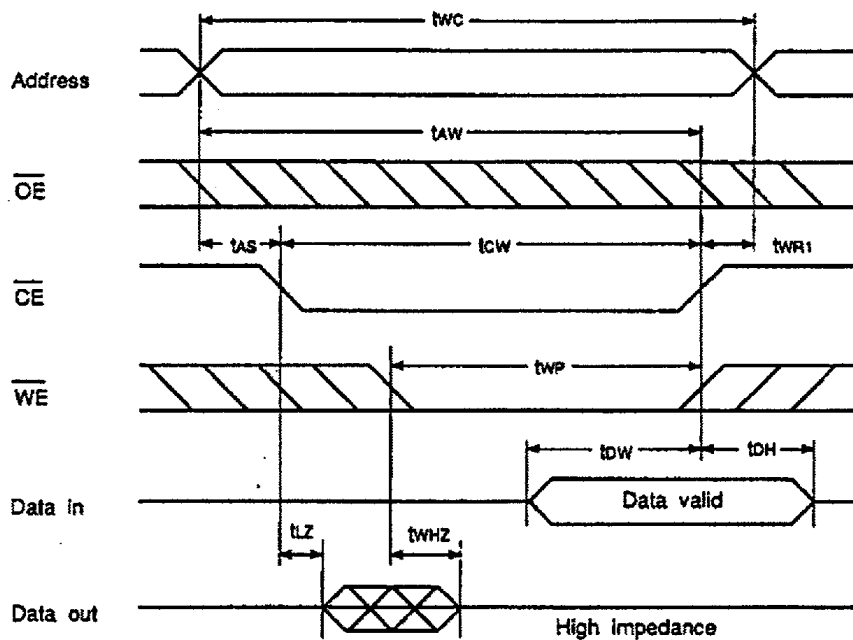
- Read cycle (2) :  $\overline{WE} = V_{IH}$



• Write cycle (1) :  $\overline{WE}$  control



• Write cycle (2) :  $\overline{CE}$  control



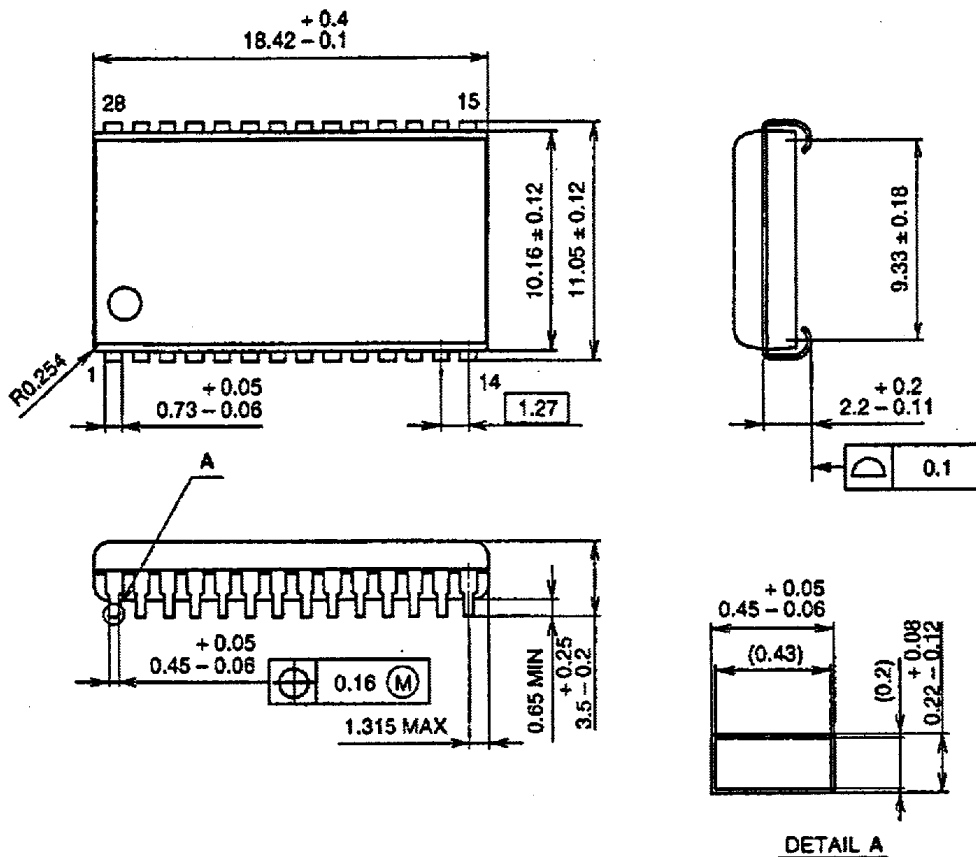
\*1 Write is executed when both  $\overline{CE}$  and  $\overline{WE}$  are at low simultaneously.

\*2 Do not apply the data input voltage of the opposite phase to the output while I/O pin is in output condition.

Package Outline

Unit : mm

28PIN SOJ (PLASTIC) 400mil



PACKAGE STRUCTURE

SONY CODE	SOJ-28P-02
EIAJ CODE	*SOJ028-P-0400-A
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER
PACKAGE WEIGHT	1.1g