

SONY

CXK5416P

35/35L/45/45L/55/55L

4096-word \times 4 bit High Speed CMOS Static RAM**Description**

The CXK5416P is a 16,384 bits high speed CMOS static RAM organized as 4,096 words by 4 bits and operates from a single 5V supply.

The CXK5416P is suitable for use in high speed and low power applications in which battery back up for nonvolatility is required.

Features

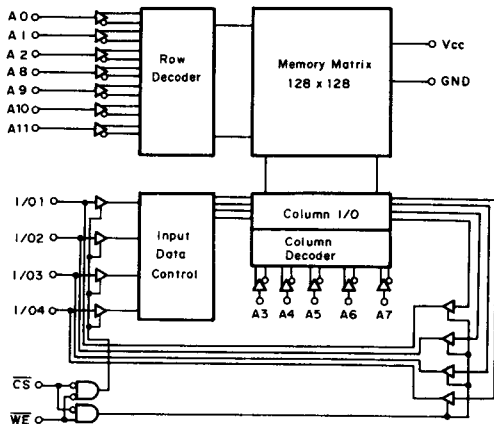
- Fast access time: 35 ns/45 ns/55 ns (Max.)
- Low power standby: 5 μ W (Typ.)—L-version
100 μ W (Typ.)—Standard version
- Low power operation: 200 mW (Typ.)
- Single +5V supply
- Fully static memory No clock or timing strobe required
- Equal access and cycle time
- Common data input and output: Three state output
- Directly TTL compatible: All inputs and outputs
- Low voltage data retention: 2.0V (Min.)

Structure

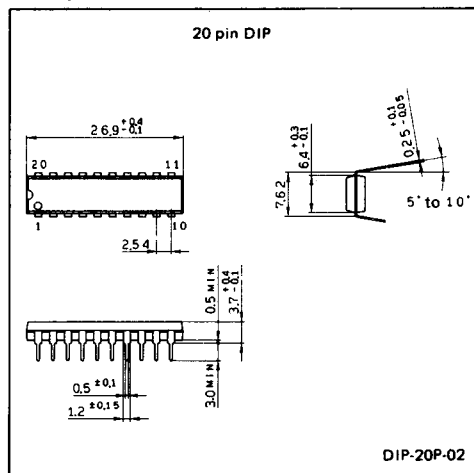
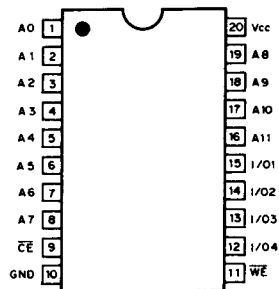
Silicon gate CMOS IC

Function

4096-word \times 4-bit static RAM

Block Diagram**Package Outline**

Unit: mm

**Pin Configuration (Top View)**

Symbol	Description
A0 to A11	Address Input
I/O 1 to I/O 4	Data Input Output
\overline{CE}	Chip Enable Input
\overline{WE}	Write Enable Input
Vcc	Power Supply
GND	Ground

www.DataSheet4U.com

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Power Supply Voltage	V _{CC}	-0.5* to +7.0	V
Input Voltage	V _{IN}	-0.5* to V _{CC} +0.5	V
Input and Output Voltage	V _{I/O}	-0.5* to V _{CC} +0.5	V
Allowable Power Dissipation	P _D	1.0	W
Operating Temperature	T _{opr}	0 to +70	°C
Storage Temperature	T _{stg}	-55 to +150	°C
Soldering Temperature	T _{solder}	260 ± .10	°C • sec

* V_{CC}, V_{IN}, V_{I/O} min=-3.5V for pulse width less than 20 ns.

Truth Table

\overline{CE}	\overline{WE}	Mode	I/O 1 to I/O 4	V _{CC} Current
H	X	Not Selected	High Z	I _{sB1} , I _{sB2}
L	H	Read	DOUT	I _{CC1} , I _{CC2}
L	L	Write	DIN	I _{CC1} , I _{CC2}

X: "H" or "L"

DC Recommended Operating Conditions

(T_a=0 to +70°C, GND=0V)

Item	Symbol	Min.	Typ.*	Max.	Unit
Power Supply Voltage	V _{CC}	4.5	5.0	5.5	V
Input High Voltage	V _{IH}	2.2	—	V _{CC} +0.3	V
Input Low Voltage	V _{IL}	-0.3**	—	0.8	V

* V_{CC}=5V, T_a=25°C

** V_{IL} min=-3.0V for pulse width less than 20 ns.

DC and Operating Characteristics

(V_{CC}=5V±10%, GND=0V, T_a=0 to +70°C)

Item	Symbol	Test condition	CXK5416P -35/45/55			CXK5416P -35L/45L/55L			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Leakage Current	I _{LI}	V _{IN} =GND to V _{CC} V _{CC} =5.5V	-2	—	2	-2	—	2	μA
Output Leakage Current	I _{LO}	\overline{CE} =V _{IH} V _{I/O} =GND to V _{CC}	-2	—	2	-2	—	2	μA
Operating Power Supply Current	I _{CC1}	\overline{CE} =V _{IL} , I _{OUT} =0 mA V _{IN} =V _{IH} /V _{IL}	—	40	70	—	40	70	mA
Average Operating Current	I _{CC2}	Cycle=Min, Duty=100% I _{OUT} =0 mA	—	60	100	—	60	100	mA
Standby Current	I _{SB1}	$\overline{CE} \geq V_{CC} - 0.2V$, V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V	—	0.02	1.0	—	0.001	0.05	mA
	I _{SB2}	\overline{CE} =V _{IH}	—	10	20	—	10	20	mA
Output High Voltage	V _{OH}	I _{OH} =-4.0 mA	2.4	—	—	2.4	—	—	V
Output Low Voltage	V _{OL}	I _{OL} =8.0 mA	—	—	0.4	—	—	0.4	V

Capacitance

(T_a=25°C, f=1 MHz)

Item		Test Condition	Symbol	Min.	Max.	Unit
Input Capacitance	A ₀ to A ₁₁ , \overline{WE}	V _{IN} =0V	C _{IN}	—	5	pF
	\overline{CE}			—	7	
Input/Output Capacitance		V _{I/O} =0V	C _{I/O}	—	7	pF

Note) This parameter is sampled and is not 100% tested.

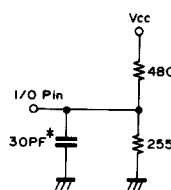
AC Operating Characteristics

• AC Test condition

(V_{CC}=5V±10%, T_a=0 to +70°C)

Item	Condition
Input Pulse High Level	V _{IH} =3.0V
Input Pulse Low Level	V _{IL} =0V
Input Rise Time	t _r =5 ns
Input Fall Time	t _f =5 ns
Input and Output Timing Reference Level	1.5V
Output Load	Fig. 1

Output Load (1)



Output Load (2)**

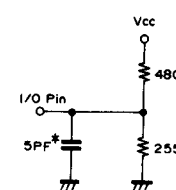
* including scope and jig
** for t_{LZ}, t_{HZ}, t_{OW}, t_{WHZ}

Fig. 1

Read Cycle

Item	Symbol	CXXK5416P -35/35L		CXXK5416P -45/45L		CXXK5416P -55/55L		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t _{RC}	35	—	45	—	55	—	ns
Address Access Time	t _{AA}	—	35	—	45	—	55	ns
Chip Enable Access Time (\overline{CE})	t _{CO}	—	35	—	45	—	55	ns
Output Hold from Address Change	t _{OH}	5	—	5	—	5	—	ns
Chip Enable to Output in Low Z (\overline{CE})	t _{LZ} *	10	—	10	—	15	—	ns
Chip Disable to Output in High Z (\overline{CE})	t _{HZ} *	0	20	0	20	0	20	ns
Chip Enable to Power Up Time	t _{PU}	0	—	0	—	0	—	ns
Chip Disable to Power Down Time	t _{PD}	—	30	—	30	—	30	ns

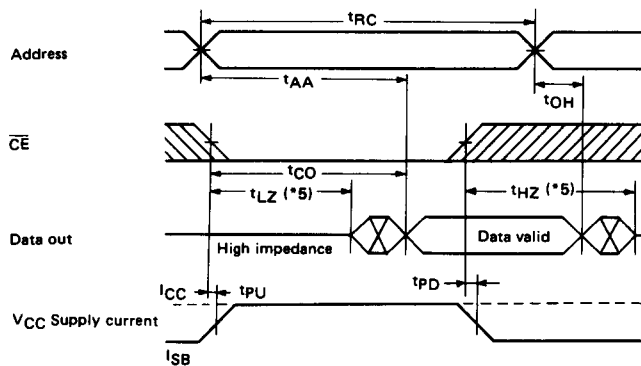
Write Cycle

Item	Symbol	CXXK5416P -35/35L		CXXK5416P -45/45L		CXXK5416P -55/55L		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	t _{WC}	35	—	45	—	55	—	ns
Address Valid to End of Write	t _{AW}	30	—	35	—	45	—	ns
Chip Enable to End of Write	t _{CW}	30	—	35	—	45	—	ns
Data to Write Time Overlap	t _{DW}	15	—	20	—	25	—	ns
Data Hold from Write Time	t _{DH}	0	—	0	—	0	—	ns
Write Pulse Width	t _{WP}	30	—	35	—	45	—	ns
Address Setup Time	t _{AS}	0	—	0	—	0	—	ns
Write Recovery Time	t _{WR}	0	—	0	—	0	—	ns
Output Active from End of Write	t _{OW} *	5	—	5	—	5	—	ns
Write to Output in High Z	t _{WHZ} *	0	15	0	15	0	20	ns

* Transition is measured ± 500 mV from steady voltage with specified loading in Fig. 1. This parameter is sampled and not 100% tested.

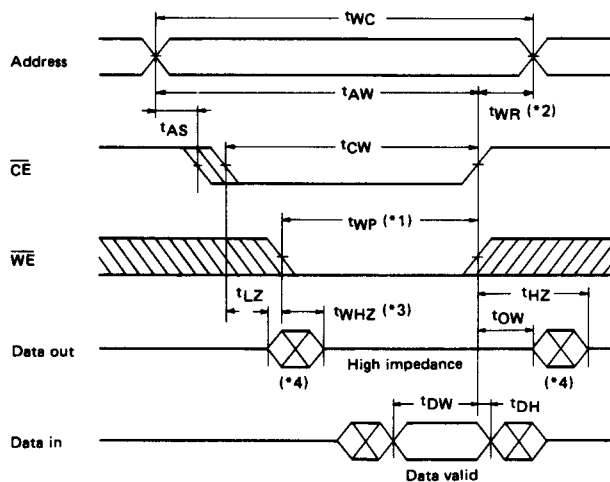
Timing Waveform

(1) Read Cycle [$\overline{WE}=V_{IH}$]

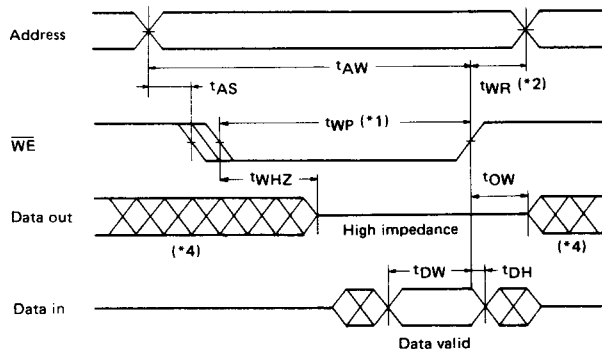


(2) Write Cycle

• Write Cycle No.1



- Write Cycle No.2: [$\overline{CE}=V_{IL}$]



*** Note)**

1. A write occurs during the low overlap of \overline{CE} and \overline{WE} .
2. t_{WR} is measured from the earlier of \overline{CE} or \overline{WE} going high to the end of write cycle.
3. If \overline{CE} low transition occurs simultaneously with the \overline{WE} low transition or after the \overline{WE} transition, output remains in a high impedance state.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the output must not be applied.
5. At any conditions, t_{HZ} is less than t_{LZ} .

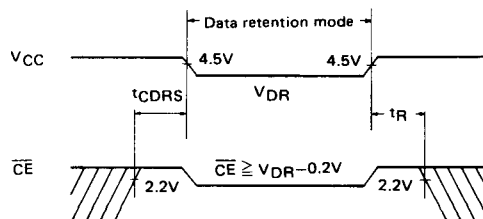
Data Retention Characteristics

($T_a=0$ to $+70^\circ\text{C}$)

Item	Symbol	Test condition	CXK5416P -35/45/55			CXK5416P -35L/45L/55L			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Data Retention Voltage	V_{DR}	$\overline{CE} \geq V_{CC} - 0.2V$	2.0	5.0	5.5	2.0	5.0	5.5	V
Data Retention Current	I_{CCDR1}	$\overline{CE} \geq V_{CC} - 0.2V$, $V_{CC}=3.0V$		12	600		0.6	30	μA
	I_{CCDR2}	$V_{IN} \leq 0.2V$ or $V_{CC}=2.0$ $V_{IN} \geq V_{CC} - 0.2V$ to 5.5V		20	1000		1.0	50	μA
Data Retention Set up Time	t_{CDRS}	Chip disable to data retention mode	0			0			ns
Recovery Time	t_R		t_{RC}^*			t_{RC}^*			ns

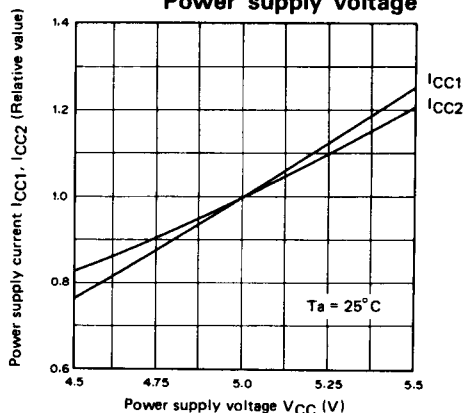
* t_{RC} : Read Cycle Time

Data Retention Waveform

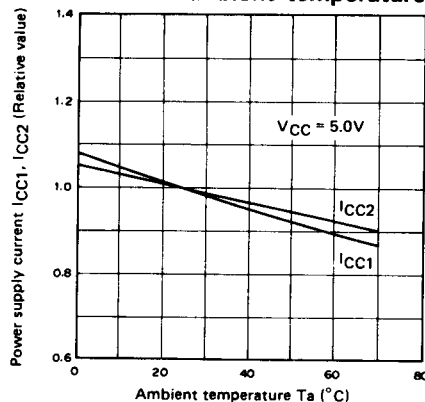


www.DataSheet4U.com

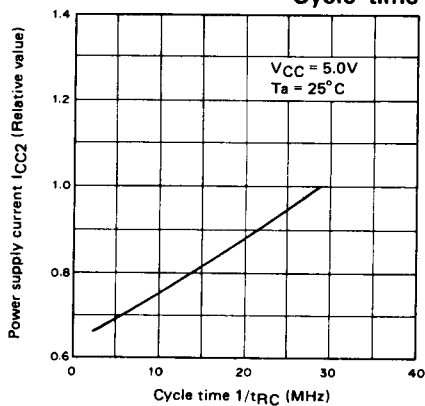
Power supply current vs. Power supply voltage



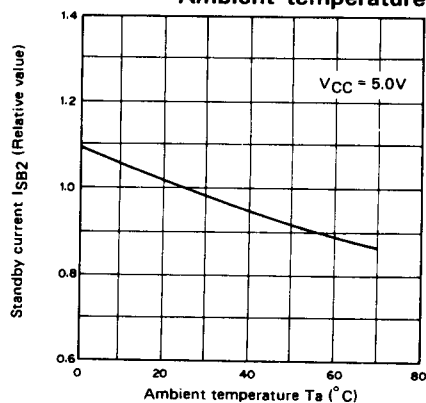
Power supply current vs. Ambient temperature



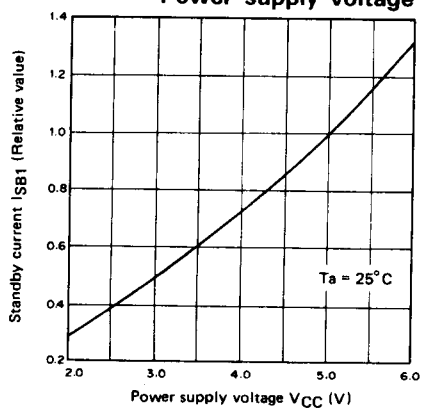
Power supply current vs. Cycle time



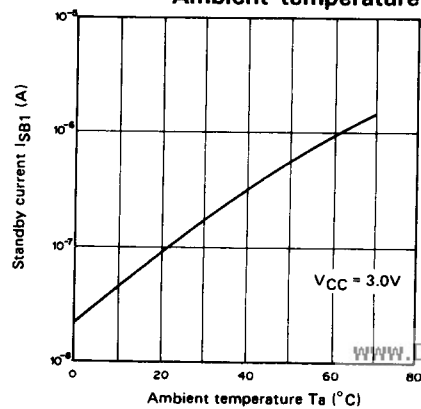
Standby current vs. Ambient temperature



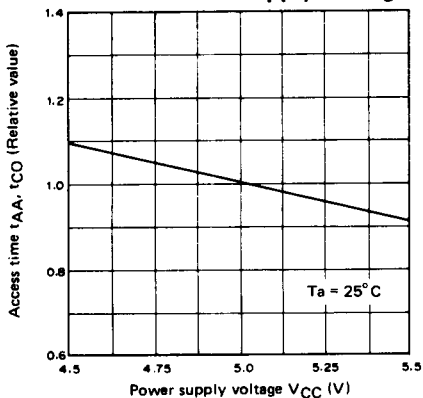
Standby current vs. Power supply voltage



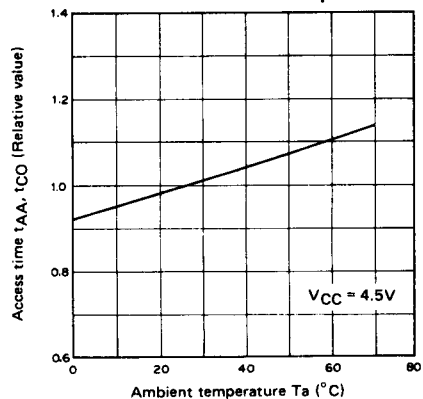
Standby current vs. Ambient temperature



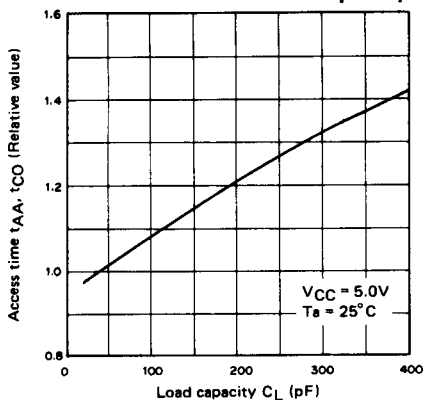
Access time vs.
Power supply voltage



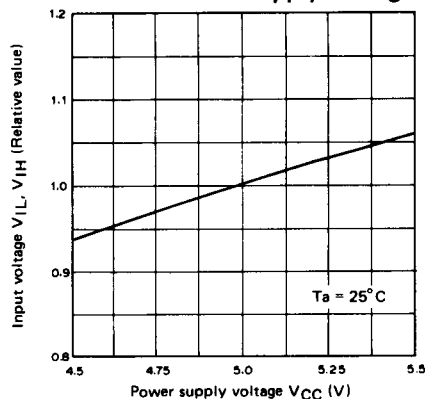
Access time vs.
Ambient temperature



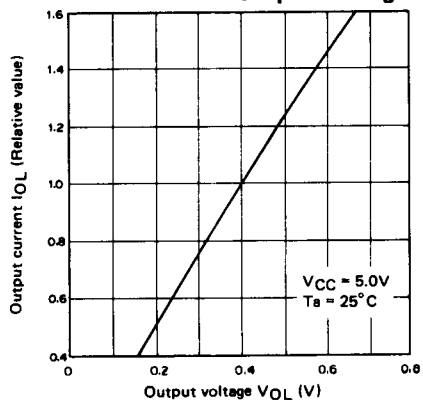
Access time vs.
Load capacity



Input voltage vs.
Power supply voltage



Output current vs.
Output voltage



Output current vs.
Output voltage

