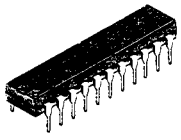
SONY CXK5464AP/AJ 25/30/35

16,384-word × 4-bit High Speed CMOS Static RAM

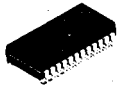
Description

CXK5464AP/AJ are 65,536 bits high speed CMOS static RAMs organized as 16,384 words by 4 bits and operate from a single 5V supply.

CXK5464AP
22 pin DIP (Plastic)



CXK5464AJ
24 pin SOJ (Plastic)



Features

- Fast access time :
  - CXK5464AP/AJ-25 25ns (Max.)
  - CXK5464AP/AJ-30 30ns (Max.)
  - CXK5464AP/AJ-35 35ns (Max.)
- Low power operation : 125mW (Typ.)
- Single + 5V supply : + 5V ± 10%
- Fully static memory...No clock or timing strobe required.
- Equal access and cycle time.
- Common data input and output : Three-state output
- Directly TTL compatible : All inputs and outputs.
- High density : 300mil 22 pin plastic DIP
  300mil 24 pin plastic SOJ

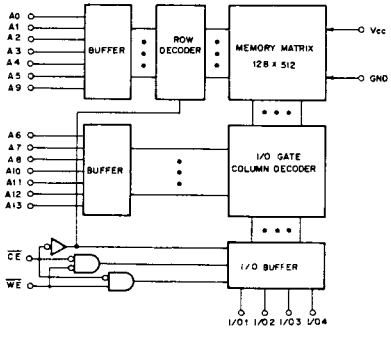
Function

16,384-word × 4-bit static RAM

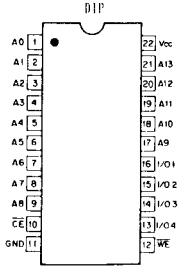
Structure

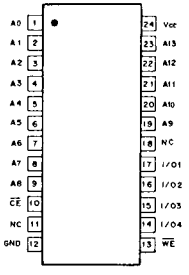
Silicon gate CMOS IC

Block Diagram



Pin Configuration (Top view)





Pin Description

Symbol	Description
A0 to A13	Address input
I/O1 to I/O4	Data input output
$\overline{CE}$	Chip enable input
$\overline{WE}$	Write enable input
Vcc	+ 5V Power supply
GND	Ground
NC	Non connection

3

Absolute Maximum Ratings (Ta = 25℃, GND = 0V)

Item	Symbol	Rating	Unit
Supply voltage	V_{CC}	− 0.5* to + 7.0	V
Input voltage	V_{IN}	− 0.5* to V_{CC} + 0.5	V
Input and output voltage	$V_{I/O}$	− 0.5* to V_{CC} + 0.5	V
Operating temperature	Topr	0 to + 70	℃
Storage temperature	Tstg	− 55 to + 150	℃
Soldering temperature	Tsolder	260 • 10	℃ • sec
Allowable power dissipation	P_D	1.0	W

* V_{CC}, V_{IN}, $V_{I/O}$ = − 3.5V Min. for pulse width less than 20ns.

Truth Table

$\overline{CE}$	$\overline{WE}$	Mode	I/O1 to I/O4	V_{CC} Current
H	X	Not selected	High Z	I_{SB1}, I_{SB2}
L	H	Read	Data out	I_{CC1}, I_{CC2}
L	L	Write	Data in	I_{CC1}, I_{CC2}

X : "H" or "L"

DC Recommended Operating Conditions (Ta = 0 to + 70℃, GND = 0V)

Item	Symbol	Min.	Typ.*1	Max.	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input low voltage	V_{IL}	− 0.3*2	—	0.8	V

*1. V_{CC} = 5V, Ta = 25℃

*2. V_{IL} = − 3.0V Min. for pulse width less than 20ns.

Electrical Characteristics

• DC and operating characteristics (Vcc = 5V ± 10%, GND = 0V, Ta = 0 to +70°C)

Item	Symbol	Test conditions	−25/30/35			Unit
			Min.	Typ.*	Max.	
Input leak current	I_{LI}	V_{IN} = GND to V_{CC}	−1	—	1	μA
Output leak current	I_{LO}	$\overline{CE}$ = V_{IH} or $\overline{WE}$ = V_{IL} $V_{I/O}$ = GND to V_{CC}	−1	—	1	μA
Operating supply current	I_{CC1}	$\overline{CE}$ = V_{IL}, I_{OUT} = 0mA V_{IN} = V_{IH}/V_{IL}	—	25	45	mA
Average operating current	I_{CC2}	Cycle = Min., Duty = 100% I_{OUT} = 0mA	—	60	90	mA
Standby current	I_{SB1}	$\overline{CE}$ ≧ V_{CC} − 0.2V, V_{IN} ≧ V_{CC} − 0.2V or V_{IN} ≦ 0.2V	—	—	1	mA
	I_{SB2}	$\overline{CE}$ = V_{IH}	—	15	30	mA
Output high voltage	V_{OH}	I_{OH} = −4.0mA	2.4	—	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0mA	—	—	0.4	V

* V_{CC} = 5.0V, Ta = 25°C

I/O capacitance (Ta = 25°C, f = 1MHz)

Item	Symbol	Test conditions	Min.	Max.	Unit
Input capacitance	C_{IN}	V_{IN} = 0V	—	7	pF
Input/Output capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	—	7	pF

Note) This parameter is sampled and is not 100% tested.

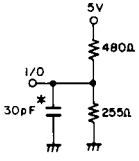
AC characteristics

• AC test conditions

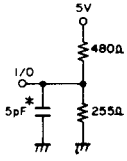
(Vcc = 5V ± 10%, Ta = 0 to +70°C)

Item	Conditions
Input pulse high level	V_{IH} = 3.0V
Input pulse low level	V_{IL} = 0V
Input rise time	tr = 5ns
Input fall time	tf = 5ns
Input and output reference level	1.5V
Output load conditions	Fig. 1

Output Load (1)



Output Load (2)**



* including scope and jig

** for t_{LZ}, t_{HZ}, t_{OW}, t_{WHZ}

Fig. 1

● **Read cycle**

Item	Symbol	−25		−30		−35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	25	—	30	—	35	—	ns
Address access time	t_{AA}	—	25	—	30	—	35	ns
Chip enable access time ($\overline{CE}$)	t_{CO}	—	25	—	30	—	35	ns
Output hold from address change	t_{OH}	5	—	5	—	5	—	ns
Chip enable to output in low Z ($\overline{CE}$)	t_{LZ}*	5	—	5	—	5	—	ns
Chip disable to output in high Z	t_{HZ}*	0	10	0	15	0	15	ns
Chip enable to power up time	t_{PU}	0	—	0	—	0	—	ns
Chip enable to power down time	t_{PD}	—	20	—	25	—	25	ns

* Transition is measured ±200mV from steady voltage with specified loading in Fig. 1. This parameter is sampled and is not 100% tested.

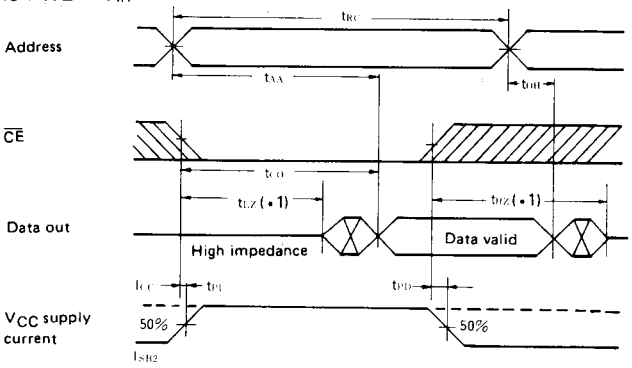
● **Write cycle**

Item	Symbol	−25		−30		−35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	25	—	30	—	35	—	ns
Address valid to end of write	t_{AW}	20	—	25	—	30	—	ns
Chip enable to end of write	t_{CW}	20	—	25	—	30	—	ns
Data to write time overlap	t_{DW}	12	—	15	—	15	—	ns
Data hold from write time	t_{DH}	0	—	0	—	0	—	ns
Write pulse width	t_{WP}	20	—	25	—	30	—	ns
Address setup time	t_{AS}	0	—	0	—	0	—	ns
Write recovery time	t_{WR}	0	—	0	—	0	—	ns
Output active from end of write	t_{OW}*	5	—	5	—	5	—	ns
Write to output in high Z	t_{WHZ}*	0	10	0	10	0	15	ns

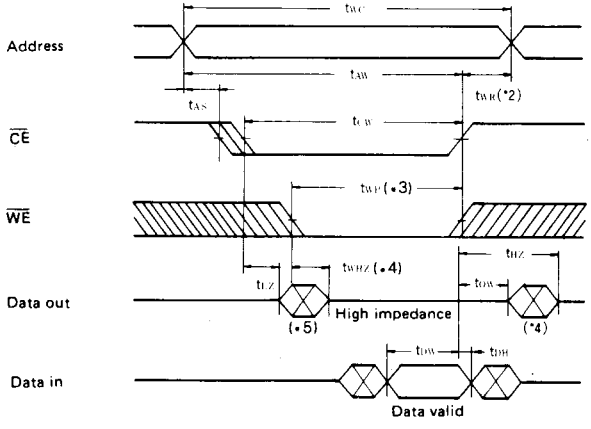
* Transition is measured ±200mV from steady voltage with specified loading in Fig. 1. This parameter is sampled and is not 100% tested.

Timing Waveform

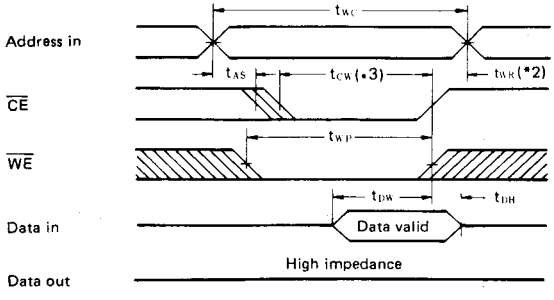
• Read cycle : $\overline{WE}$ = V_{IH}



• Write cycle (1) : $\overline{WE}$ control



• Write cycle (2) : $\overline{CE}$ control

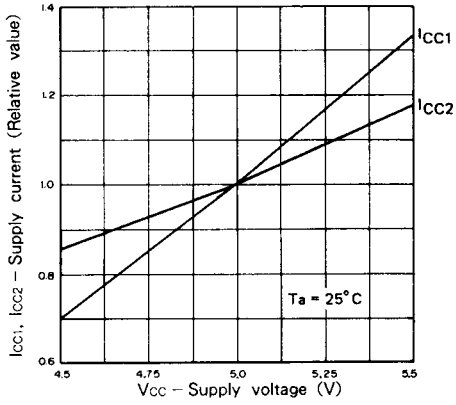


***Note)**

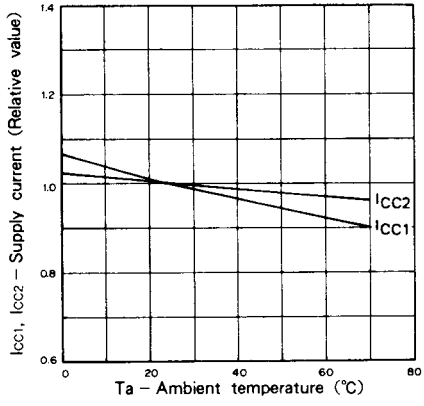
1. At any conditions, t_{HZ} is less than t_{LZ}.
2. t_{WR} is measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high to the end of write cycle.
3. A write occurs during the low overlap of $\overline{CE}$ and $\overline{WE}$.
4. If $\overline{CE}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, output remains in a high impedance state.
5. During this period, I/O pins are in the output state so that the input signals of opposite phase to the output must not be applied.

Example of Representative Characteristics

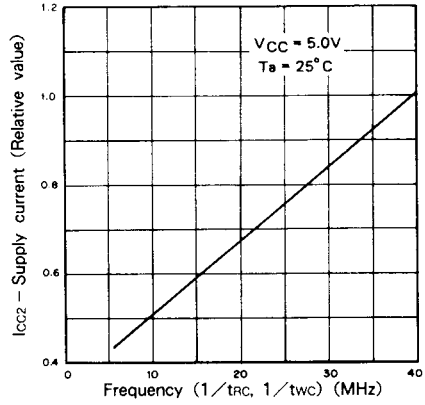
Supply current vs. Supply voltage



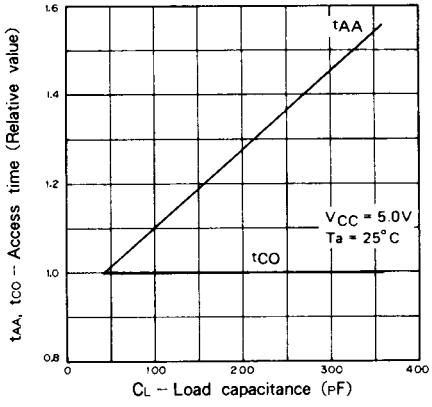
Supply current vs. Ambient temperature



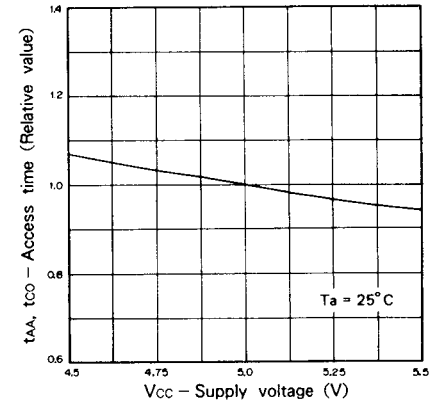
Supply current vs. Frequency



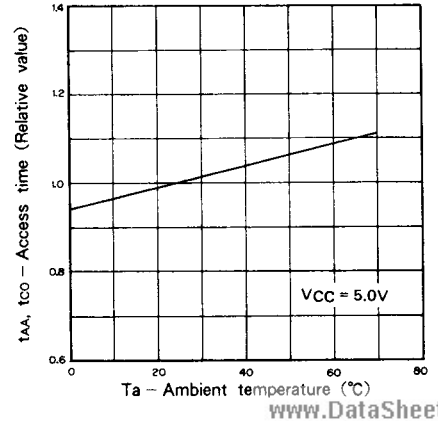
Access time vs. Load capacitance



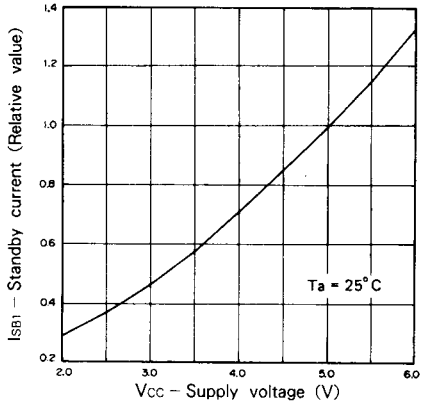
Access time vs. Supply voltage



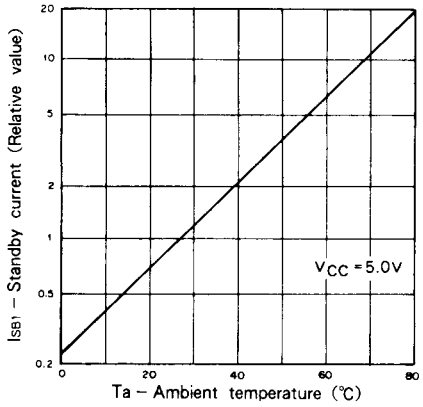
Access time vs. Ambient temperature



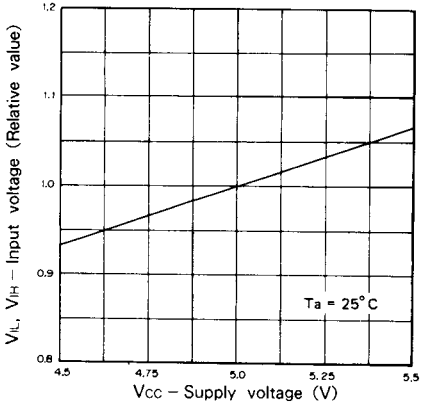
Standby current vs. Supply voltage



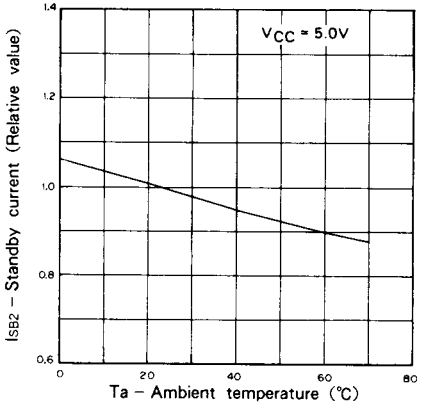
Standby current vs. Ambient temperature



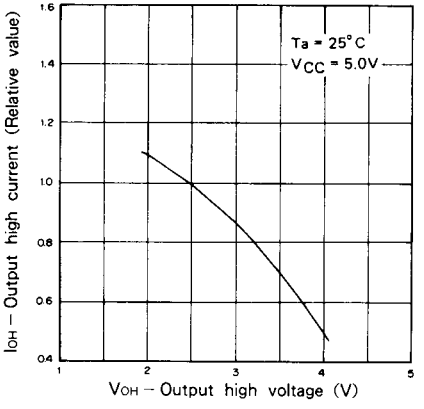
Input voltage level vs. Supply voltage



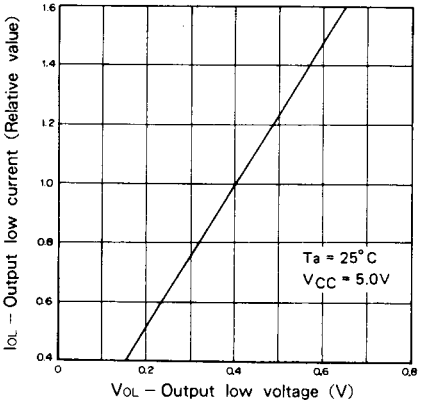
Standby current vs. Ambient temperature



Output high current vs. Output high voltage



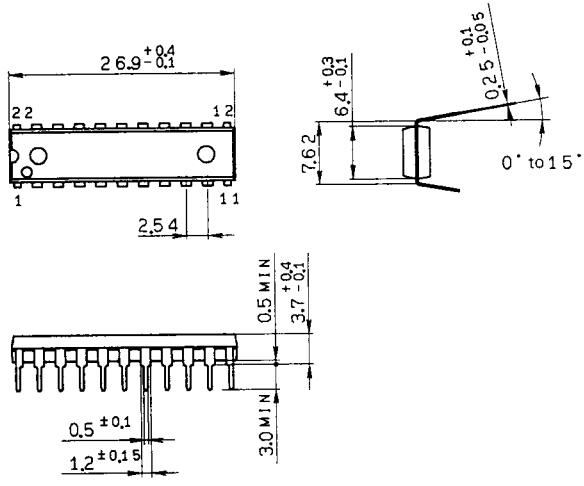
Output low current vs. Output low voltage



3

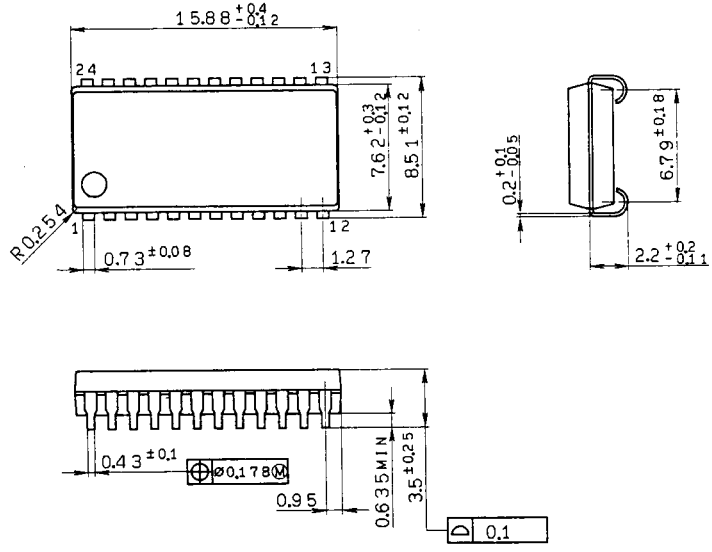
Package Outline Unit : mm

CXK5464AP 22 pin DIP (Plastic) 300mil 1.3g



DIP-22P-02

CXK5464AJ 24 pin SOJ (Plastic) 300mil 0.7g



SOJ-24P-01