

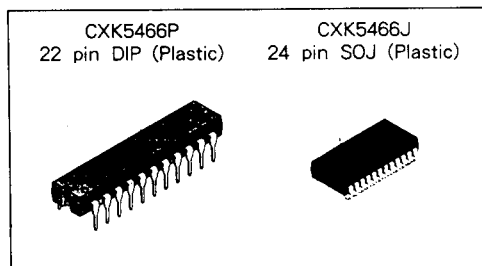
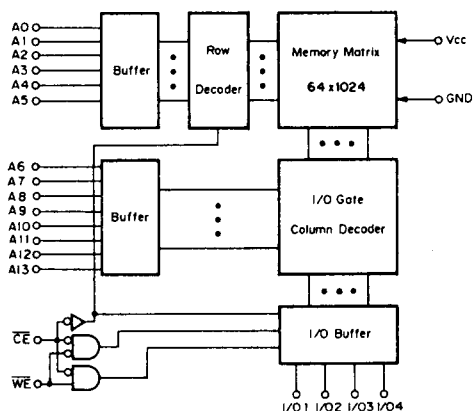
**SONY****CXK5466P/J** -15/20**16,384 word × 4-bit High Speed CMOS Static RAM****Description**

CXK5466P/J is a high speed CMOS static RAM with TTL compatible I/O organized as 16,384 words × 4 bits.

This IC operating on a single 5V supply turns to power down mode at no select time by means of chip enable signal.

**Features**

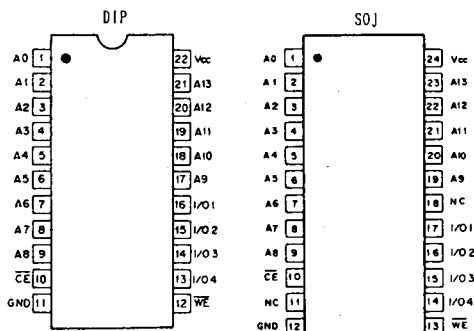
- Fast access time :  
CXK5466P/J-15 15ns (Max.)  
CXK5466P/J-20 20ns (Max.)
- Low power consumption : 150mW (Typ.)  
During operation
- Single +5V supply : +5V ± 10%
- Fully static memory  
...No clock or timing strobe required
- Equal access and cycle time
- Common data input and output :  
three-state output
- Directly TTL compatible :  
All inputs and outputs
- Compatible with various types of packages
- High density : 300 mil 22 pin plastic DIP  
300 mil 24 pin plastic SOJ

**Block Diagram****Functions**

16,384 word × 4-bit static RAM

**Structure**

Silicon gate CMOS IC

**Pin Configuration (Top View)****Pin Description**

Symbol	Description
A0 to A13	Address input
I/O1 to I/O4	Data input/output
CE	Chip enable input
WE	Write enable input
Vcc	+5V power supply
GND	Ground
NC	No connection

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## Absolute Maximum Ratings

(Ta = 25°C, GND = 0V)

Item	Symbol	Ratings	Unit
Supply voltage	V <sub>CC</sub>	- 0.5 * to + 7.0	V
Input voltage	V <sub>IN</sub>	- 0.5 * to V <sub>CC</sub> + 0.5	V
Input and output voltage	V <sub>I/O</sub>	- 0.5 * to V <sub>CC</sub> + 0.5	V
Allowable power dissipation	P <sub>D</sub>	1.0	W
Operating temperature	T <sub>opr</sub>	0 to + 70	°C
Storage temperature	T <sub>stg</sub>	- 55 to + 150	°C
Soldering temperature * time	T <sub>solder</sub>	260 * 10	°C * sec

\* V<sub>CC</sub>, V<sub>IN</sub>, V<sub>I/O</sub> Min. = - 3.5V for pulse width less than 20ns.

## Truth Table

CE	WE	Mode	I/O1 to I/O4	V <sub>CC</sub> current
H	X	Not selected	High Z	I <sub>SB1</sub> , I <sub>SB2</sub>
L	H	Read	Data output	I <sub>CC1</sub> , I <sub>CC2</sub>
L	L	Write	Data input	I <sub>CC1</sub> , I <sub>CC2</sub>

X : "H" or "L"

## DC Recommended Operating Conditions (Ta = 0 to + 70°C, GND = 0V)

Item	Symbol	Min.	Typ.*1	Max.	Unit
Supply voltage	V <sub>CC</sub>	4.5	5.0	5.5	V
Input high voltage	V <sub>IH</sub>	2.2	—	V <sub>CC</sub> + 0.3	V
Input low voltage	V <sub>IL</sub>	- 0.3*2	—	0.8	V

\*1) V<sub>CC</sub> = 5V, Ta = 25°C\*2) V<sub>IL</sub> Min. = - 3.0V for pulse width less than 20ns.

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## DC Electrical Characteristics

## • DC and operating characteristics

(V<sub>CC</sub> = 5V ± 10%, GND = 0V, T<sub>a</sub> = 0 to +70°C)

Item	Symbol	Test Conditions	Min.	Typ.*	Max.	Unit	
Input leak current	I <sub>LI</sub>	V <sub>IN</sub> = GND to V <sub>CC</sub>	-1	—	1	μA	
Output leak current	I <sub>LO</sub>	$\overline{CE} = V_{IH}$ or $\overline{WE} = V_{IL}$ V <sub>I/O</sub> = GND to V <sub>CC</sub>	-1	—	1	μA	
Operating power supply current	I <sub>CC1</sub>	$\overline{CE} = V_{IL}$ , I <sub>OUT</sub> = 0mA, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	—	30	55	mA	
Average operating current	I <sub>CC2</sub>	Cycle = Min., Duty = 100%, I <sub>OUT</sub> = 0mA	-15	—	95	150	mA
			-20	—	90	140	mA
Standby current	I <sub>SB1</sub>	$\overline{CE} \geq V_{CC} - 0.2V$ , V <sub>IN</sub> $\geq V_{CC} - 0.2V$ or V <sub>IN</sub> $\leq 0.2V$	—	—	1	mA	
	I <sub>SB2</sub>	$\overline{CE} = V_{IH}$ , V <sub>IN</sub> = V <sub>IH</sub> /V <sub>IL</sub> Cycle = Min.	—	—	85	mA	
Output high voltage	V <sub>OH</sub>	I <sub>OH</sub> = -4.0mA	2.4	—	—	V	
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> = 8.0mA	—	—	0.4	V	

\* V<sub>CC</sub> = 5.0V, T<sub>a</sub> = 25°C

## I/O capacitance

(T<sub>a</sub> = 25°C, f = 1MHz)

Item	Symbol	Test Conditions	Min.	Max.	Unit
Input capacitance	C <sub>IN</sub>	V <sub>IN</sub> = 0V	—	7	pF
Input/output capacitance	C <sub>I/O</sub>	V <sub>I/O</sub> = 0V	—	7	pF

**Note)** This parameter is sampled and is not 100% tested.

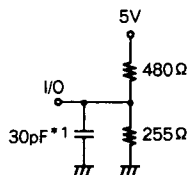
## AC characteristics

## • AC test conditions

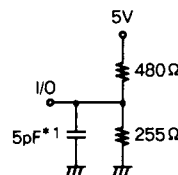
(V<sub>CC</sub> = 5V ± 10%, T<sub>a</sub> = 0 to +70°C)

Item	Conditions
Input pulse high level	V <sub>IH</sub> = 3.0V
Input pulse low level	V <sub>IL</sub> = 0V
Input rise time	t <sub>r</sub> = 5ns
Input fall time	t <sub>f</sub> = 5ns
Input and output reference level	1.5V
Output load conditions	Fig. 1

## Output Load (1)



## Output Load (2)\*2



\*1 including scope and jig capacitance

\*2 for t<sub>LZ</sub>, t<sub>HZ</sub>, t<sub>OW</sub>, t<sub>WHZ</sub>

Fig. 1

## • Read cycle

Item	Symbol	- 15		- 20		Unit
		Min.	Max.	Min.	Max.	
Read cycle time	t <sub>RC</sub>	15	—	20	—	ns
Address access time	t <sub>AA</sub>	—	15	—	20	ns
Chip enable access time ( $\overline{CE}$ )	t <sub>CO</sub>	—	15	—	20	ns
Output hold from address change	t <sub>OH</sub>	3	—	3	—	ns
Chip enable to output in low Z ( $\overline{CE}$ )	t <sub>LZ</sub> *	2	—	3	—	ns
Chip disable to output in high Z	t <sub>HZ</sub> *	0	6	0	8	ns
Chip enable to power up time	t <sub>PU</sub>	0	—	0	—	ns
Chip disable to power down time	t <sub>PD</sub>	—	15	—	20	ns

\* Transition is tested by means of load conditions (2), from stationary condition at  $\pm 200\text{mV}$  (See Fig. 1)

## • Write cycle

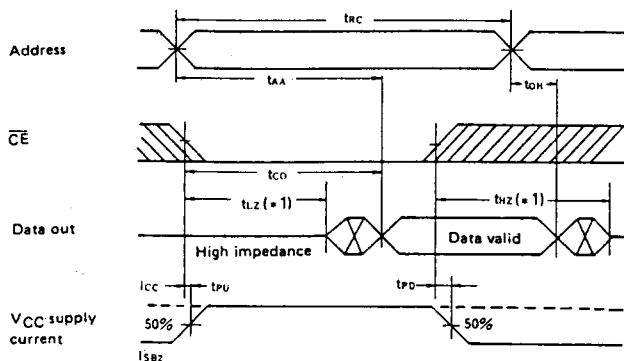
Item	Symbol	- 15		- 20		Unit
		Min.	Max.	Min.	Max.	
Write cycle time	t <sub>WC</sub>	15	—	20	—	ns
Address valid to end of write	t <sub>AW</sub>	13	—	18	—	ns
Chip enable to end of write	t <sub>CW</sub>	13	—	18	—	ns
Data to write time overlap	t <sub>DW</sub>	8	—	11	—	ns
Data hold from write time	t <sub>DH</sub>	0	—	0	—	ns
Write pulse width	t <sub>WP</sub>	13	—	18	—	ns
Address setup time	t <sub>AS</sub>	0	—	0	—	ns
Write recovery time	t <sub>WR</sub>	0	—	0	—	ns
Output active from end of write	t <sub>OW</sub> *	2	—	3	—	ns
Write to output in high Z	t <sub>WHZ</sub> *	0	5	0	7	ns

\* Transition is tested by means of load conditions (2), from stationary condition at  $\pm 200\text{mV}$  (See Fig. 1)

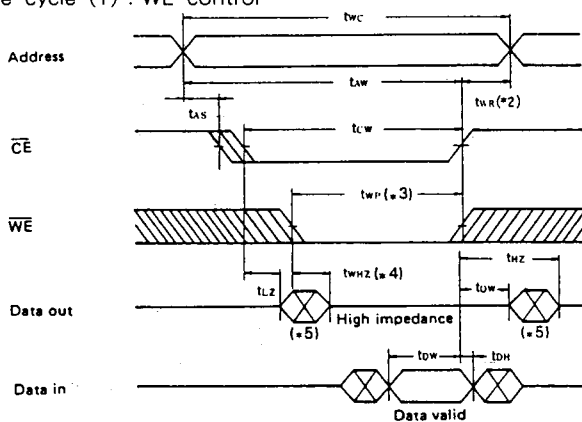
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### Timing Waveform

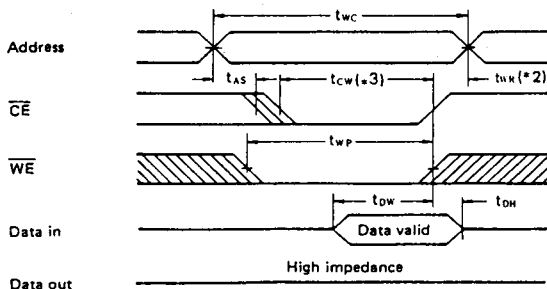
- Read cycle :  $\overline{WE} = V_{IH}$



- Write cycle (1) :  $\overline{WE}$  control



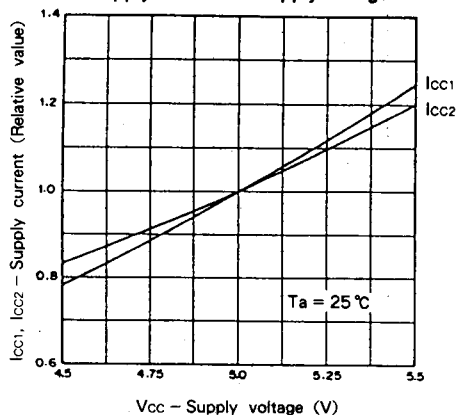
- Write cycle (2) :  $\overline{CE}$  control



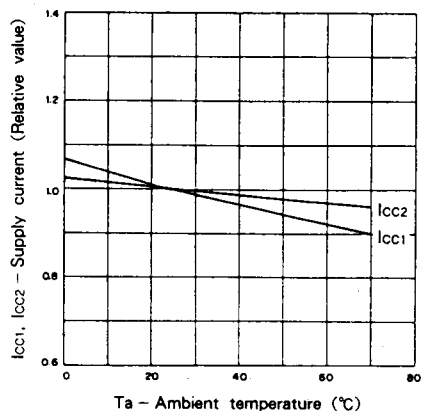
- \*1) Whatever the conditions,  $t_{HZ}$  is smaller than  $t_{LZ}$ .
- \*2)  $t_{WR}$  is tested from either  $\overline{CE}$  or  $\overline{WE}$  rise, whichever comes earlier, until the end of write cycle.
- \*3) Write is performed when both  $\overline{CE}$  and  $\overline{WE}$  are in the low overlap.
- \*4) When  $\overline{WE}$  fall is performed simultaneously with  $\overline{CE}$  fall, or before, output is kept to high impedance.
- \*5) While I/O pins are in output state, do not apply data input signals with a phase opposite to that of the output.

## Example of Representative Characteristics

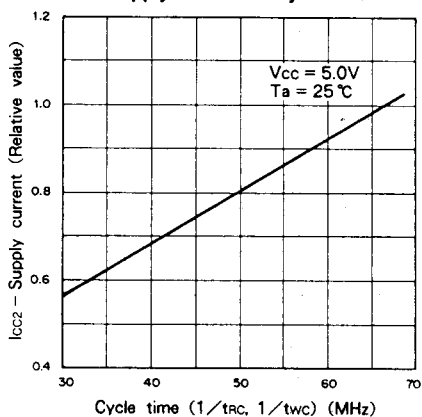
Supply current vs. Supply voltage



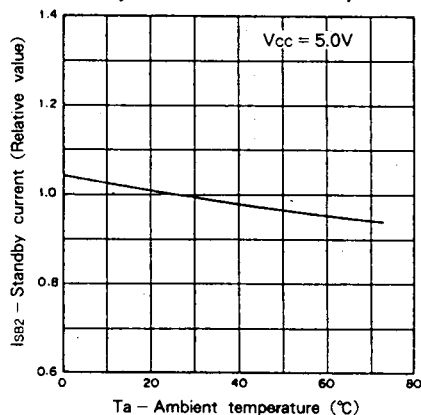
Supply current vs. Ambient temperature



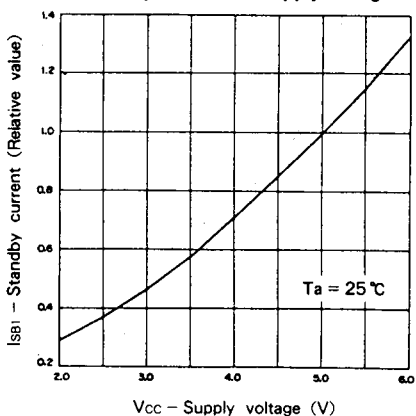
Supply current vs. Cycle time



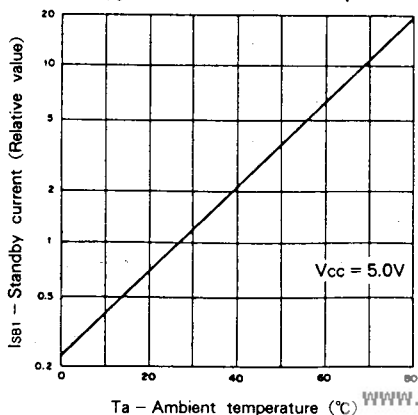
Standby current vs. Ambient temperature



Standby current vs. Supply voltage

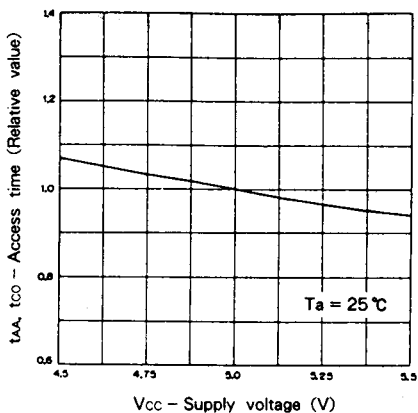


Standby current vs. Ambient temperature

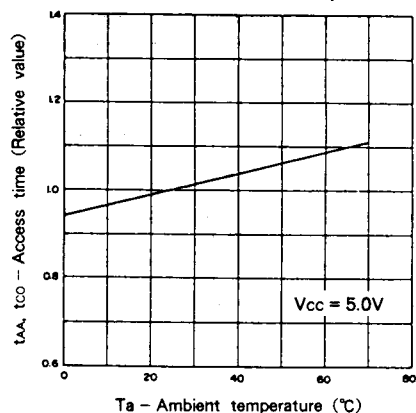


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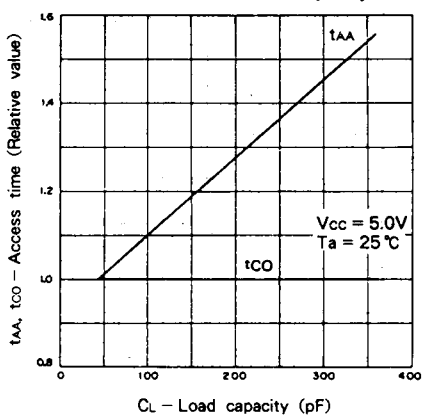
Access time vs. Supply voltage



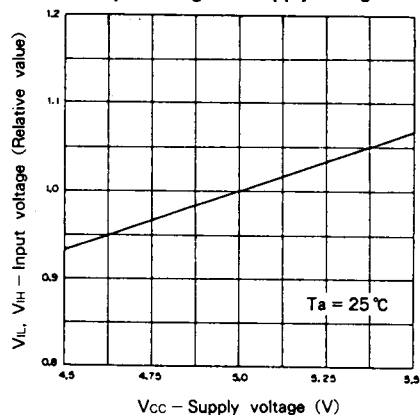
Access time vs. Ambient temperature



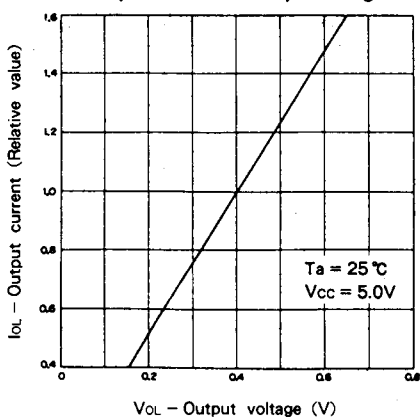
Access time vs. Load capacity



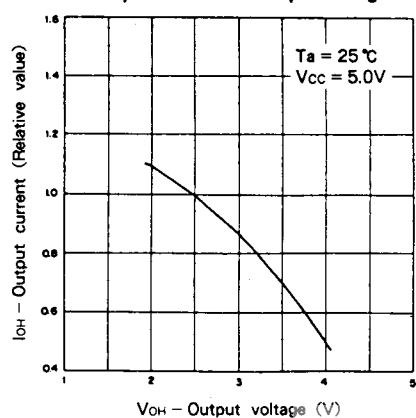
Input voltage vs. Supply voltage



Output current vs. Output voltage

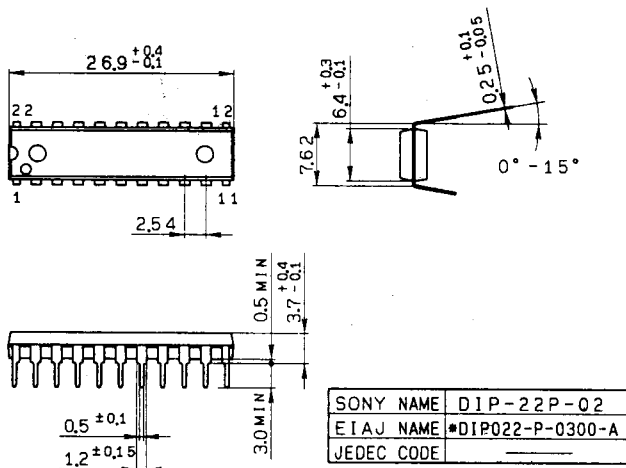


Output current vs. Output voltage

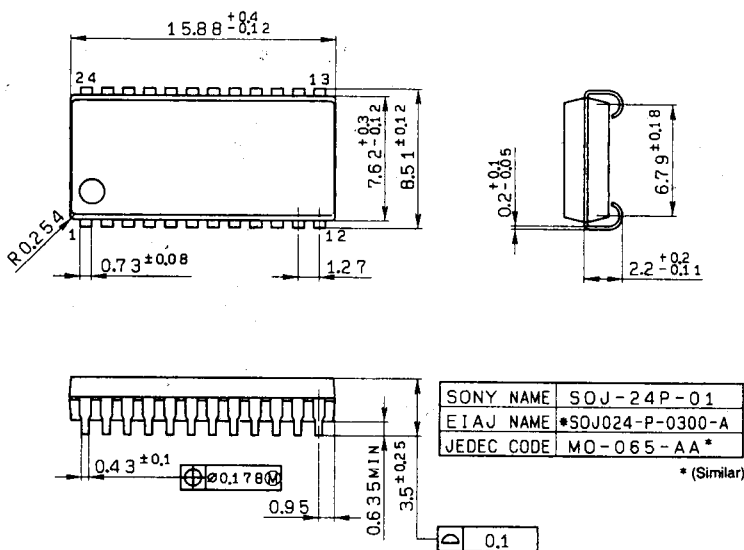


**Package Outline** Unit : mm

CXK5466P 22 pin DIP (Plastic) 300mil 1.3g



CXK5466J 24 pin SOJ (Plastic) 300mil 0.7g



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