SONY CXK581000P/M -10L/12L/15L -10LL/12LL/15LL

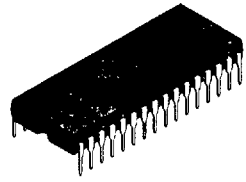
131072-word × 8-bit High Speed CMOS Static RAM

SONY CORP/COMPONENT PRODS

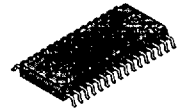
Description

CXK581000P/M is a general purpose high speed CMOS static RAM organized as 131, 072 words by 8 bits. Operating on a single 5V supply, this asynchronous IC is suitable for high speed and low power consumption applications where battery back up for nonvolatility is required.

CXK581000P
32 pin DIP (Plastic)



CXK581000M
32 pin SOP (Plastic)



Features

- Fast access time : (Access time)
  CXK581000P/M-10L/10LL 100ns (Max.)
  CXK581000P/M-12L/12LL 120ns (Max.)
  CXK581000P/M-15L/15LL 150ns (Max.)
- Low power consumption operation :

	Standby	/DC operation
CXK581000P/M-10L, 12L, 15L ;	10 µW (Typ.)	/35mW (Typ.)
10LL, 12LL, 15LL ;	3.5 µW (Typ.)	/35mW (Typ.)

- Single +5V supply : +5V ± 10%
- Fully static memory ··· No clock or timing strobe required.
- Equal access and cycle time.
- Common data input and output:three state output.
- Directly TTL compatible : All inputs and outputs.
- Low voltage data retention : 2.0V (Min.)
- CXK581000P 600mil 32 pin DIP package
  CXK581000M 525mil 32 pin SOP package

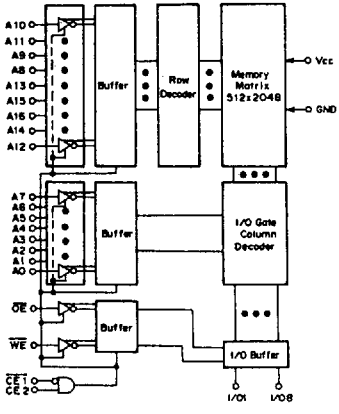
Functions

131,072 word × 8 bit static RAM

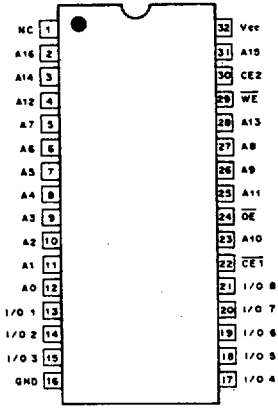
Structure

Silicon gate CMOS IC

Block Diagram



Pin Configuration (Top View)



Pin Description

Symbol	Description
A0 to A16	Address input
I/O1 to I/O8	Data input output
$\overline{CE1}$, CE2	Chip enable 1, 2 input
$\overline{WE}$	Write enable input
$\overline{OE}$	Output enable input
Vcc	Power supply
GND	Ground
NC	No connection

Absolute Maximum Ratings (Ta=25 °C, GND=0V)

Item	Symbol		Rating	Unit
Supply voltage	V_{CC}		− 0.5 to +7.0	V
Input voltage	V_{IN}		− 0.5 * to V_{CC}+0.5	V
Input and output voltage	$V_{I/O}$		− 0.5 * to V_{CC}+0.5	V
Allowable power dissipation	P_D	CXK581000P	1.0	W
		CXK581000M	0.7	
Operating temperature	Topr		0 to +70	°C
Storage temperature	Tstg		− 55 to +150	°C
Soldering temperature	Tsolder		260•10	°C • sec

* V_{IN}, $V_{I/O}$= − 3.0V Min. for pulse width less than 50ns.

Truth Table

$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	Mode	I/O pin	V_{CC} current
H	×	×	×	Not selected	High Z	I_{SB1}, I_{SB2}
×	L	×	×	Not selected	High Z	I_{SB1}, I_{SB2}
L	H	H	H	Output disable	High Z	I_{CC1}, I_{CC2}, I_{CC3}
L	H	L	H	Read	Data out	I_{CC1}, I_{CC2}, I_{CC3}
L	H	×	L	Write	Data in	I_{CC1}, I_{CC2}, I_{CC3}

× : "H" or "L"

DC Recommended Operating Conditions (Ta=0 to +70 °C, GND=0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.2	—	V_{CC}+0.3	V
Input low voltage	V_{IL}	− 0.3 *	—	0.8	V

* V_{IL}= − 3.0V Min. for pulse width less than 50ns.

Electrical Characteristics

• DC characteristics

(Vcc=5V ± 10%, GND=0V, Ta=0 to +70 ℃)

Item	Symbol	Test conditions		− 10L/12L/15L			− 10LL/12LL/15LL			Unit
				Min.	Typ. *	Max.	Min.	Typ. *	Max.	
Input leakage current	I_{LI}	V_{IN}=GND to V_{CC}		− 1	—	1	− 1	—	1	μA
Output leakage current	I_{LO}	$\overline{CE1}$=V_{IH} or CE2=V_{IL} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} $V_{I/O}$=GND to V_{CC}		− 1	—	1	− 1	—	1	μA
Operating power supply current	I_{CC1}	$\overline{CE1}$=V_{IL}, CE2=V_{IH} V_{IN}=V_{IH} or V_{IL} I_{OUT}=0mA		—	7	15	—	7	15	mA
Average operating current	I_{CC2}	Min. cycle Duty=100% I_{OUT}=0mA	Write cycle	—	35	60	—	35	60	mA
			Read cycle	—	25	40	—	25	40	
	I_{CC3}	Cycle time 1 μs Duty=100% I_{OUT}=0mA $\overline{CE1}$ ≦ 0.2V, CE2 ≧ V_{CC} − 0.2V V_{IL} ≦ 0.2V, V_{IH} ≧ V_{CC} − 0.2V	Write cycle	—	10	20	—	10	20	mA
			Read cycle	—	5	10	—	5	10	
Standby current	I_{SB1}	CE2 ≦ 0.2V or $\overline{CE1}$ ≧ V_{CC} − 0.2V CE2 ≧ V_{CC} − 0.2V	0 to 70 ℃	—	—	100	—	—	20	μA
			0 to 40 ℃	—	—	20	—	—	4	
			+25 ℃	—	2	8	—	0.7	2	
	I_{SB2}	$\overline{CE1}$=V_{IH} or CE2=V_{IL}		—	0.6	3	—	0.6	3	mA
Output high voltage	V_{OH}	I_{OH}= − 1.0mA		2.4	—	—	2.4	—	—	V
Output low voltage	V_{OL}	I_{OL}=2.1mA		—	—	0.4	—	—	0.4	V

* Vcc=5V, Ta=25 ℃

I/O capacitance

(Ta=25 ℃, f=1MHz)

Item	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C_{IN}	V_{IN}=0V	—	—	6	pF
I/O capacitance	$C_{I/O}$	$V_{I/O}$=0V	—	—	8	pF

Note) This parameter is sampled and is not 100% tested.

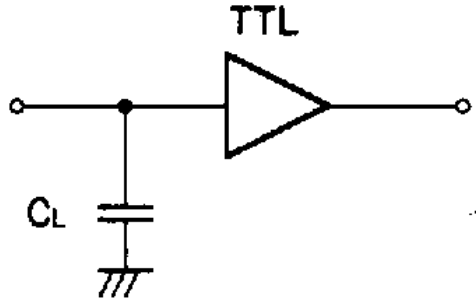
AC characteristics

• AC test conditions

(Vcc=5V ± 10%, Ta=0 to +70°C)

Item	Conditions
Input pulse high level	V_{IH}=2.2V
Input pulse low level	V_{IL}=0.8V
Input rise time	tr=5ns
Input fall time	tf=5ns
Input and output reference level	1.5V
Output load conditions	C_L * =100pF, 1TTL

• Test circuit



* C_L includes scope and jig capacitances.

• **Read cycle** ($\overline{WE}$="H")

Item	Symbol	− 10L/10LL		− 12L/12LL		− 15L/15LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	100	—	120	—	150	—	ns
Address access time	t_{AA}	—	100	—	120	—	150	ns
Chip enable access time ($\overline{CE1}$)	t_{CO1}	—	100	—	120	—	150	ns
Chip enable access time (CE2)	t_{CO2}	—	100	—	120	—	150	ns
Output enable to output valid	t_{OE}	—	50	—	60	—	70	ns
Output hold from address change	t_{OH}	15	—	15	—	15	—	ns
Chip enable to output in low Z ($\overline{CE1}$, CE2)	t_{LZ1}, t_{LZ2}	10	—	10	—	10	—	ns
Output enable to output in low Z ($\overline{OE}$)	t_{OLZ}	5	—	5	—	5	—	ns
Chip disable to output in high Z ($\overline{CE1}$, CE2)	t_{HZ1} *, t_{HZ2}*	—	35	—	40	—	50	ns
Output disable to output in high Z ($\overline{OE}$)	t_{OHZ} *	—	35	—	40	—	50	ns

* t_{HZ1}, t_{HZ2} and t_{OHZ} are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

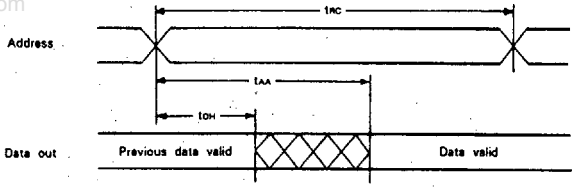
• **Write cycle**

Item	Symbol	− 10L/10LL		− 12L/12LL		− 15L/15LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	100	—	120	—	150	—	ns
Address valid to end of write	t_{AW}	70	—	85	—	100	—	ns
Chip enable to end of write	t_{CW}	70	—	85	—	100	—	ns
Data to write time overlap	t_{DW}	40	—	50	—	60	—	ns
Data hold from write time	t_{DH}	0	—	0	—	0	—	ns
Write pulse width	t_{WP}	70	—	80	—	90	—	ns
Address setup time	t_{AS}	0	—	0	—	0	—	ns
Write recovery time ($\overline{WE}$)	t_{WR}	0	—	0	—	0	—	ns
Write recovery time ($\overline{CE1}$, CE2)	t_{WR1}	0	—	0	—	0	—	ns
Output active from end of write	t_{OW}	10	—	10	—	10	—	ns
Write to output in high Z	t_{WHZ} *	—	30	—	30	—	30	ns

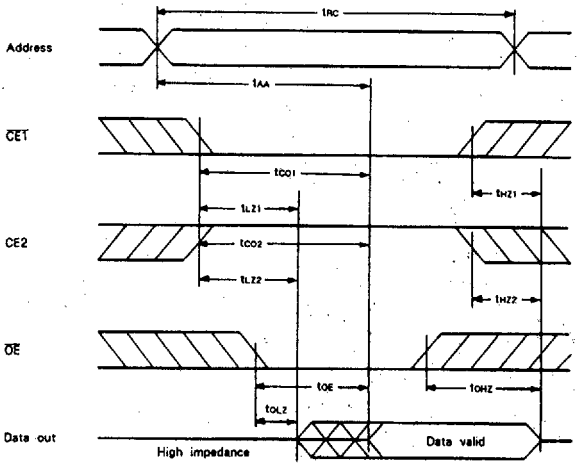
* t_{WHZ} is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage level.

Timing Waveform

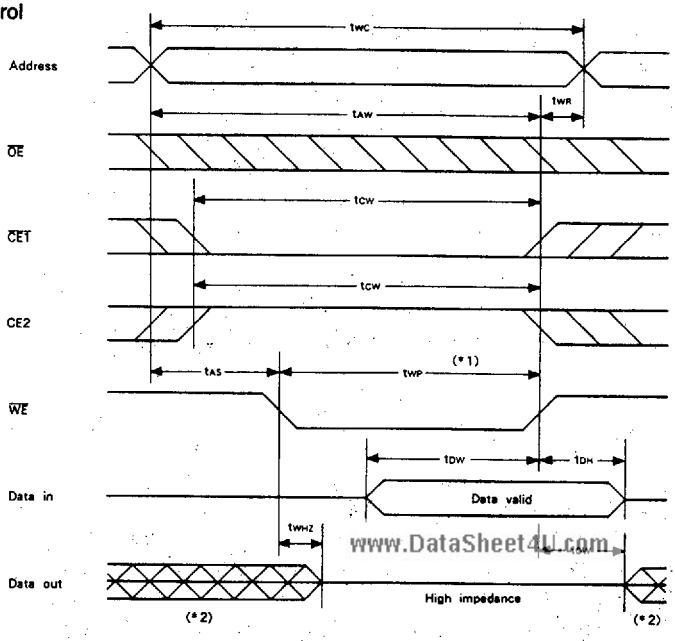
- Read cycle (1) : $\overline{CE1}$=$\overline{OE}$=V_{IL}, CE2=V_{IH}, $\overline{WE}$=V_{IH}



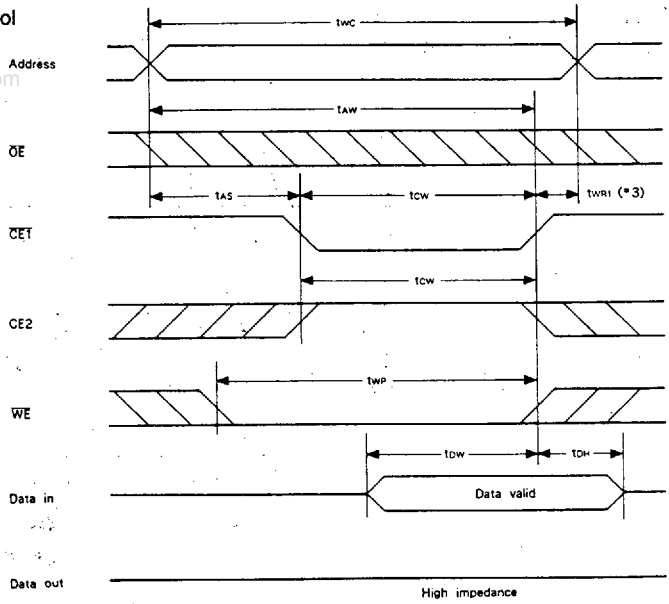
- Read cycle (2) : $\overline{WE}$=V_{IH}



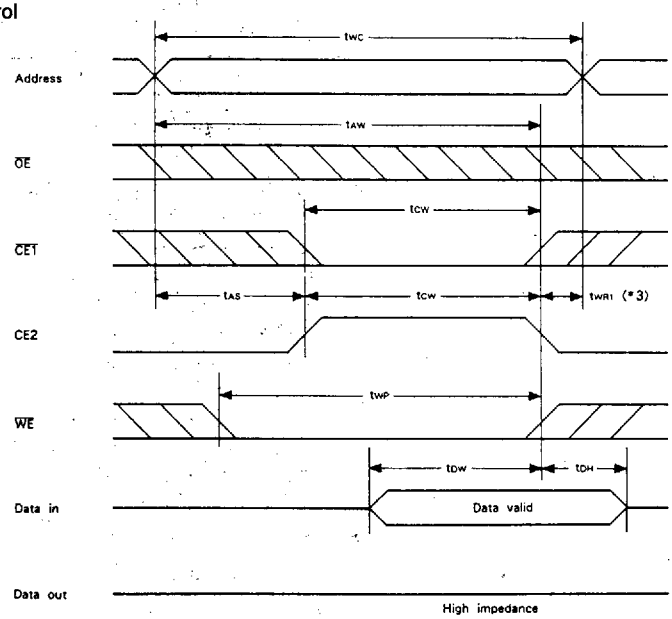
- Write cycle (1) : $\overline{WE}$ control



● Write cycle (2) : $\overline{CE1}$ control



● Write cycle (3) : CE2 control



Note)

*1. Write is executed when both $\overline{CE1}$ and $\overline{WE}$ are at low and CE2 is at high simultaneously.

*2. Do not apply the data input valtage of the opposite phase to the output while output is the output condition.

*3. t_{WR1} is tested from either the rising edge of $\overline{CE1}$ or the falling edge of CE2, whichever comes earlier, until the end of the write cycle.

Data Retention Characteristics

(Ta=0 to 70 ℃)

Item	Symbol	Test conditions		− 10L/12L/15L			− 10LL/12LL/15LL			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
Data retention voltage	V_{DR}	*1		2.0	—	5.5	2.0	—	5.5	V
Data retention current	I_{CCDR1}	V_{CC}=3.0V *1	0 to 70 ℃	—	—	50	—	—	12	μA
			0 to 40 ℃	—	—	10	—	—	2.4	
			+25 ℃	—	1	4	—	0.4	1.2	
	I_{CCDR2}	V_{CC}=2.0 to 5.5V *1		—	2	100	—	0.7	20	mA
Data retention setup time	t_{CDRS}	Chip disable to data retention mode		0	—	—	0	—	—	ns
Recovery time	t_R			t_{RC} *2	—	—	t_{RC} *2	—	—	ns

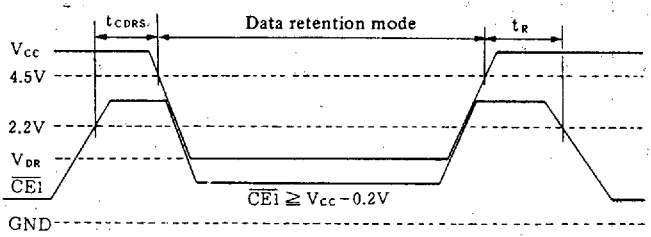
Note)

*1. $\overline{CE1} \geqq V_{CC} - 0.2V$, $CE2 \geqq V_{CC} - 0.2V$ (CE1 control) or $CE2 \leqq 0.2V$ (CE2 control)

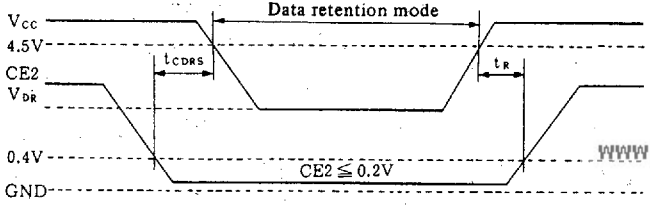
*2. t_{RC} : Read cycle time

Data retention waveform

- Low supply voltage data retention waveform (1) ($\overline{CE1}$ control)

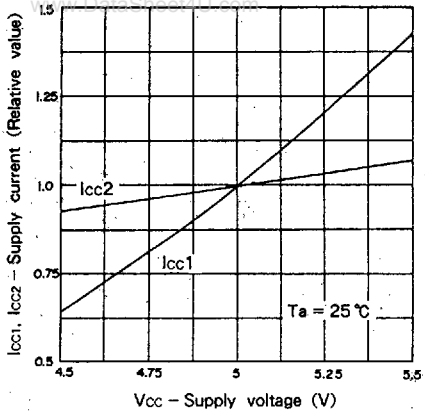


- Low supply voltage data retention waveform (2) (CE2 control)

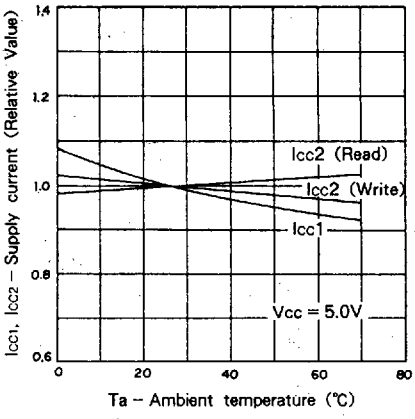


Example of Represeutative Characteristics

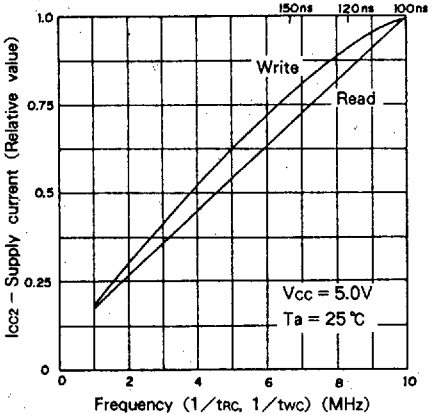
Supply current vs. Supply voltage



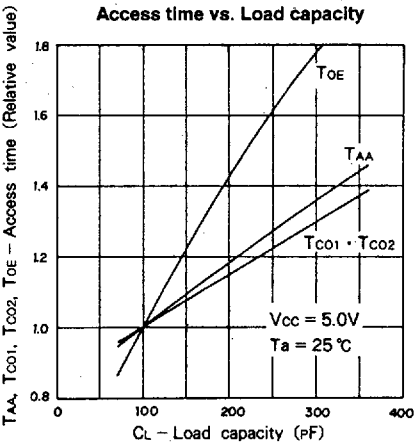
Supply current vs. Ambient temperature



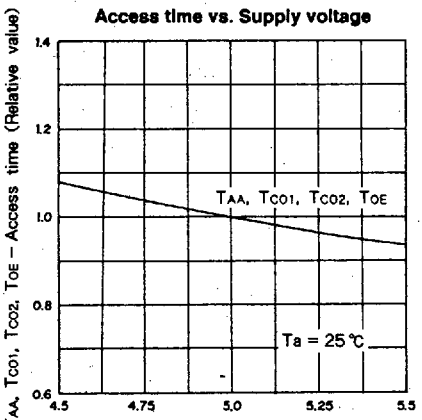
Supply current vs. Frequency



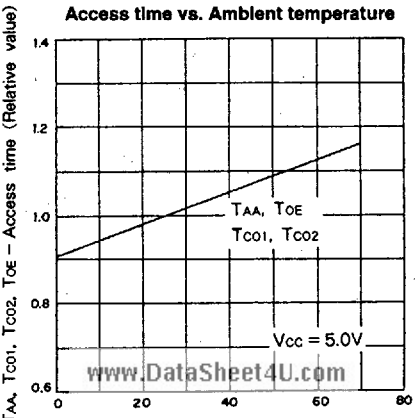
Access time vs. Load capacity



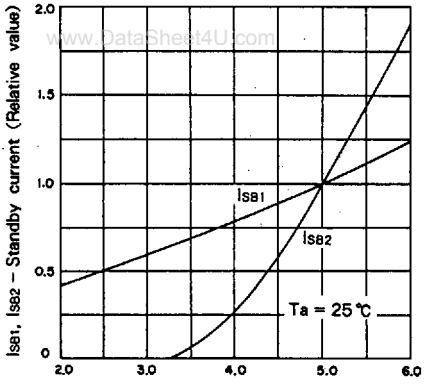
Access time vs. Supply voltage



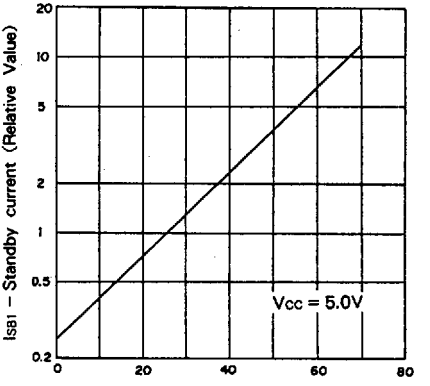
Access time vs. Ambient temperature



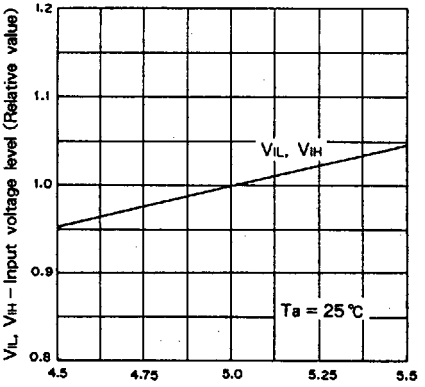
Standby current vs. Supply voltage



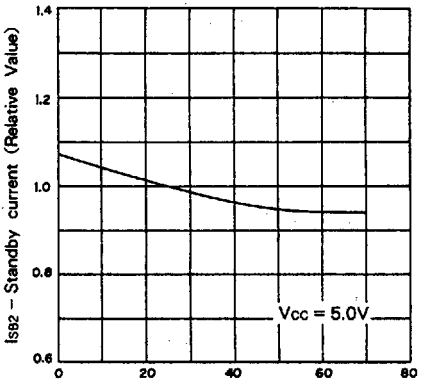
Standby current vs. Ambient temperature



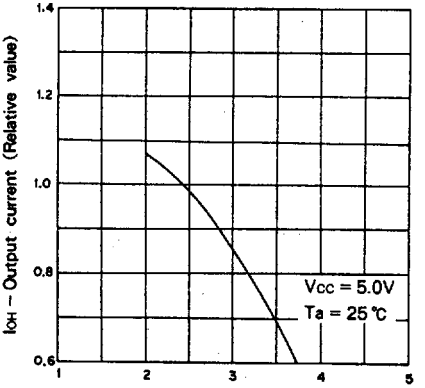
Input voltage level vs. Supply voltage



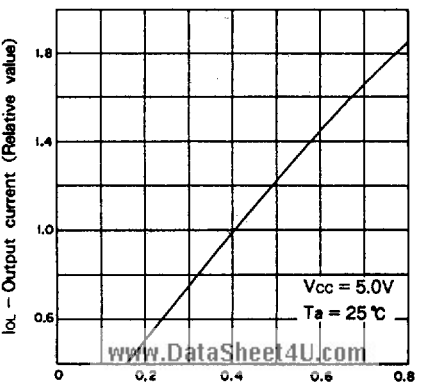
Standby current vs. Ambient temperature



Output current vs. Output voltage

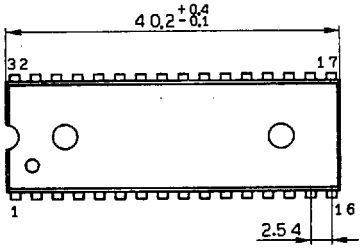


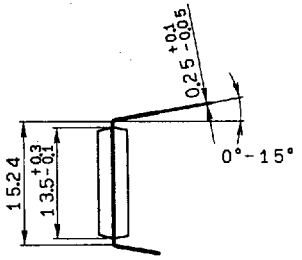
Output current vs. Output voltage

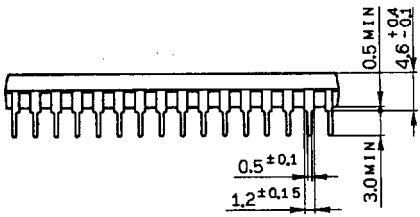


Package Outline Unit : mm

CXK581000P 32Pin DIP (Plastic) 600mil 4.5g

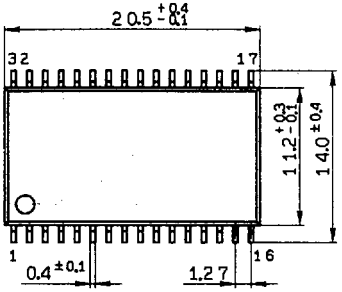


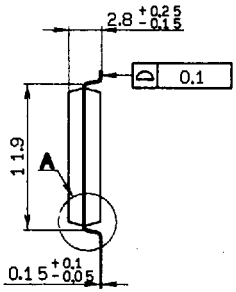


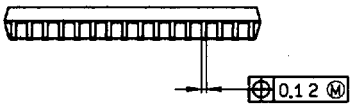


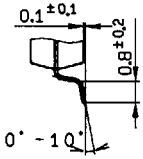
SONY NAME	DIP-32P-01
EIAJ NAME	*DIP032-P-0600-A
JEDEC CODE	———

CXK581000M 32Pin SOP (Plastic) 525mil 1.2g









Detailed diagram of A

SONY NAME	SOP032-P-0525
EIAJ NAME	*SOP032-P-0525-A
JEDEC CODE	———