

CMOS-CCD 1/2H Delay Line for NTSC

Description

The CXL5002M/P are general-purpose CMOS-CCD delay line ICs that provide 1/2H delay time for NTSC.

Features

- Low power consumption 70mW (Typ.)
- Small size package (8-pin SOP, DIP)
- Low differential gain DG = 3% (Typ.)
- Input signal amplitude 180 IRE (= 1.28Vp-p, Max.)
- Low input clock amplitude operation 150mVp-p (Min.)
- Built-in peripheral circuits (clock driver, timing generator, autobias, and output circuits)

Functions

- 340-bit CCD register
- Clock drivers
- Autobias circuit
- Sync tip clamp circuit
- Sample and hold circuit

Structure

CMOS-CCD

Absolute Maximum Ratings (Ta = 25°C)

- Supply voltage V_{DD} 11 V
- Supply voltage V_{CL} 6 V
- Operating temperature T_{opr} -10 to +60 °C
- Storage temperature T_{stg} -55 to +150 °C
- Allowable power dissipation P_D

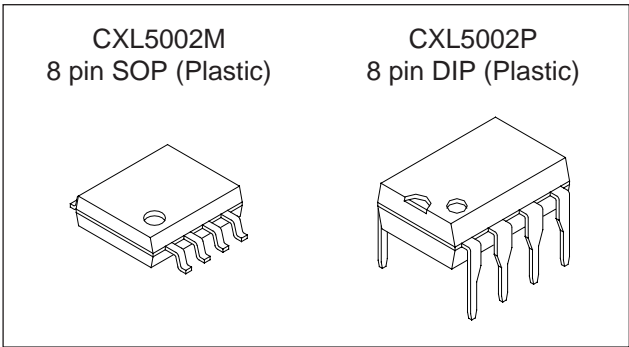
| | |
|----------|--------|
| CXL5002M | 350 mW |
| CXL5002P | 480 mW |

Recommended Operating Conditions

- Supply voltage V_{DD} 9 ± 5% V
- V_{CL} 5 ± 5% V

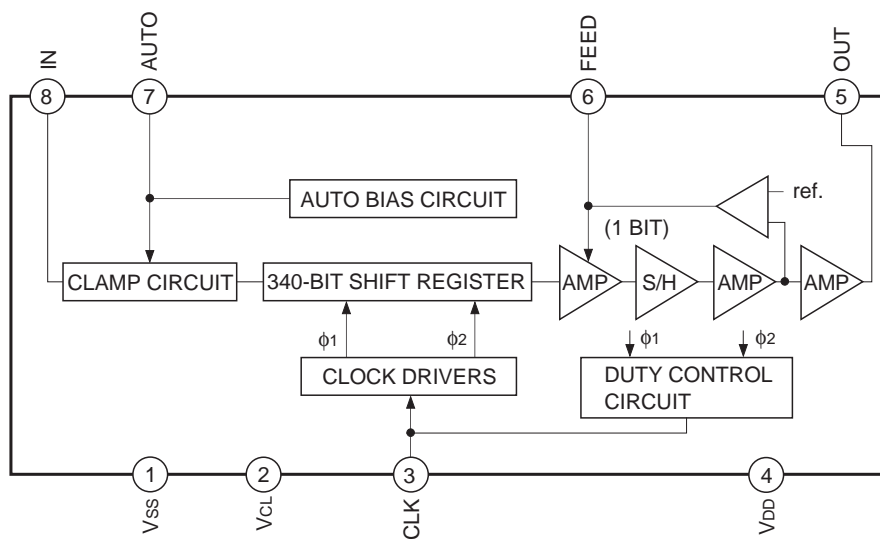
Recommended Clock Conditions

- Input clock amplitude V_{CK} 150mVp-p to 1.0Vp-p
(250mVp-p typ.)
- Clock frequency f_{CK} 10.7MHz



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Block Diagram



Pin Description

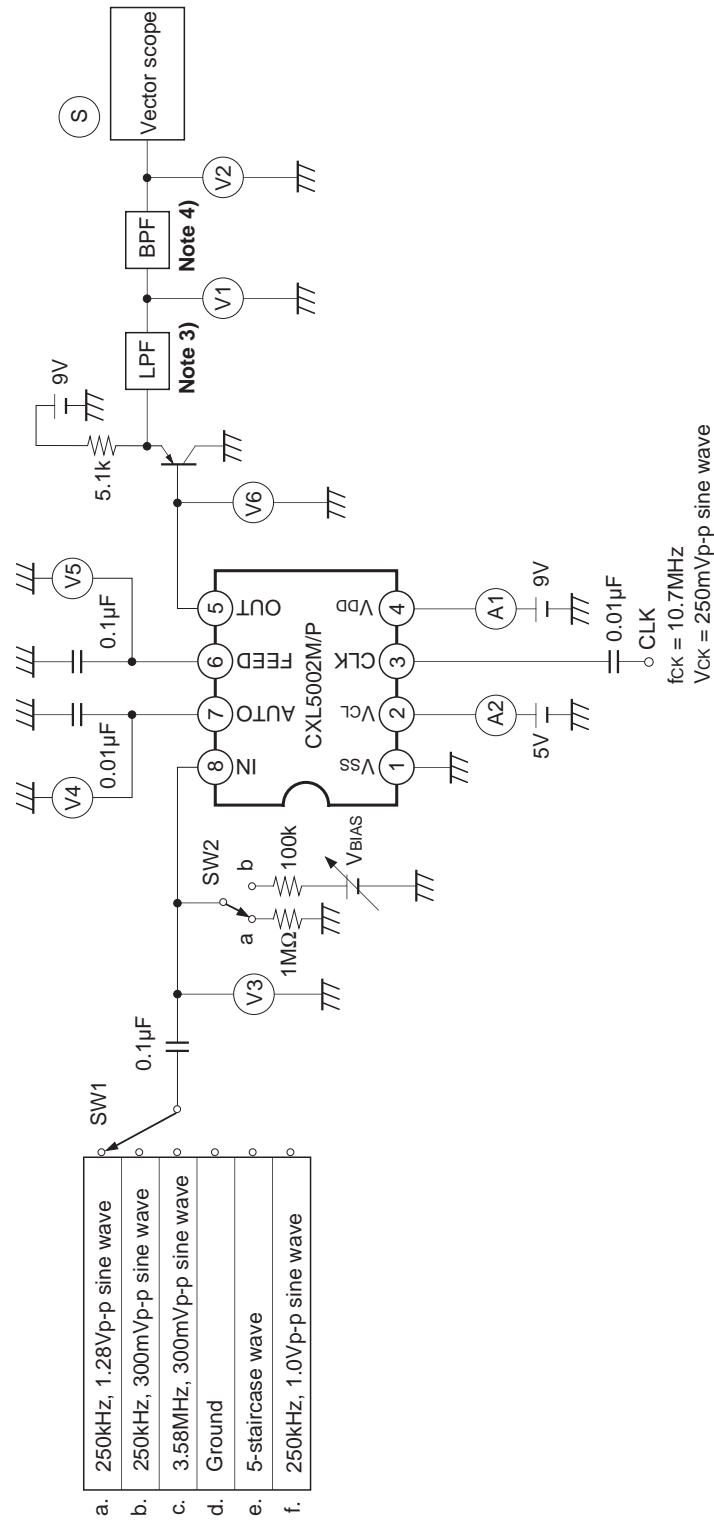
| Pin No. | Symbol | Description | Impedance [Ω] | Pin No. | Symbol | Description | Impedance [Ω] |
|---------|-----------------|-----------------|------------------------|---------|--------|--------------------|------------------------|
| 1 | V _{SS} | GND | | 5 | OUT | Signal output | 600 to 1k |
| 2 | V _{CL} | 5V power supply | | 6 | FEED | Feedback DC output | > 100k |
| 3 | CLK | Clock input | > 100k | 7 | AUTO | Autobias DC output | 10k |
| 4 | V _{DD} | 9V power supply | | 8 | IN | Signal input | > 100k |

Electrical Characteristics

($T_a = 25^\circ\text{C}$, $V_{DD} = 9.0\text{V}$, $V_{CL} = 5.0\text{V}$, $f_{CK} = 10.7\text{MHz}$, $V_{CK} = 250\text{mVp-p}$ sine wave,
See "Electrical characteristics test circuit")

| Item | Symbol | Measuring condition | SW conditions | | Measuring point | Min. | Typ. | Max. | Unit |
|------------------------------|----------------------|---|---------------|---|-----------------|------|------|------|------|
| | | | 1 | 2 | | | | | |
| Supply current | I _{DD} | 250kHz, 1.28Vp-p, sine wave input | a | a | A1 | — | 4 | 5 | mA |
| | I _{CL} | | | | A2 | — | 7 | 9 | mA |
| Insertion gain | IG | 250kHz, 1.28Vp-p, sine wave input IG = 20 log (Output voltage [Vp-p] / 1.28 [Vp-p]) | a | a | V1 | -3 | 0 | 3 | dB |
| Frequency response | fG | Dissipation at 3.5MHz in relation to 250kHz fG = 20 log (V _{3.5MHz} / V _{250kHz}) (Note 1) | b, c | b | V1 | -3.0 | -2.1 | — | dB |
| Differential gain | DG | 5-staircase wave input Y = 140 IRE (= 1.0Vp-p) Measure S point with vector scope (Note 2) | e | a | S | — | 3 | 5 | % |
| Differential phase | DP | | | | | — | 3 | 5 | deg |
| Allowable input amplitude | V _{IN-AC} | | — | — | — | — | — | 1.28 | Vp-p |
| Noise | S/N | S: Input = 250kHz, 1.0Vp-p output (Vp-p) | f | a | V2 | 55 | 60 | — | dB |
| | | N: Input = DC ground output (mVrms) | d | a | V2 | | | | |
| Output DC voltage | V _{IN-AC} | | d | a | V3 | 3.5 | 5.0 | 6.5 | V |
| | V _{AUTO-DC} | | | | V4 | 3.5 | 5.0 | 6.5 | V |
| | V _{FEED-DC} | 250kHz, 1.28Vp-p, sine wave input | a | a | V5 | 1.3 | 2.3 | 3.3 | V |
| | V _{OUT-DC} | | | | V6 | 1.7 | 2.7 | 3.7 | V |

Electrical Characteristics Test Circuit

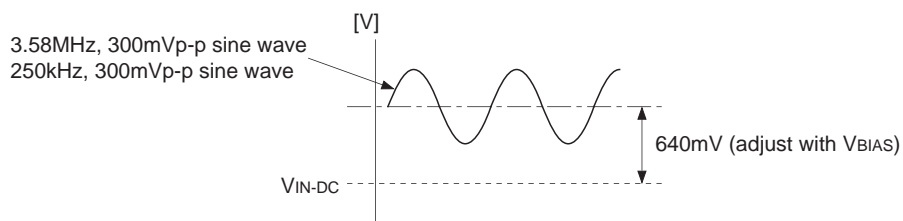


Note 1) Frequency response measuring condition

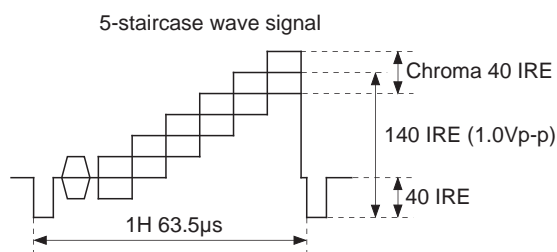
$V_{3.58\text{MHz}}$ (Output signal voltage [Vp-p] at 3.58MHz input)

$V_{250\text{kHz}}$ (Output signal voltage [Vp-p] at 250kHz input)

Set Pin 8 (IN) voltage [V] = $V_{\text{IN-DC}} + 640\text{mV}$.

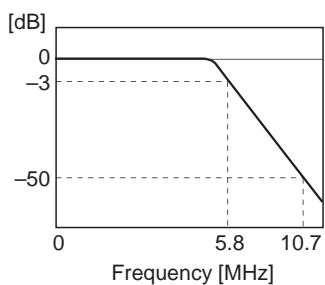


Note 2) Differential gain and differential phase measuring condition

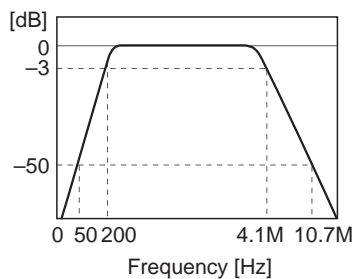


DG and DP are measured at output S point by vector scope.

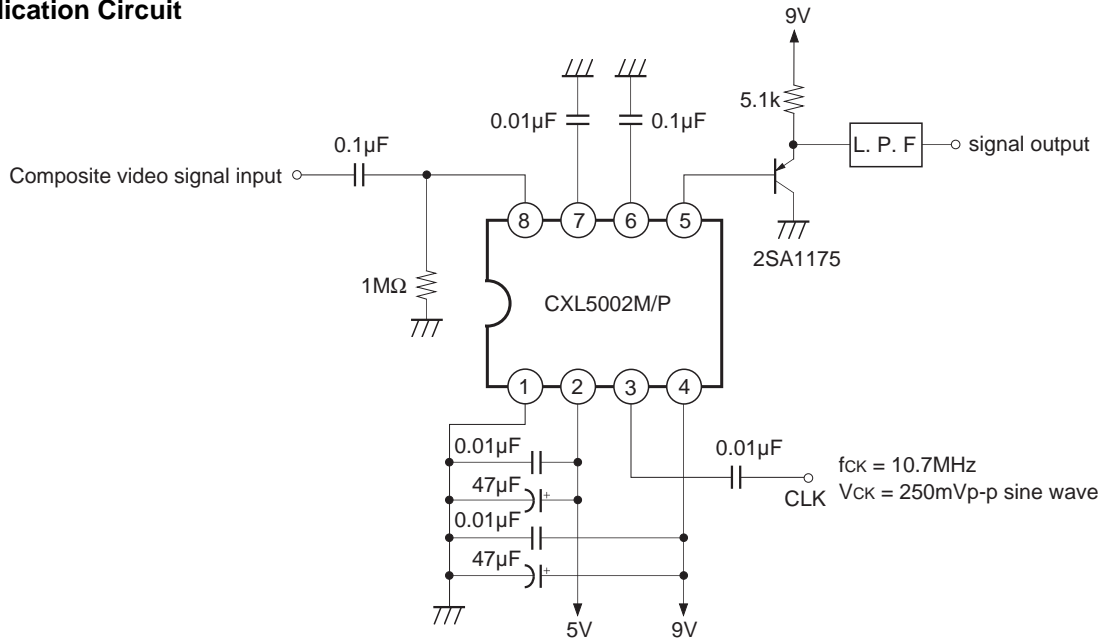
Note 3) LPF frequency response



Note 4) BPF frequency response



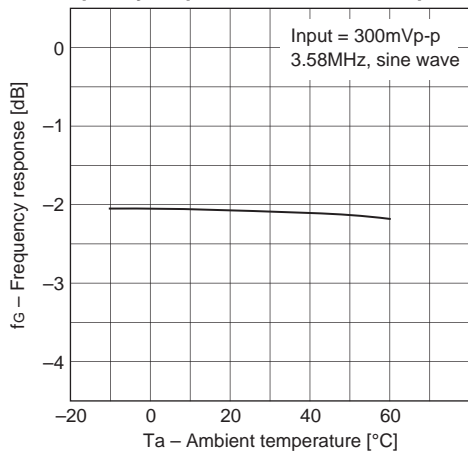
Application Circuit



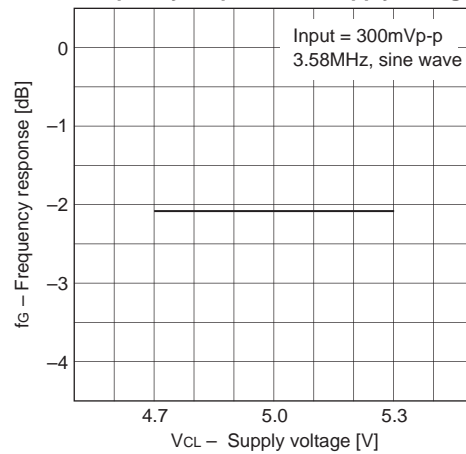
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Example of Representative Characteristics

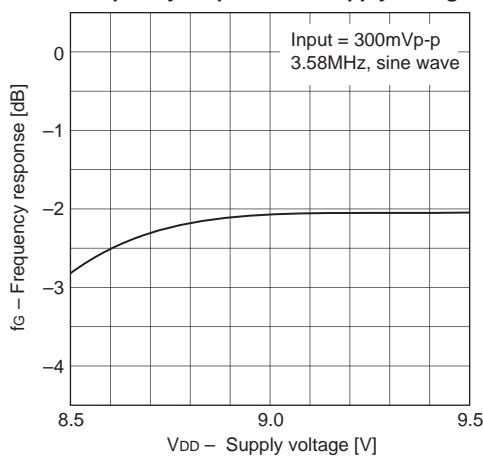
Frequency response vs. Ambient temperature



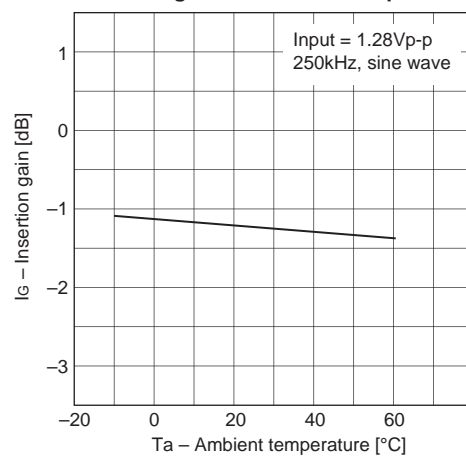
Frequency response vs. Supply voltage

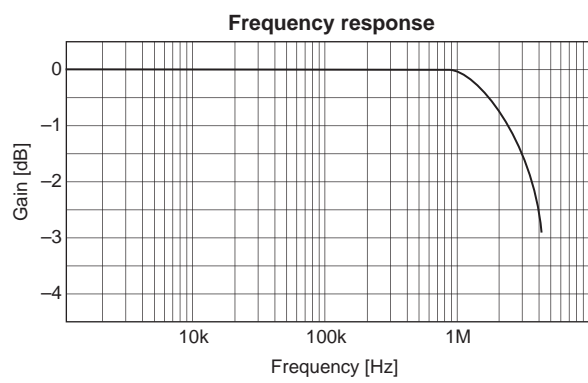
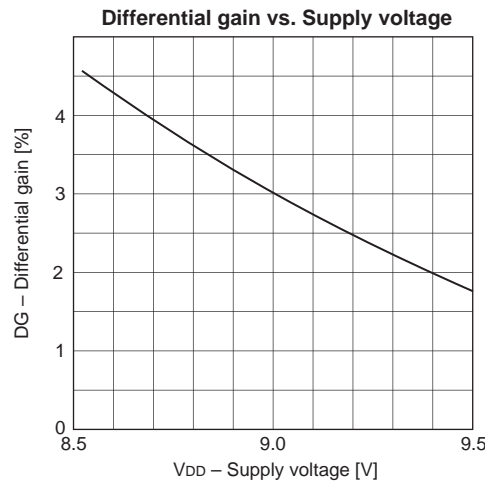
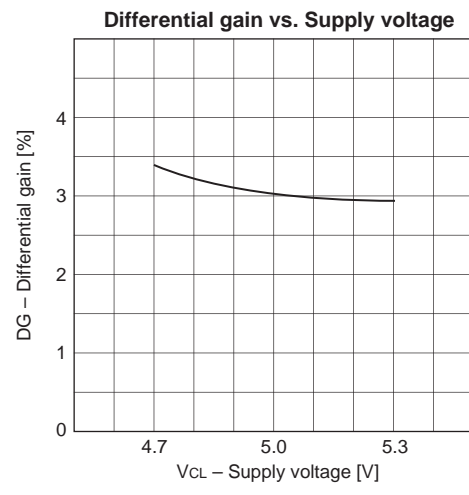
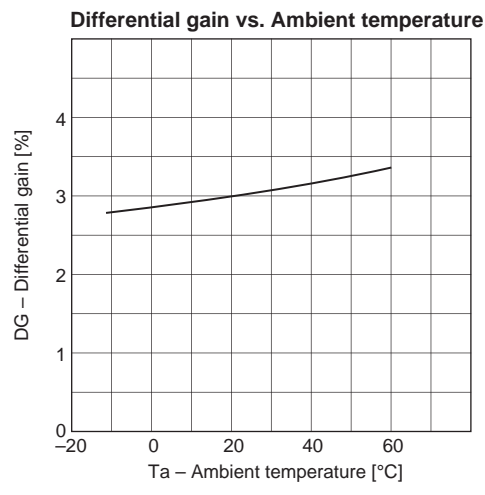
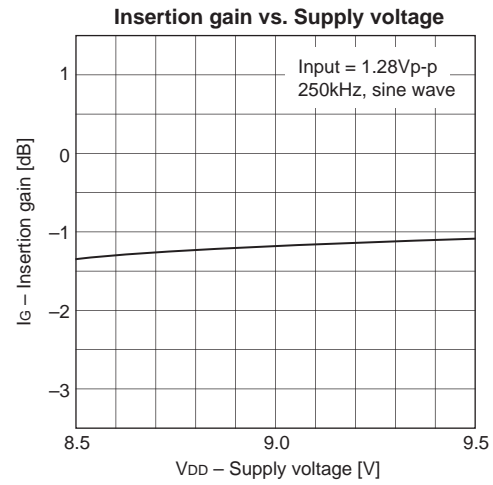
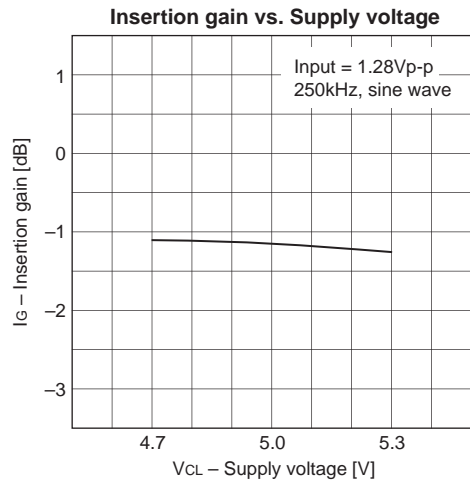


Frequency response vs. Supply voltage



Insertion gain vs. Ambient temperature



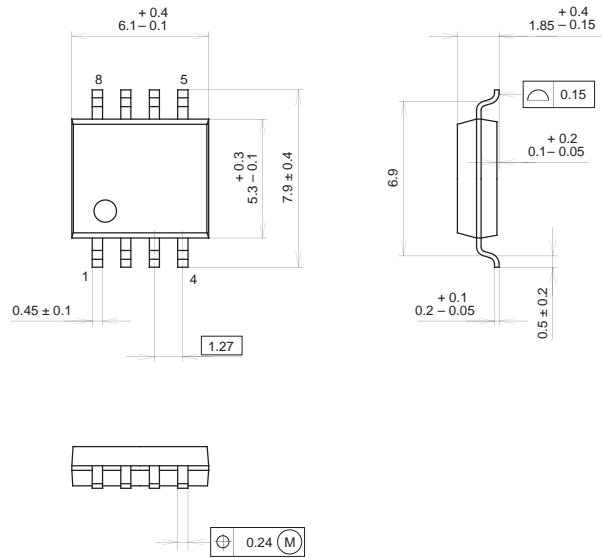


Package Outline

Unit: mm

CXL5002M

8PIN SOP (PLASTIC)



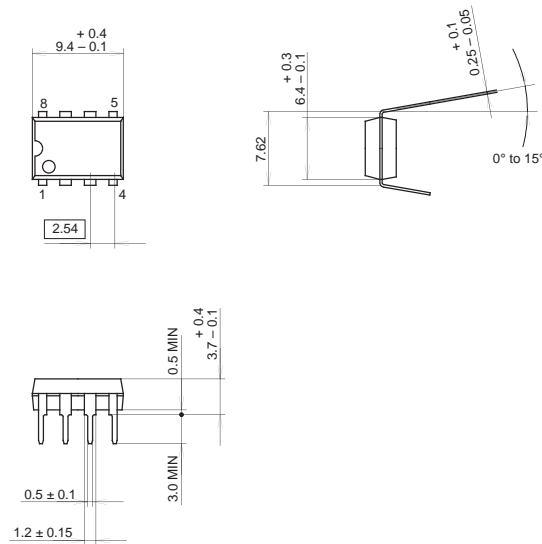
PACKAGE STRUCTURE

| | |
|------------|---------------|
| SONY CODE | SOP-8P-L01 |
| EIAJ CODE | SOP008-P-0300 |
| JEDEC CODE | — |

| | |
|------------------|-----------------|
| PACKAGE MATERIAL | EPOXY RESIN |
| LEAD TREATMENT | SOLDER PLATING |
| LEAD MATERIAL | 42/COPPER ALLOY |
| PACKAGE MASS | 0.1g |

CXL5002P

8PIN DIP (PLASTIC)



PACKAGE STRUCTURE

| | |
|------------|---------------|
| SONY CODE | DIP-8P-01 |
| EIAJ CODE | DIP008-P-0300 |
| JEDEC CODE | — |

| | |
|------------------|----------------|
| PACKAGE MATERIAL | EPOXY RESIN |
| LEAD TREATMENT | SOLDER PLATING |
| LEAD MATERIAL | COPPER ALLOY |
| PACKAGE MASS | 0.5g |