SONY

SP7T Antenna Switch Module for GSM and UMTS or CDMA Dual Mode Handset

CXM3517BER

Description

This switch is one of a range of low insertion loss, good linearity and high power MMIC antenna switch modules for GSM/UMTS or CDMA dual-mode handsets.
The Sony A.S.M. contains SP7T switch, a 1.8V CMOS decoder and a dual-LPF on GSM transmit paths.
The Sony GaAs junction gate pHEMT (JPHEMT) process is used for very low insertion loss and high linearity.
The excellent insertion loss contributes to good sensitivity and longer talk time.
* A.S.M. = Antenna Switch Module
(Applications: Quad Band GSM and Single Band UMTS or CDMA Dual-Mode Handset)

Features

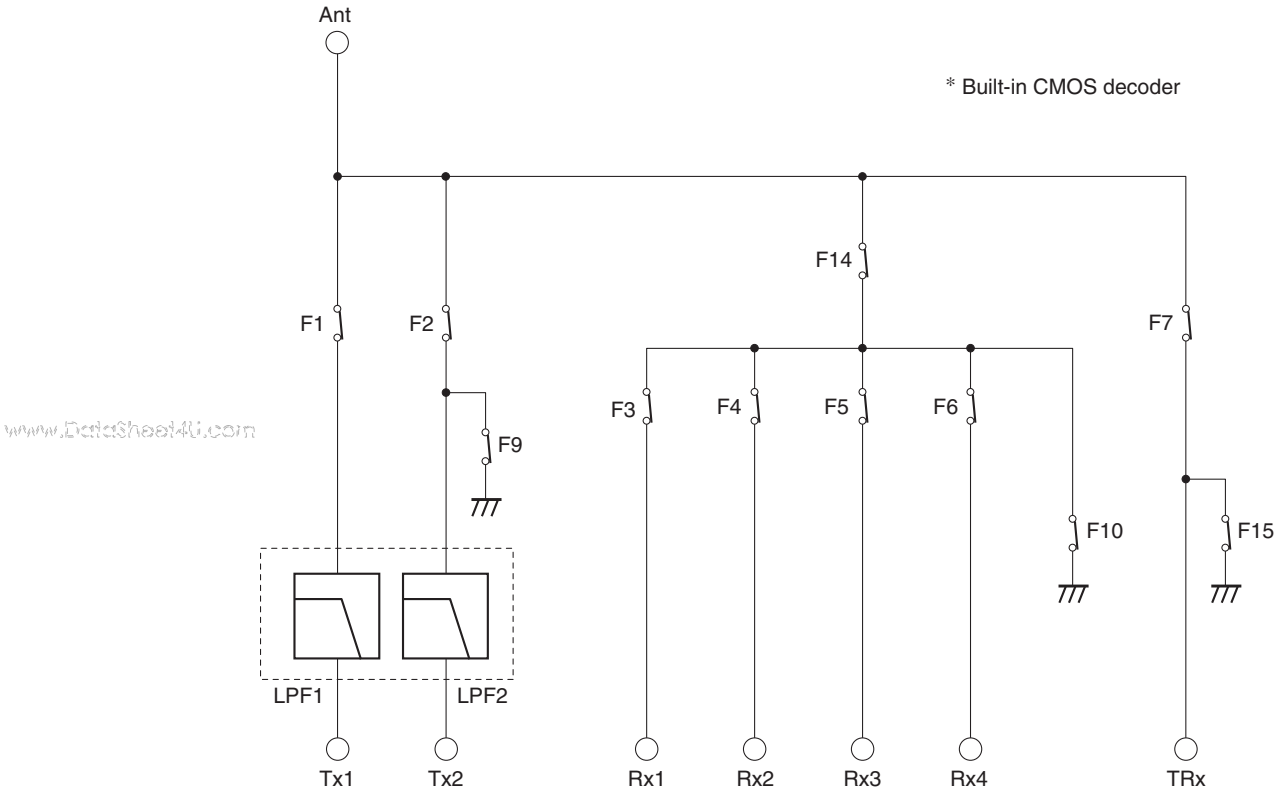
- ◆ Low insertion loss: 0.80dB (Typ.) on Tx1 (GSM Low Band Tx)
  0.80dB (Typ.) on Tx2 (GSM High Band Tx)
  0.33dB (Typ.) on TRx (UMTS Band I)
- ◆ High attenuation: 30dB (Typ.) Tx1 @ 2nd Harmonic freq.
  30dB (Typ.) Tx2 @ 2nd Harmonic freq.
- ◆ No DC blocking capacitors (Small device footprint)
  Small package: VQFN-22P (2.6mm × 3.4mm × 0.8mm Typ.)
- ◆ Low voltage operation: V_{DD} = +2.65V
- ◆ CMOS control line (CTLA/CTLB/CTLC)
- ◆ RX paths are changeable for band assignment
- ◆ Lead-free and RoHS compliant

Structure

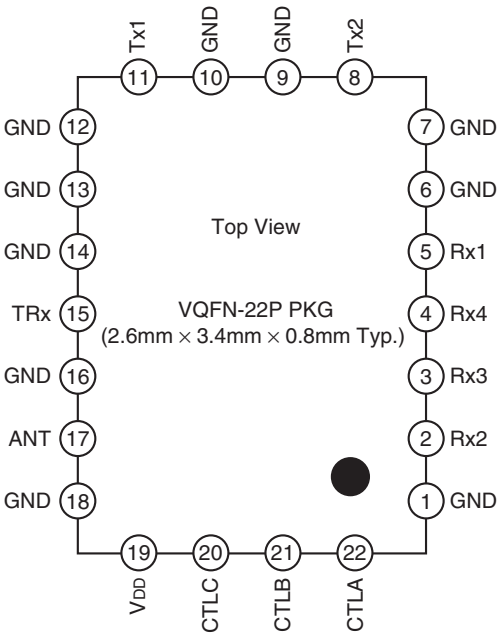
GaAs Junction Gate pHEMT (JPHEMT) Switch, CMOS Decoder and Dual-LPF

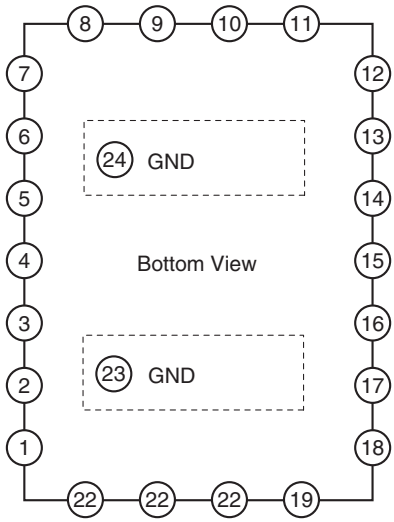
Note on Handling
- GaAs MMIC's are ESD sensitive devices. Special handling precautions are required.

Block Diagram



Pin Configuration





Pin Description

Pin No.	Symbol	Pin No.	Symbol
1	GND	13	GND
2	Rx2	14	GND
3	Rx3	15	TRx
4	Rx4	16	GND
5	Rx1	17	ANT
6	GND	18	GND
7	GND	19	V_{DD}
8	Tx2 (GSM1800/1900)	20	CTLC
9	GND	21	CTLB
10	GND	22	CTLA
11	Tx1 (GSM850/900)	23	GND (Bottom)
12	GND	24	GND (Bottom)

Truth Table

State	Active path	Vctl state			Switch state*2										
		A	B	C	F1	F2	F3	F4	F5	F6	F7	F9	F10	F14	F15
1	Tx1	H	H	L	H	L	L	L	L	L	L	H	H	L	H
2	Tx2	H	L	L	L	H	L	L	L	L	L	L	H	L	H
3	Rx1 *1	L	L	L	L	L	H	L	L	L	L	H	L	H	H
4	Rx2 *1	L	L	H	L	L	L	H	L	L	L	H	L	H	H
5	Rx3 *1	L	H	H	L	L	L	L	H	L	L	H	L	H	H
6	Rx4 *1	L	H	L	L	L	L	L	L	H	L	H	L	H	H
7	TRx	H	L	H	L	L	L	L	L	L	H	H	H	L	L

*1 Each RX path can be used from 869MHz to 1990MHz frequency, user can select these RX paths changeably.

*2 State “L” means a switch “OFF”, state “H” means a switch “ON”.

Electrical Characteristics

Supply Voltage Value

(Ta = +25°C)

Item	Min.	Typ.	Max.	Unit
Bias voltage (V_{DD})	+2.5	+2.65	+3.3	V

Logic Value

(Ta = +25°C)

Item	State	Min.	Typ.	Max.	Unit
Control voltage (CTL-A/B/C)	High	+1.5	+1.8	+3.3	V
	Low	0	—	+0.3	

Absolute Maximum Ratings

Item	Ratings
Bias voltage (V_{DD})	4.3V (Ta: +25°C)
Control voltage (CTL-A/B/C)	4.3V (Ta: +25°C)
Input power max. [Tx1] *1	+36.5dBm (Duty cycle: 25%) (Ta: +25°C)
Input power max. [Tx2] *1	+34.5dBm (Duty cycle: 25%) (Ta: +25°C)
Input power max. [TRx] *1	+32dBm (Ta: +25°C)
Input power max. [Rx1, Rx2, Rx3, Rx4] *1	+13dBm (Ta: +25°C)
Operating temperature range	–30 to +90°C
Strage temperature range	–65 to +150°C

*1 FR-4 (4 layers), 30mm Sqr., t = 0.8mm

(V_{DD} = 2.65V, Vctl = 0/1.8V, Ta: +25°C)

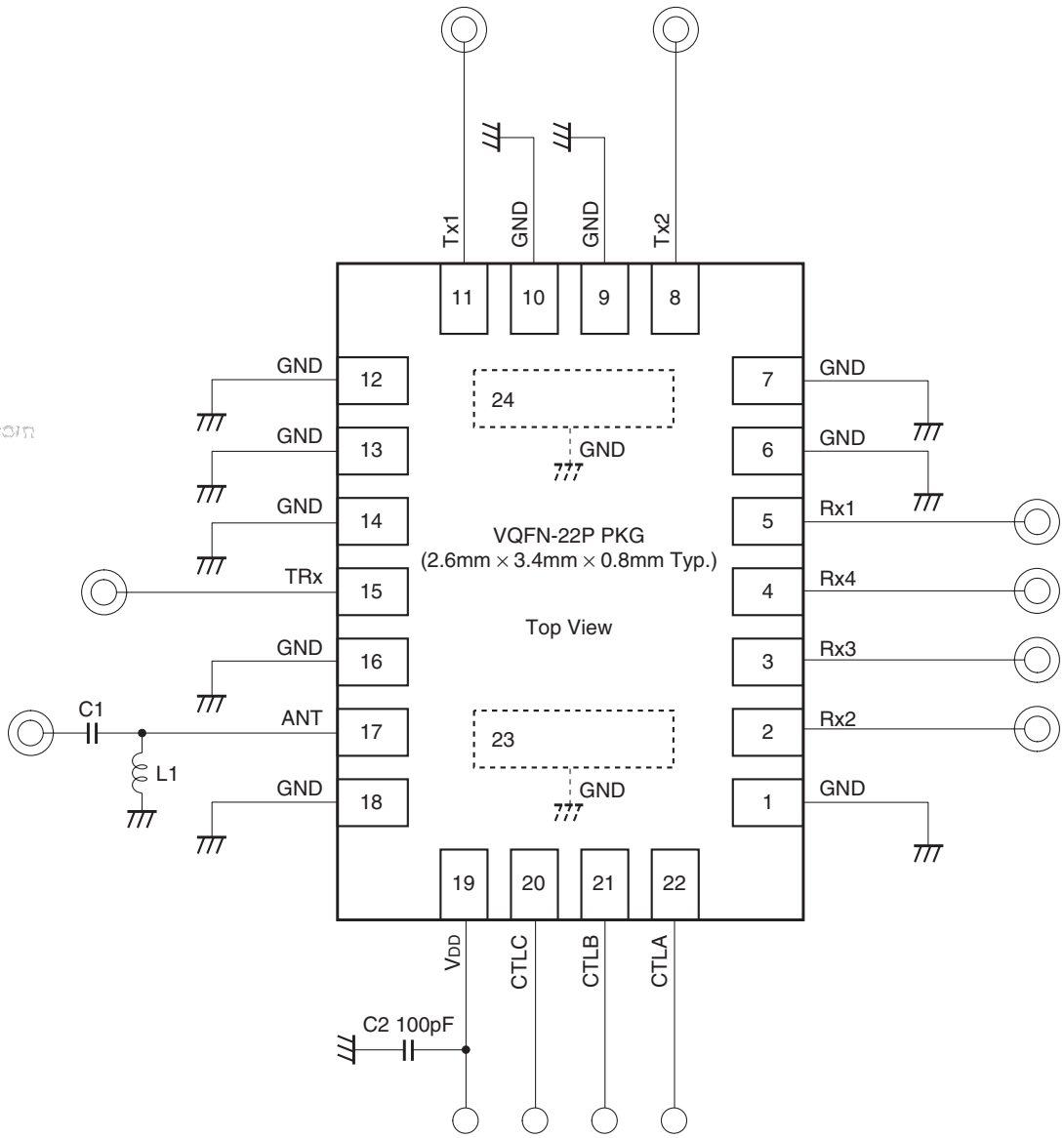
Item	Symbol	Path	Conditions		Min.	Typ.	Max.	Unit
Insertion loss	I.L	Ant - Tx1	*1		—	0.80	1.00	dB
		Ant - Tx2	*2		—	0.80	1.00	
		Ant - Rx1, Rx2, Rx3, Rx4	*3		—	0.65	0.80	
			*4		—	0.85	1.00	
		Ant - TRx	*5		—	0.33	0.50	
			*8		—	0.25	0.40	
Isolation	Iso	Tx1 - Rx1, Rx2, Rx3, Rx4	*1 824 to 915MHz	State 1	45	55	—	dB
		Tx1 - TRx	*1 824 to 915MHz	State 1	30	40	—	
		Tx1 - Tx2	*1 824 to 915MHz	State 1	18	21	—	
		Tx1 - Ant	*1 880 to 915MHz	State 3/4/5/6	22	26	—	
			*10 1710 to 1910MHz	State 3/4/5/6	30	40	—	
		Tx2 - Ant	*1 1760 to 1830MHz	State 1	26	31	—	
			*1 2640 to 2745MHz	State 1	26	31	—	
			*11 824 to 915MHz	State 3/4/5/6	20	28	—	
			*2 1710 to 1910MHz	State 3/4/5/6	19	23	—	
		Tx2 - Rx1, Rx2, Rx3, Rx4	*2 1710 to 1910MHz	State 2	40	50	—	
		Tx2 - TRx	*2 1710 to 1910MHz	State 2	25	30	—	
		Tx2 - Tx1	*2 1710 to 1910MHz	State 2	28	31	—	
		TRx - Rx1, Rx2, Rx3, Rx4	*5 1920 to 2170MHz	State 7	40	50	—	
			*8 824 to 894MHz	State 7	45	55	—	
			*9 1710 to 1990MHz	State 7	45	55	—	
		TRx - Tx1	*5 1920 to 2170MHz	State 7	30	39	—	
			*8 824 to 894MHz	State 7	20	26	—	
			*9 1710 to 1990MHz	State 7	30	39	—	
		TRx - Tx2	*5 1920 to 2170MHz	State 7	20	24	—	
			*8 824 to 894MHz	State 7	30	38	—	
			*9 1710 to 1990MHz	State 7	20	25	—	
V.S.W.R.	VSWR	Ant - Tx1	824 to 915MHz		—	1.30	1.60	—
		Ant - Tx2	1710 to 1910MHz		—	1.45		
		Ant - Rx1, Rx2, Rx3, Rx4, TRx	824 to 2170MHz		—	1.20		
Harmonic level	2fo	Tx1 - Ant	*1		—	–48	–36	dBm
	3fo				—	–48	–36	
	2fo	Tx2 - Ant	*2		—	–52	–36	
	3fo				—	–43	–36	
	2fo	TRx - Ant	*5		—	–54	–36	
	3fo				—	–53	–36	
	2fo	TRx - Ant	*8		—	–60	–36	
	3fo				—	–58	–36	

Item	Symbol	Path	Conditions	Min.	Typ.	Max.	Unit
Inter modulation distortion	IMD2	TRx - Ant	*6, *12	—	–107	–105	dBm
	IMD3	TRx - Ant	*7, *12	—	–106	–102	
Attenuation	ATT	Tx1 - Ant	1648 to 1830MHz	25	30	—	dB
			2472 to 2745MHz	25	41	—	
			3296 to 3660MHz	20	26	—	
		Tx2 - Ant	3420 to 3820MHz	25	30	—	
			5130 to 5730MHz	25	33	—	
Switching time	Ts		90% OFF – 90% ON	—	3	5	μs
Control current	Ictl		V_{DD} = 2.65V, Vctl = 1.8V	—	5	20	μA
Supply current	Idd		Active Mode	—	0.18	0.40	mA

Electrical characteristics are specified on Sony EVB and with all RF ports terminated with 50Ω.

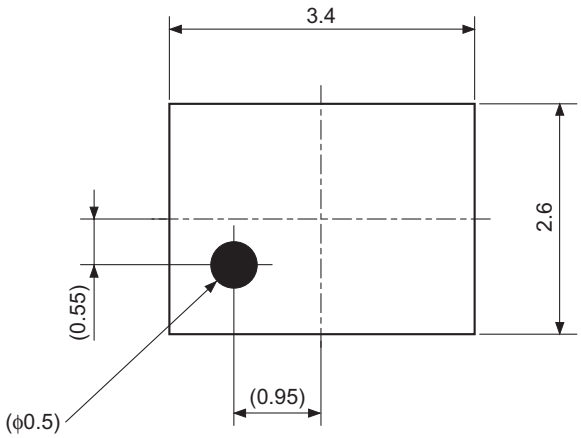
*1 Pin on Tx1: +34dBm, 824 to 915MHz, V_{DD} = 2.65V
*2 Pin on Tx2: +32dBm, 1710 to 1910MHz, V_{DD} = 2.65V
*3 Pin on Ant: +10dBm, 869 to 960MHz, V_{DD} = 2.65V
*4 Pin on Ant: +10dBm, 1805 to 1990MHz, V_{DD} = 2.65V
*5 Pin on TRx: +26dBm, 1920 to 2170MHz, V_{DD} = 2.65V
*6 Pin on TRx: +20dBm, 1950MHz, Pin on Ant: –15dBm, 190MHz, V_{DD} = 2.65V
*7 Pin on TRx: +20dBm, 1950MHz, Pin on Ant: –15dBm, 1760MHz, V_{DD} = 2.65V
*8 Pin on TRx: +26dBm, 824 to 894MHz, V_{DD} = 2.65V
*9 Pin on TRx: +26dBm, 1710 to 1990MHz, V_{DD} = 2.65V
*10 Pin on Tx1: +5dBm, 1710 to 1910MHz, V_{DD} = 2.65V
*11 Pin on Tx2: +5dBm, 824 to 915MHz, V_{DD} = 2.65V
*12 Measured with recommended circuit

Recommended Circuit



Note) 1. No DC blocking capacitors are required on all RF ports.
2. DC levels of all RF ports are GND.
3. L1 (22nH) and C1 (22pF) are recommended on Ant port for ESD protection.

Pin 1 Index

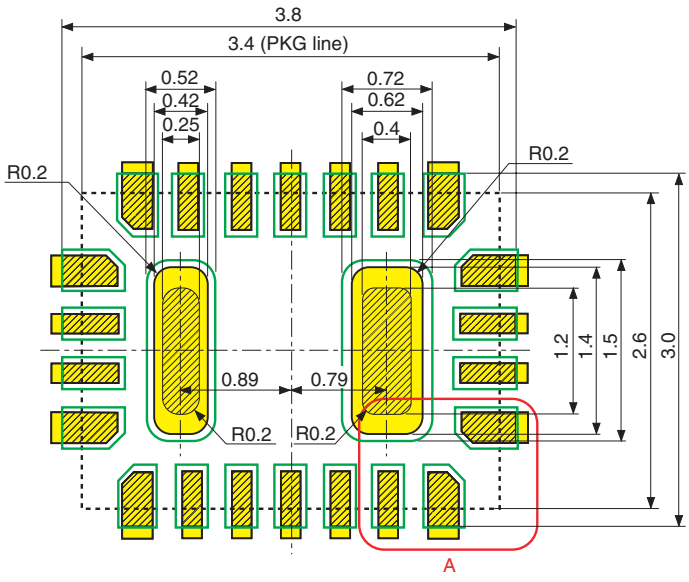


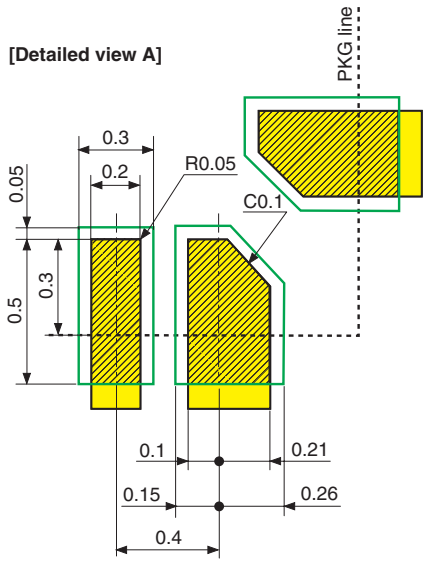
PCB Layout Template

• PKG size: 3.4mm × 2.6mm
• Pin pitch: 0.4mm

: Land
: Mask (Open area)
: Resist (Open area)

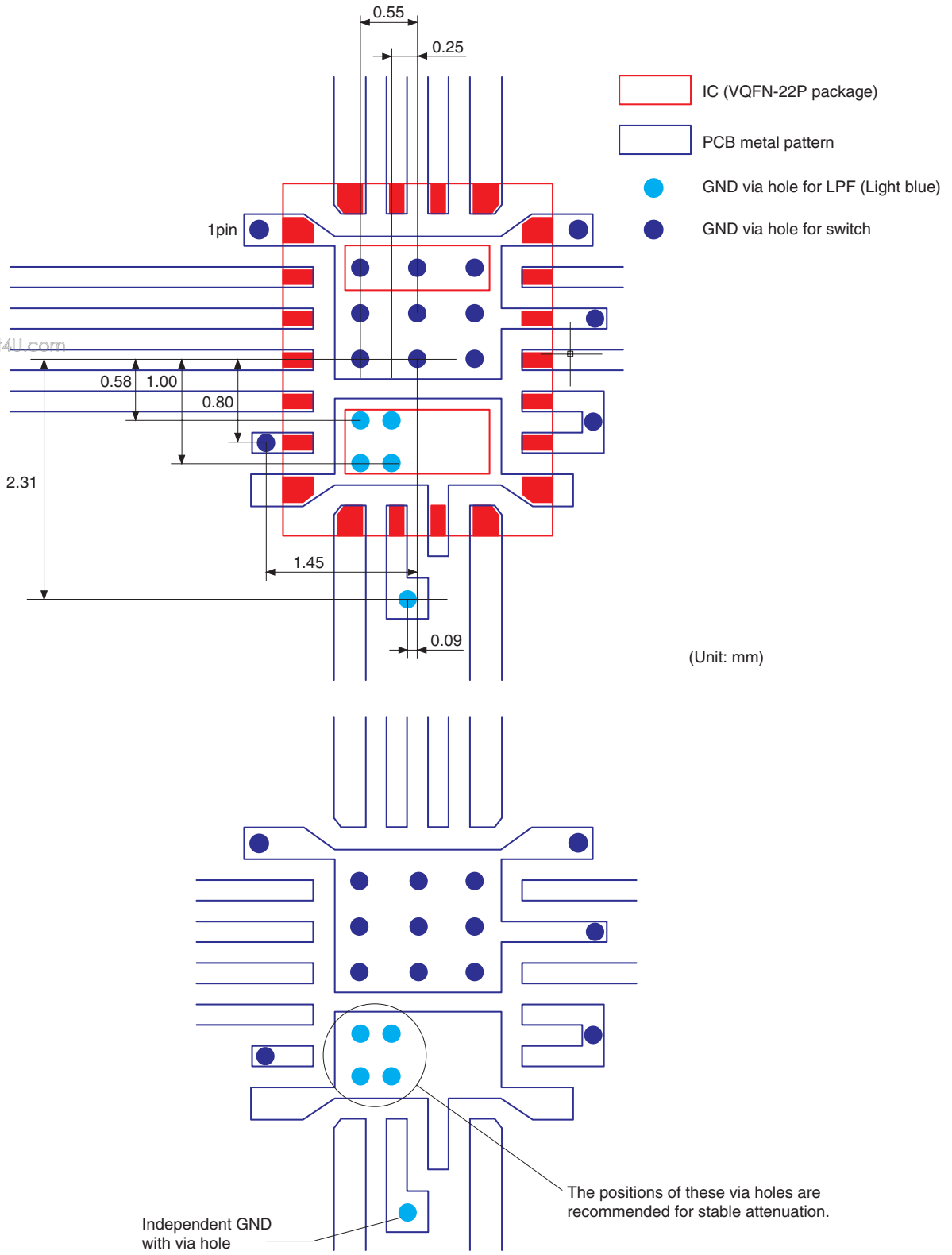
* Metal mask thickness: 110µm





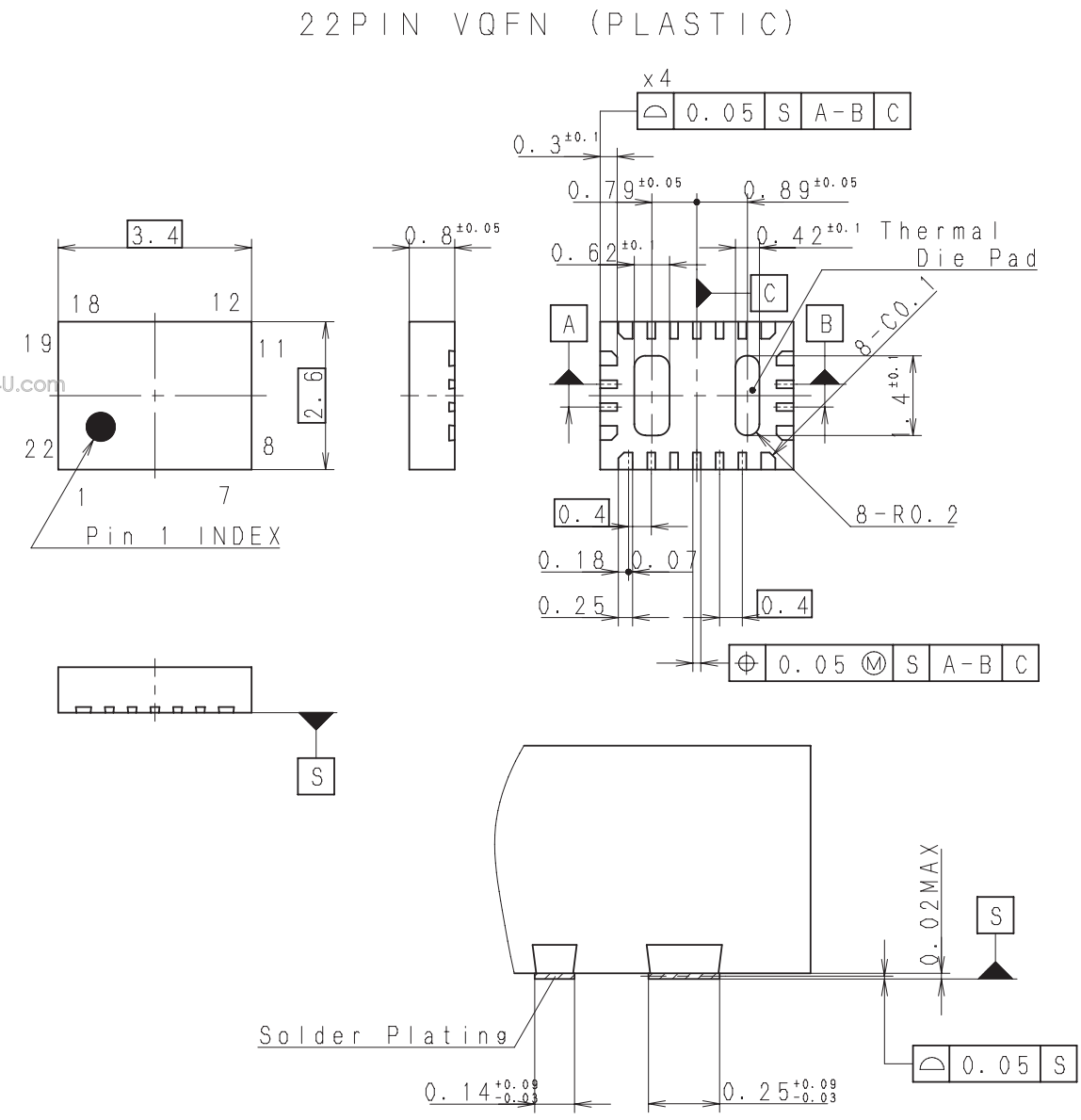
* Mask corner R = 0.05mm

Recommended PCB Design



Package Outline

(Unit: mm)



TERMINAL SECTION

PACKAGE STRUCTURE

Note:Cutting burr of lead are 0.05mm MAX.

SONY CODE	VQFN-22P-01
JEITA CODE	————
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
TERMINAL TREATMENT	SOLDER PLATING
TERMINAL MATERIAL	COPPER ALLOY
PACKAGE MASS	0.02g

AP-4000-22007S Rev. 0

LEAD PLATING SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	COPPER ALLOY
SOLDER COMPOSITION	Sn-Bi Bi:1-4wt%
PLATING THICKNESS	5-18µm