SONY

SP4T Antenna Switch for GSM / CDMA / UMTS

CXM3569XR

Description

The CXM3569XR is a high power SP4T antenna switch for GSM / CDMA / UMTS applications.
The antenna port can be routed to either of the 4TRx ports.
The low insertion loss on transmit means increased talk time as the Tx power amplifier can be operated at a lower output level.
Built-in decoder reduces component count and simplifies PCB layout by allowing direct connection of the switch to digital base band control lines with the 1.8 V CMOS logic levels.
The Sony GaAs JPHEMT MMIC Process is used for low insertion loss and high linearity.

Features

◆Low Insertion Loss: 0.31 dB typical (Cellular / GSM Low Band)
0.41 dB typical (PCS / GSM High Band)
0.46 dB typical (IMT2000)

◆High Linearity: IIP3=70 dBm

◆No DC Blocking Capacitors Required on RF ports.

◆Small Package Size: XQFN-20P (2.5 mm × 2.5 mm × 0.35 mm Typ.)

◆Lead-Free and RoHS Compliant

Structure

GaAs JPHEMT MMIC

Absolute Maximum Ratings

◆Bias Voltage	Vdd	4 V (Ta = 25 °C)
◆Control Voltage	Vctl	3.6 V (Ta = 25 °C)
◆Maximum input power	[Ant, RF1, RF2, RF3, RF4]	35 dBm (410 to 2690 MHz, Ta = 25 °C)
◆Operating Temperature		-35 °C to +90 °C
◆Storage Temperature		-65 °C to +150 °C
◆Maximum power dissipation	PD	500 mW
◆Copper-clad lamination of glass board(4 layer)		30 mm, t=0.8 mm, FR-4

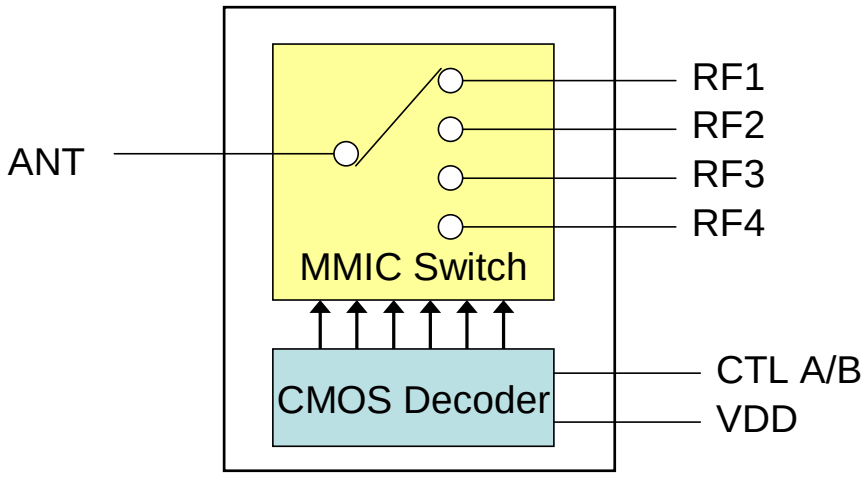
*NOTICE

Please use this product without exceeding PD value showed on it's specification. If it is used with exceeding PD value even for a moment, there are possibilities of degradation or breakdown because of the heat generated by product operation.

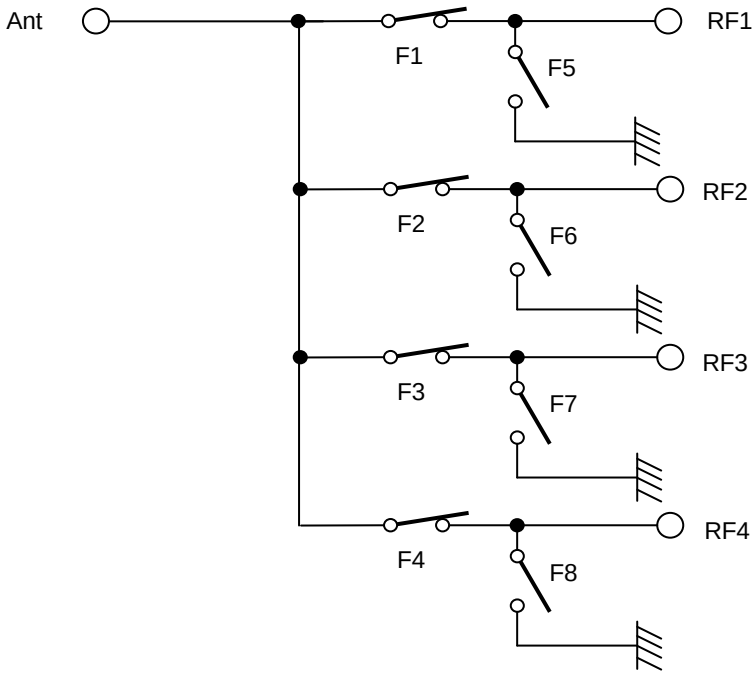
GaAs MMICs are ESD sensitive devices. Special handling precautions are required.

E12413B2Z

Block Diagram



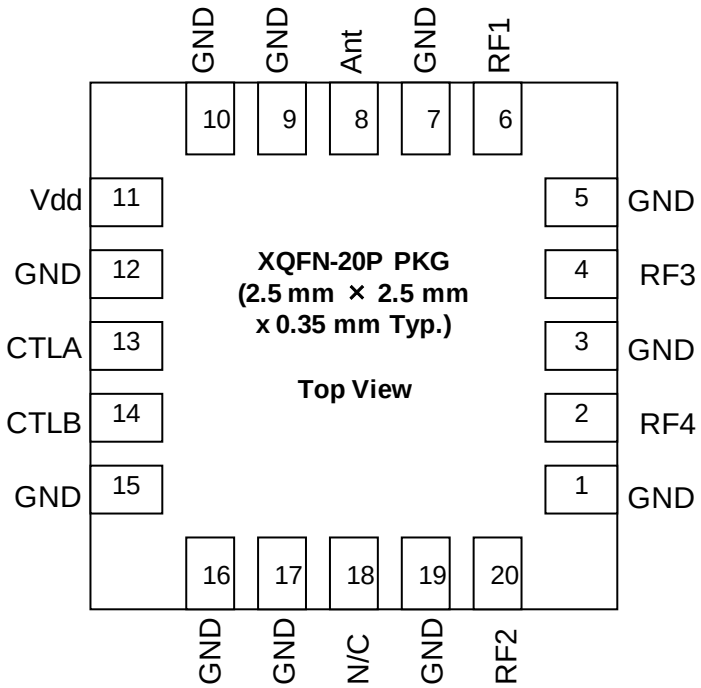
Block Diagram of RF Switch



Truth Table

ON Path	CTLA	CTLB	F1	F2	F3	F4	F5	F6	F7	F8
ANT – RF1	L	L	ON	OFF	OFF	OFF	OFF	ON	ON	ON
ANT – RF2	H	L	OFF	ON	OFF	OFF	ON	OFF	ON	ON
ANT – RF3	L	H	OFF	OFF	ON	OFF	ON	ON	OFF	ON
ANT – RF4	H	H	OFF	OFF	OFF	ON	ON	ON	ON	OFF

Pin Configuration



DC Bias Conditions

Ta = 25 °C

Parameter	Min.	Typ.	Max.	Unit
Vdd	2.5	2.8	3.3	V
Vctl(H)	1.35	1.8	3.3	V
Vctl(L)	0	-	0.3	V

Electrical Characteristics 1

Vdd = 2.5 V, Vctl = 0/1.8 V Ta = 25 °C

Item	Symbo	Path	Condition	Min.	Typ.	Max.	Unit
Insertion Loss	IL	ANT – RF1	*1	-	0.31	0.46	dB
			*2	-	0.41	0.56	
			*3	-	0.41	0.56	
			*4	-	0.46	0.66	
		ANT – RF2	*1	-	0.33	0.48	
			*2	-	0.43	0.58	
			*3	-	0.43	0.58	
			*4	-	0.46	0.66	
		ANT – RF3	*1	-	0.32	0.47	
			*2	-	0.42	0.57	
			*3	-	0.42	0.57	
			*4	-	0.46	0.66	
		ANT – RF4	*1	-	0.35	0.50	
			*2	-	0.45	0.60	
			*3	-	0.45	0.60	
			*4	-	0.49	0.69	
Isolation	ISO.	ANT – RF1	*1	25	30	-	dB
			*2	19	23	-	
			*3	18	22	-	
			*4	16	20	-	
		ANT – RF2, 3, 4	*1	30	36	-	
			*2	24	29	-	
			*3	23	28	-	
			*4	20	25	-	

Electrical Characteristics are measured with all RF ports terminated in 50 Ω.

* 1 freq = 698 to 960 MHz
* 2 freq = 1710 to 1990 MHz
* 3 freq = 2110 to 2170 MHz
* 4 freq = 2500 to 2690 MHz

Electrical Characteristics 2

Vdd = 2.5 V, Vctl = 0/1.8 V Ta = 25 °C

Item	Symbo	Path	Condition	Min.	Typ.	Max.	Unit
VSWR	VSWR		698 to 2170 MHz	-	1.1	1.4	-
			2500 to 2690 Mhz	-	1.2	1.6	
Harmonics	2fo		*1	-	-52	-36	dBm
	3fo			-	-43	-36	
	2fo		*2	-	-55	-40	
	3fo			-	-52	-40	
	2fo		*3	-	-63	-40	
	3fo			-	-63	-40	
	2fo		*4	-	-63	-40	
	3fo			-	-60	-40	
$P_{0.2dB}$ Compression	$P_{0.2dB}$	ANT-RF1, 2, 3,	824 to 1980 MHz	33	-	-	dBm
Inter Modulation Product Power in Rx Band	IMD2	ANT-RF1, 2, 3, 4	*5 -*8, *15	-	-115	-105	dBm
	IMD3		*9 -*12, *15	-	-115	-105	
Input IP3	IIP3	ANT-RF1, 2, 3, 4	*13, *15	65	70	-	dBm
			*14, *15	65	70	-	
Control Current	Ictl		Vctl = 1.8 V per line	-	0.005	1	µA
Supply Current	Idd		Vdd = 2.5 V	-	145	250	µA
Switching Time	Swt	RF1, 2, 3, 4	50 % Ctl to 90 % RF	-	3	5	µs
Wakeup Time	Wkt	RF1, 2, 3, 4	Wakeup time from Vdd on to Active mode	-	20	40	µs

Electrical Characteristics are measured with all RF ports terminated in 50 Ω.

Corresponding Band of TRx (UMTS/CDMA)

* 1 Pin = 35 dBm, freq = 824 to 915 MHz
* 2 Pin = 32 dBm, freq = 1710 to 1910 MHz
* 3 Pin = 27 dBm, freq = 1920 to 1980 MHz
* 4 Pin = 27 dBm, freq = 2500 to 2570 MHz
* 5 Pin on RF: 20 dBm, 1950 MHz, Pin on ANT: -15 dBm, 190 MHz
* 6 Pin on RF: 20 dBm, 1745 MHz, Pin on ANT: -15 dBm, 95 MHz
* 7 Pin on RF: 20 dBm, 1880 MHz, Pin on ANT: -15 dBm, 80 MHz
* 8 Pin on RF: 20 dBm, 835 MHz, Pin on ANT: -15 dBm, 45 MHz
* 9 Pin on RF: 20 dBm, 1950 MHz, Pin on ANT: -15 dBm, 1760 MHz
* 10 Pin on RF: 20 dBm, 1745 MHz, Pin on ANT: -15 dBm, 1650 MHz
* 11 Pin on RF: 20 dBm, 1880 MHz, Pin on ANT: -15 dBm, 1800 MHz
* 12 Pin on RF: 20 dBm, 835 MHz, Pin on ANT: -15 dBm, 790 MHz
* 13 Pin = 27 + 27 dBm, 835 + 836 MHz, IIP3=(3*Pout-IM3)/2+Loss
* 14 Pin = 27 + 27 dBm, 1950 + 1951 MHz, IIP3=(3*Pout-IM3)/2+Loss
* 15 Measured with the recommended circuit

Electrical Characteristics 3

Vdd = 2.5 V, Vctl = 0/1.8 V Ta = 25 °C

Item	Symbol	Path	Condition					Min.	Typ.	Max.
			P_{Tx} at RF*			Jammer at Ant -30dBm [MHz]	Triple Beat Product at RF* [MHz]			
			Pin [dBm]	PTx1 [MHz]	PTx2 [MHz]					
Triple Beat Ratio	TBR	ANT - RF1, RF2, RF3, RF4	21.5	835.5	836.5	881.5	881.5±1	81	-	-
			21.5	1880	1881	1960	1960±1	81	-	-
			13.5	1732	1733	2132	2132±1	81	-	-

Electrical Characteristics are measured with all RF ports terminated in 50 Ω.

Measured with the recommended circuit

Electrical Characteristics 4

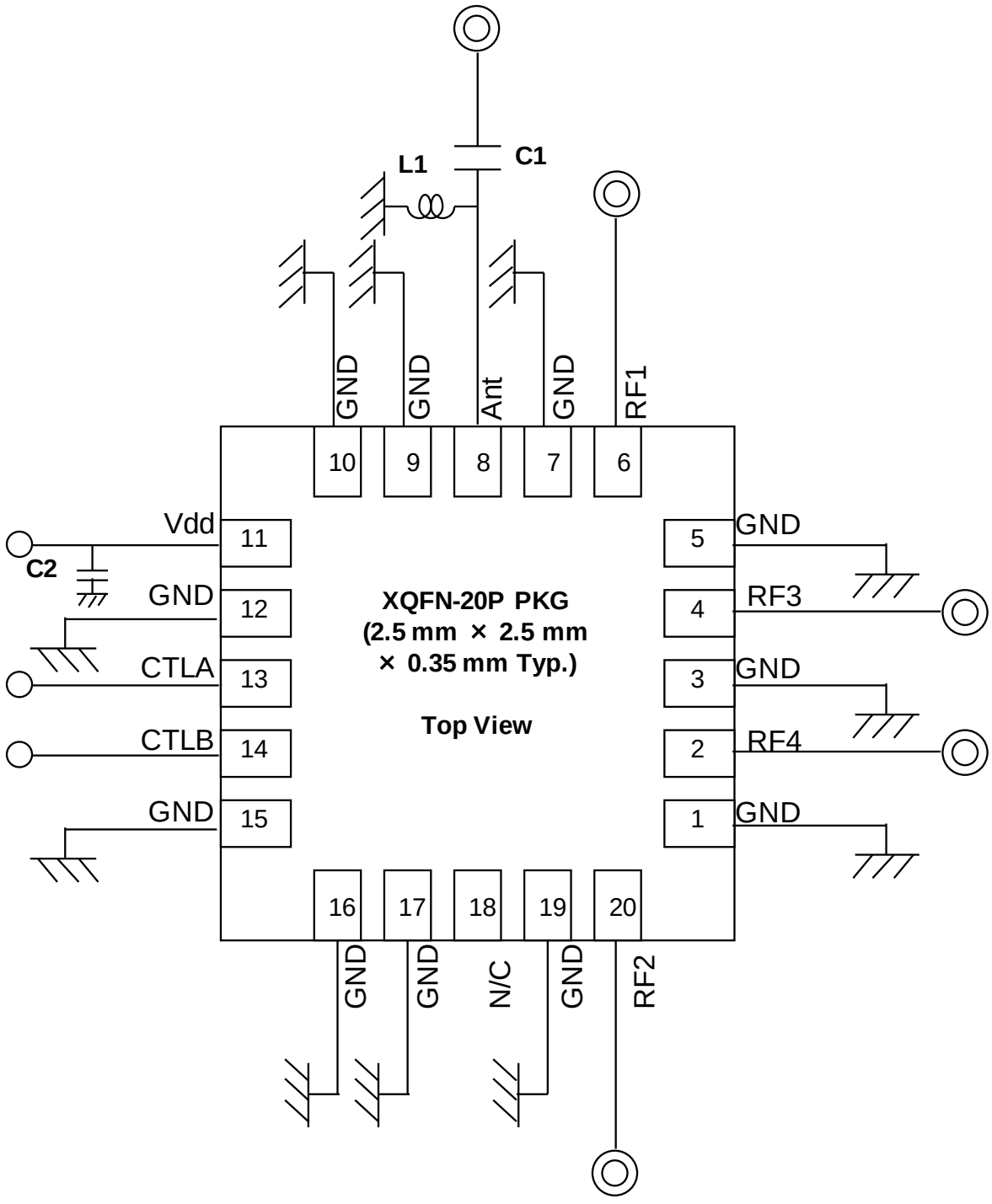
Vdd = 2.5 V, Vctl = 0/1.8 V Ta = 25 °C

Item	Symbol	Path	Condition			Min.	Typ.	Max.	Unit
			P_{Tx} at RF* 24dBm [MHz]	Jammer at ANT -20dBm	IM2 Product at RF* [MHz]				
Input IP2	IIP2	Ant - RF1, RF2, RF3, RF4	836.61	1718.61	881.61	113.5	-	-	dBm
			836.61	45	881.61	95.5	-	-	
			1885	3850	1965	95.5	-	-	
			1885	80	1965	95.5	-	-	
			1732.5	3865	2132.5	95.5	-	-	
			1732.5	400	2132.5	95.5	-	-	

Electrical Characteristics are measured with all RF ports terminated in 50 Ω.

Measured with the recommended circuit

Recommended Circuit



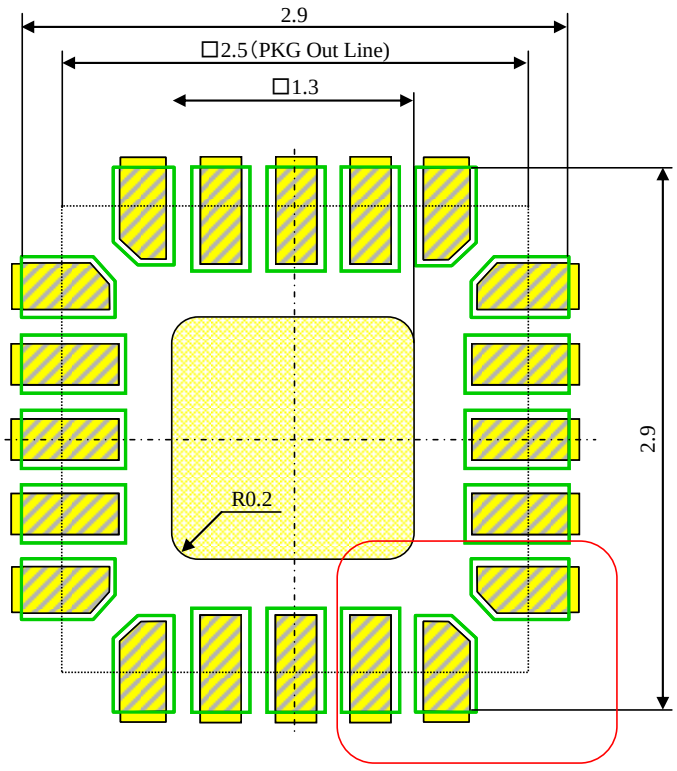
1: No DC blocking capacitors are required on all RF ports.
*2: DC levels of all RF ports are GND.
*3: L1(39 nH) and C1(15 pF) are recommended on Ant port for ESD protection.
*4: C2(100 pF) is recommended on Vdd pin for Decoupling Capacitor.

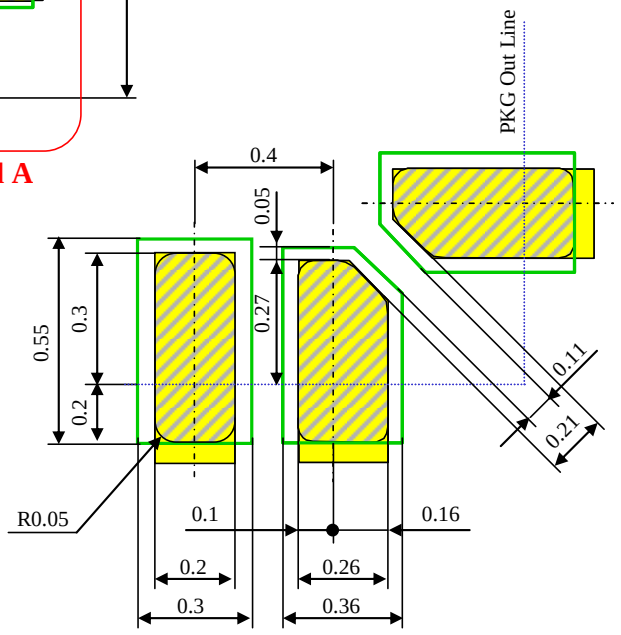
Recommended Land Pattern

XQFN-20P-02 Macro for MMIC

- PKG Size : □2.5mm × t0.35mm
- Terminal Pitch : 0.4mm
- Terminal Length : 0.3mm
- Mask thickness : 0.11mm

:Land area　:Mask open area (Solder printing area)
:Board resist open area　:Metal area in board (*1)
:PKG Outline





※R0.05:Mask corner

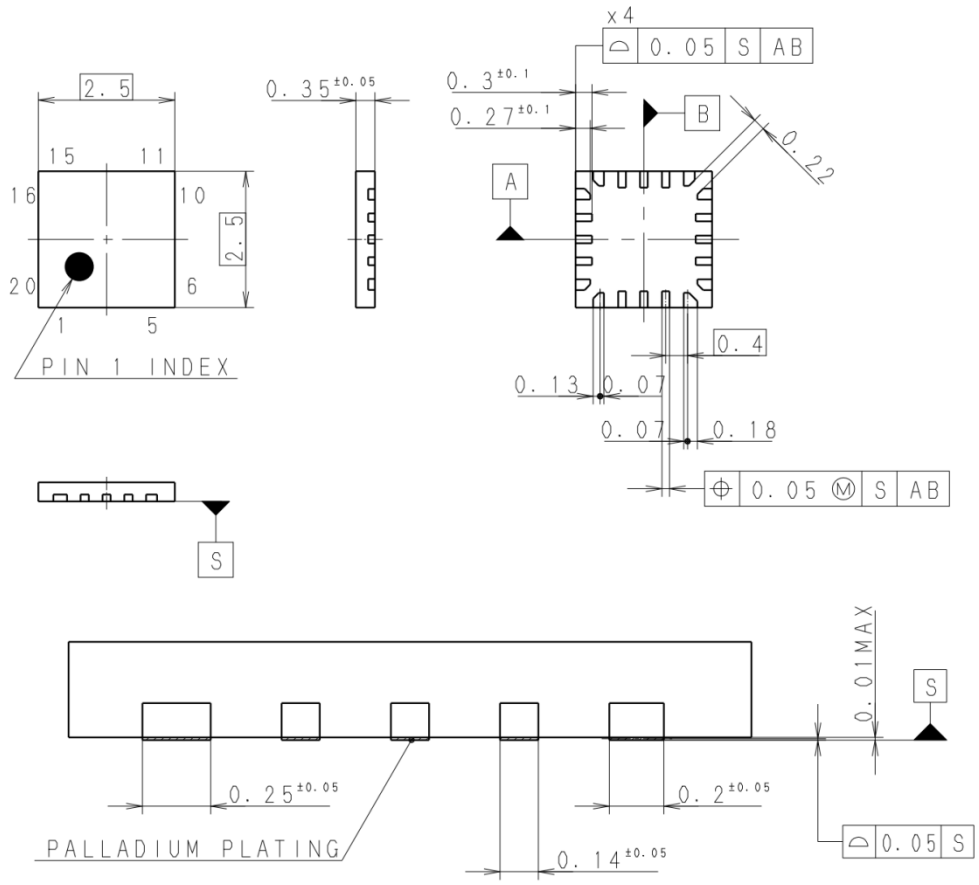
Detail A

Package Outline

(Unit: mm)

Product Code: 875341510

20PIN XQFN (PLASTIC)



TERMINAL SECTION

Note:Terminal burr Height 0.05mm MAX.

SONY CODE	XQFN-20P-052
JEITA CODE	————
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
TERMINAL TREATMENT	PALLADIUM PLATING
TERMINAL MATERIAL	COPPER ALLOY
PACKAGE MASS	0.006g

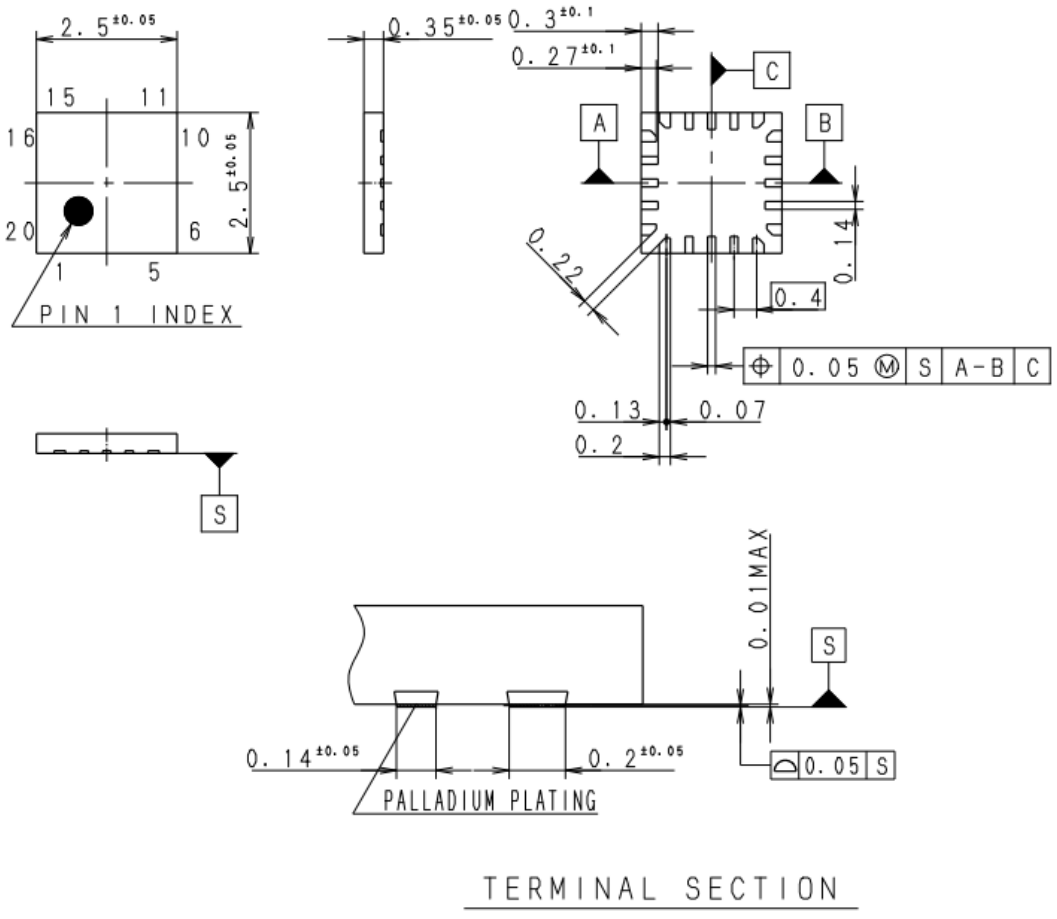
PART No. AP-2000-20XND2	Rev. 0
ISSUED 11.12.01	REVISED
PRODUCTION LINE	COMPILING DIV. SONY SEMICONDUCTOR.
REMARKS PKG CODE:XR-20-HD	

Package Outline

(Unit: mm)

Product Code: 875342678

20PIN XQFN (PLASTIC)



TERMINAL SECTION

Note:Terminal burr Height 0.05mm MAX.

SONY CODE	XQFN-20P-02
JEITA CODE	————
JEDEC CODE	————

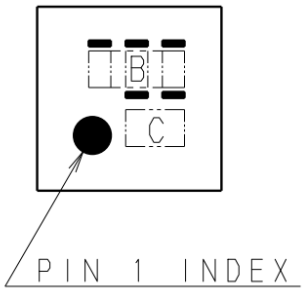
PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
TERMINAL TREATMENT	PALLADIUM PLATING
TERMINAL MATERIAL	COPPER ALLOY
PACKAGE MASS	0.006g

PART No. AP-4000-20023S1		Rev. 0
ISSUED 10.06.30	REVISED	
PRODUCTION LINE	COMPILING DIV. SONY SEMICONDUCTOR KYUSHU.	
REMARKS PKG CODE:XR-020-C For Specific Customer		

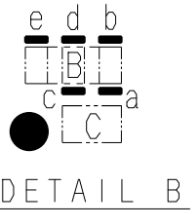
Marking

Product Code: 875341510



MARKING C : GH

注1） B部はロット番号（Ｍａｘ３文字で通し記号）を配置する。
（規定文字数未満につき省略は省略規定に従う。
製造年は下記２進法ビット方式により表示する。）
ａ部年コード（２進法ビット方式の１ビット目を表示）を配置する。
ｂ部年コード（２進法ビット方式の２ビット目を表示）を配置する。
ｃ部年コード（２進法ビット方式の３ビット目を表示）を配置する。
ｄ部年コード（２進法ビット方式の４ビット目を表示）を配置する。
注2） C部は製品名（Ｍａｘ２文字）を配置する。
（２文字を超える場合は製品名省略標示規定に従う。）
注3） マーク深さは，Ｍａｘ０．０５ｍｍの事。
注4） ｅ部は組立場所表記を配置する。

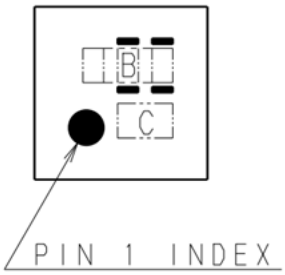


DETAIL B

< INSTRUCTIONS >
1) LOT NO. (MAX 3 CHARACTERS : SERIAL CODE) IN SECTION B.
(FOLLOW RULES FOR ABBREVIATIONS.
MANUFACTURING YEAR IS DISPLAYED BY FOLLOWING BYNARY BIT SYSTEM.)
A YEAR CODE(THE 1ST BIT OF A BINARY SYSTEM BIT SYSTEM IS DISPLAYED IN 1 DOT)IN SECTION a.
A YEAR CODE(THE 2ND BIT OF A BINARY SYSTEM BIT SYSTEM IS DISPLAYED IN 1 DOT)IN SECTION b.
A YEAR CODE(THE 3RD BIT OF A BINARY SYSTEM BIT SYSTEM IS DISPLAYED IN 1 DOT)IN SECTION c.
A YEAR CODE(THE 4TH BIT OF A BINARY SYSTEM BIT SYSTEM IS DISPLAYED IN 1 DOT)IN SECTION d.
2) TYPE NO.(MAX 2 CHARACTERS) IN SECTION C.
(FOR MORE THAN 2 CHARACTERS FOLLOW RULES FOR ABBREVIATIONS.)
3) MARK DEPTH MAX 0.05 mm.
4) ASSEMBLY PLACE IN SECTION e.

Marking

Product Code: 875342678



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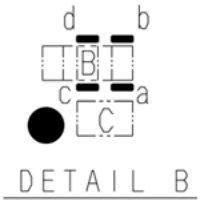

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Note

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