SONY

SP14T Antenna Switch Module for 12TRx/2Tx with MIPI I/F for Qualcomm chipset

CXM3617ER

Description

The CXM3617ER is a SP14T antenna switch module for GSM / UMTS / CDMA / LTE multi-mode handset.
The CXM3617ER has a +1.8 V CMOS compatible decoder with MIPI function for Qualcomm chipset.
The Sony GaAs junction gate pHEMT (JPHEMT) MMIC process is used for low insertion loss and high linearity. The device has low BOM with no DC blocking Capacitor.
(Applications: GSM/TD-SCDMA/WCDMA/LTE multi-mode handset)

Features

- Low Insertion Loss: 0.50 dB (Typ.) TRx (Cellular Band)
  0.70 dB (Typ.) TRx (IMT Tx Band)
- Low Voltage Operation: V_{DD} = 2.5 V
- Supports CMOS control for serial interface (MIPI I/F for Qualcomm chipset)
- No DC Blocking Capacitors
- Small Package Size: VQFN-26P (2.8 mm × 3.2 mm × 0.775 mm Max.)
- Lead-Free and RoHS Compliant

Structure

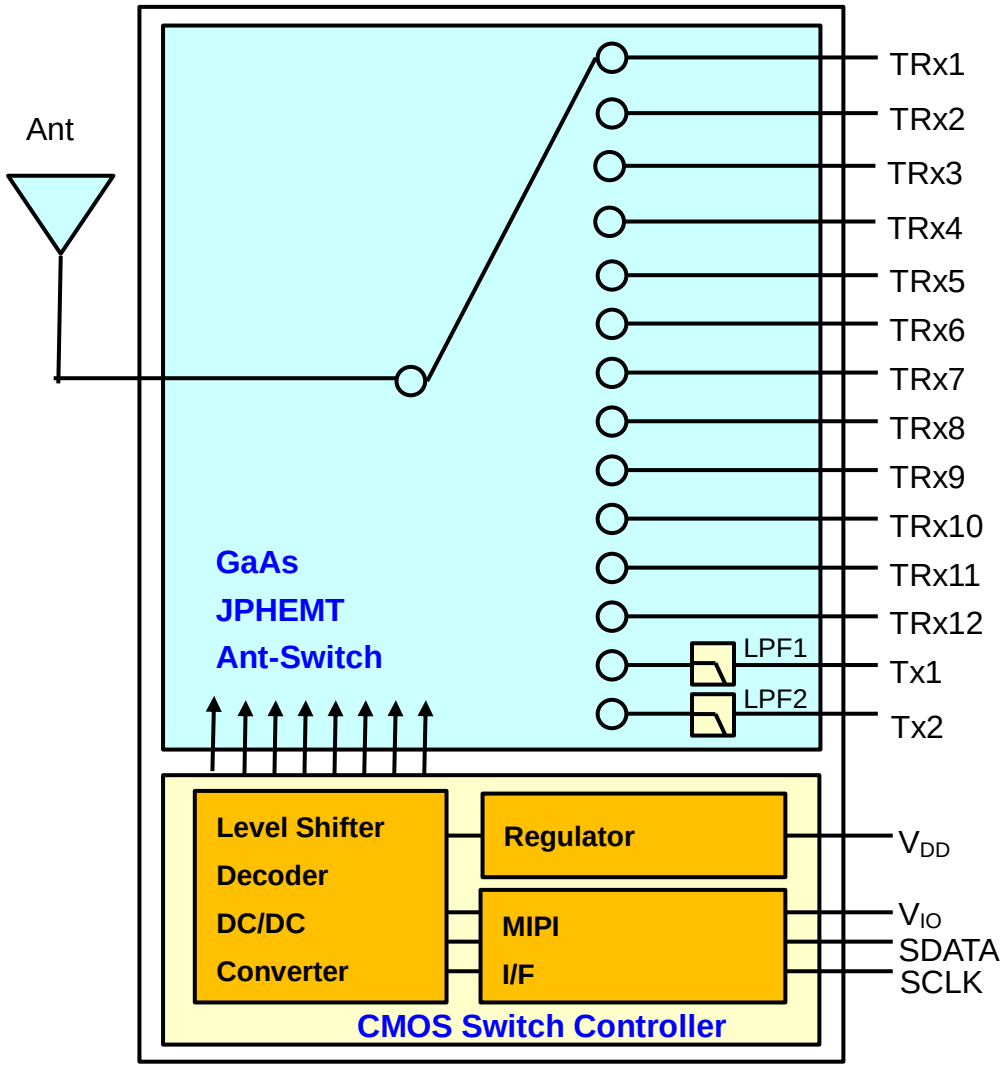
GaAs Junction Gate pHEMT (JPHEMT) MMIC Switch, CMOS Decoder

This IC is ESD sensitive device. Special handling precautions are required.

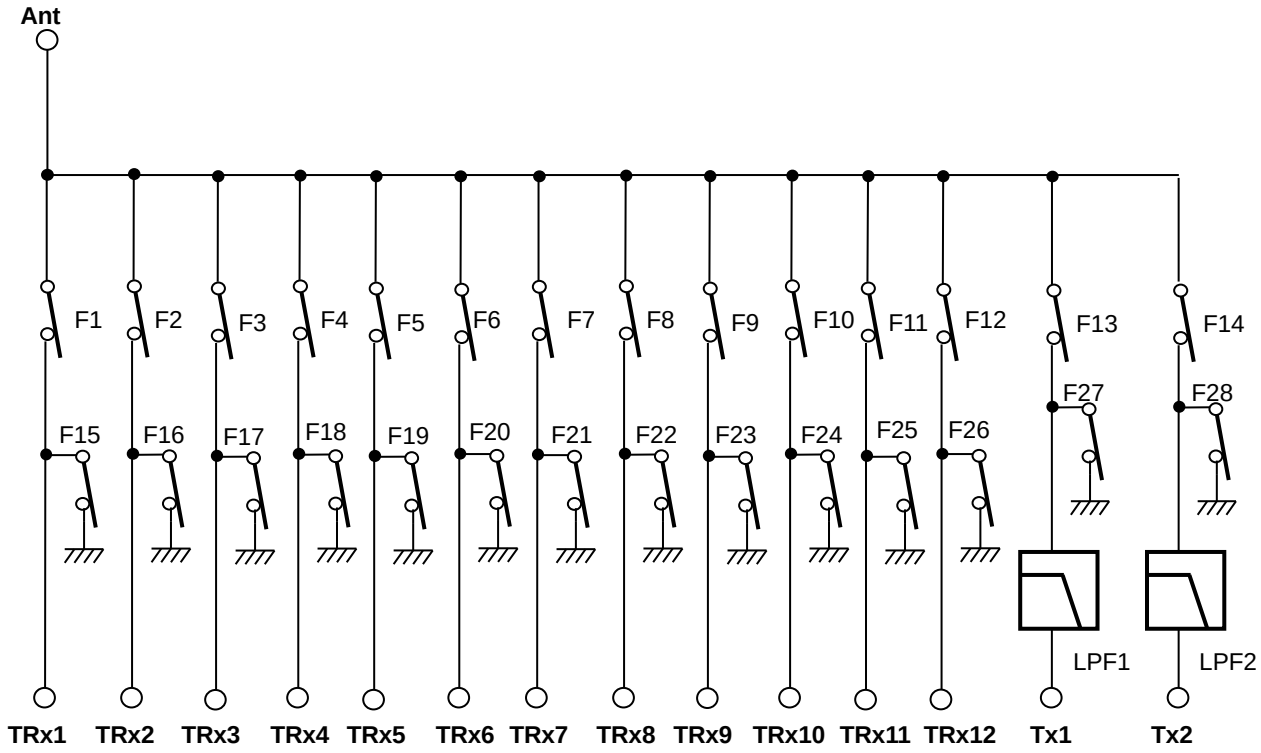
Absolute Maximum Ratings

◆Supply voltage	V_{DD}	6	V	(Ta = 25 °C)
◆Control voltage for MIPI	V_{IO}	2.5	V	(Ta = 25 °C)
	SDATA	2.5	V	(Ta = 25 °C)
	SCLK	2.5	V	(Ta = 25 °C)
◆Maximum input	[Tx1]	36	dBm	(Duty cycle = 12.5 % to 50 %) (Ta = 25 °C)
	[Tx2]	34	dBm	(Duty cycle = 12.5 % to 50 %) (Ta = 25 °C)
	[TRx]	32	dBm	(Ta = 25 °C)
◆Operating temperature	Topr	–35 to +90	°C	
◆Storage temperature	Tstg	–65 to +150	°C	

Block Diagram of SP14T Antenna Switch Module with MIPI



Block Diagram

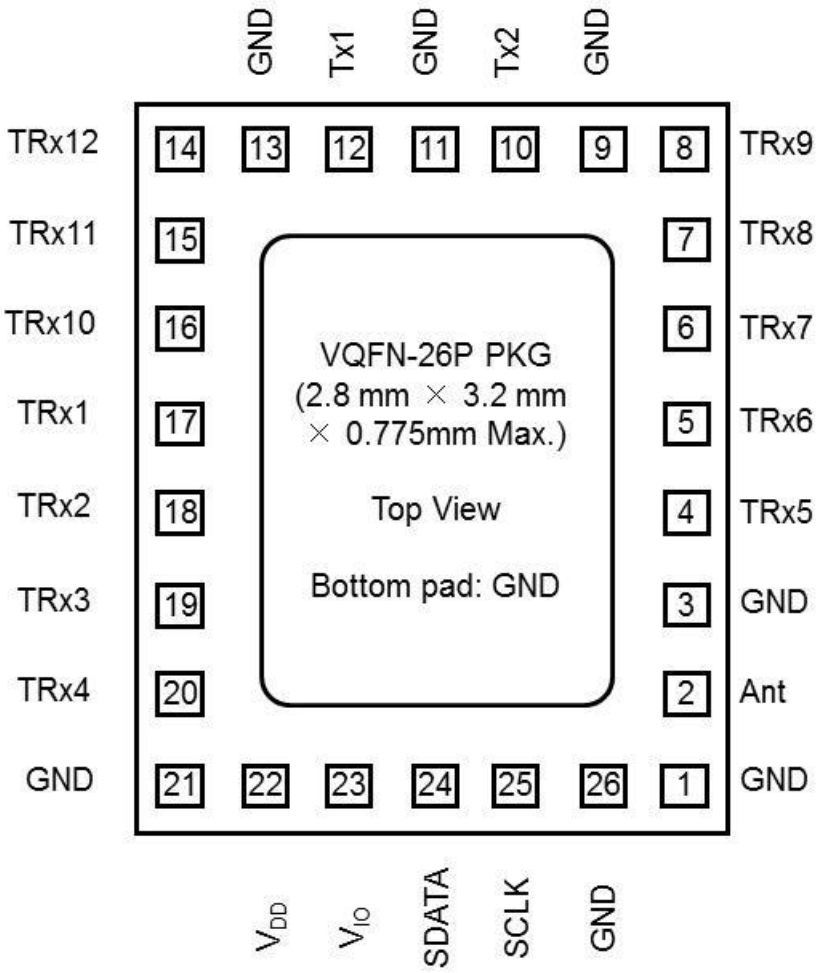


Truth Table

State	Path	Data Bits of Register 0							SW State (*1)																											
		D6	D5	D4	D3	D2	D1	D0	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10	F11	F12	F13	F14	F15	F16	F17	F18	F19	F20	F21	F22	F23	F24	F25	F26	F27	F28
1	TRx1	0	0	0	1	0	1	0	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H
2	TRx2	0	0	0	1	1	1	0	L	H	L	L	L	L	L	L	L	L	L	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H
3	TRx3	0	0	0	1	0	1	1	L	L	H	L	L	L	L	L	L	L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H
4	TRx4	0	0	0	0	1	0	1	L	L	L	H	L	L	L	L	L	L	L	L	L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H
5	TRx5	0	0	0	1	0	0	1	L	L	L	L	H	L	L	L	L	L	L	L	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H
6	TRx6	0	0	0	1	1	0	1	L	L	L	L	L	H	L	L	L	L	L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H
7	TRx7	0	0	0	0	0	0	1	L	L	L	L	L	L	H	L	L	L	L	L	L	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H
8	TRx8	0	0	0	0	0	1	1	L	L	L	L	L	L	L	H	L	L	L	L	L	L	H	H	H	H	H	H	H	L	H	H	H	H	H	H
9	TRx9	0	0	0	0	1	1	1	L	L	L	L	L	L	L	L	H	L	L	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H
10	TRx10	0	0	0	0	0	1	0	L	L	L	L	L	L	L	L	L	H	L	L	L	L	H	H	H	H	H	H	H	H	H	L	H	H	H	H
11	TRx11	0	0	0	0	1	1	0	L	L	L	L	L	L	L	L	L	L	H	L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H
12	TRx12	0	0	0	0	1	0	0	L	L	L	L	L	L	L	L	L	L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	H	L	H	H
13	Tx1	0	0	0	1	1	0	0	L	L	L	L	L	L	L	L	L	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H
14	Tx2	0	0	0	1	0	0	0	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
15	Isolation	0	0	0	0	0	0	0	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H

*1) State “L” means a switch “OFF”, state “H” means a switch “ON”.

Pin Configuration



Electrical Characteristics

V_{DD} = 2.5 V, Ta = 25 °C

Item	Symbol	Path	Condition	Min.	Typ.	Max.	Unit
Insertion Loss	IL	Ant - TRx1	*1, *2, *3, *10	-	0.51	0.61	dB
			*4, *11	-	0.57	0.67	
			*5	-	0.60	0.75	
			*6	-	0.66	0.86	
			*7	-	0.77	0.97	
		Ant - TRx2	*1, *2, *3, *10	-	0.51	0.61	
			*4, *11	-	0.59	0.69	
			*5	-	0.62	0.77	
			*6	-	0.67	0.87	
			*7	-	0.78	0.98	
		Ant - TRx3	*1, *2, *3, *10	-	0.52	0.62	
			*4, *11	-	0.58	0.68	
			*5	-	0.61	0.76	
			*6	-	0.67	0.87	
			*7	-	0.79	0.99	
		Ant - TRx4	*1, *2, *3, *10	-	0.39	0.49	
			*4, *11	-	0.46	0.56	
			*5	-	0.48	0.63	
			*6	-	0.54	0.74	
			*7	-	0.64	0.84	
		Ant - TRx5	*1, *2, *3, *10	-	0.41	0.51	
			*4, *11	-	0.63	0.73	
			*5	-	0.70	0.85	
			*6	-	0.83	1.03	
			*7	-	1.09	1.29	
		Ant - TRx6	*1, *2, *3, *10	-	0.47	0.57	
			*4, *11	-	0.64	0.74	
			*5	-	0.69	0.84	
			*6	-	0.80	1.00	
			*7	-	1.02	1.22	
		Ant - TRx7	*1, *2, *3, *10	-	0.52	0.62	
			*4, *11	-	0.60	0.70	
			*5	-	0.62	0.77	
			*6	-	0.68	0.88	
			*7	-	0.79	0.99	
		Ant - TRx8	*1, *2, *3, *10	-	0.50	0.60	
			*4, *11	-	0.56	0.66	
			*5	-	0.58	0.73	
			*6	-	0.62	0.82	
			*7	-	0.73	0.93	
		Ant - TRx9	*1, *2, *3, *10	-	0.51	0.61	
			*4, *11	-	0.55	0.65	
			*5	-	0.56	0.71	
			*6	-	0.60	0.80	
			*7	-	0.70	0.90	
		Ant - TRx10	*1, *2, *3, *10	-	0.58	0.68	
			*4, *11	-	0.72	0.82	
			*5	-	0.78	0.93	
			*6	-	0.91	1.11	
			*7	-	1.12	1.32	
		Ant - TRx11	*1, *2, *3, *10	-	0.55	0.65	
			*4, *11	-	0.69	0.79	
			*5	-	0.74	0.89	
			*6	-	0.86	1.06	
			*7	-	1.06	1.26	
		Ant - TRx12	*1, *2, *3, *10	-	0.54	0.64	
			*4, *11	-	0.70	0.80	
			*5	-	0.76	0.91	
			*6	-	0.89	1.09	
			*7	-	1.15	1.35	
		Ant - Tx1	*8	-	1.09	1.24	
		Ant - Tx2	*9	-	1.03	1.23	

V_{DD} = 2.5 V, Ta = 25 °C

Item	Symbol	Path	Condition	Min.	Typ.	Max.	Unit
VSWR	VSWR	All Ports in Active Paths	600 to 2170 MHz	-	-	1.50	-
Harmonics	2fo	Ant - TRx1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12	*3, *4	-	-65	-55	dBm
	3fo			-	-65	-55	
	2fo	Ant - Tx1	*8	-	-48	-36	
	3fo			-	-45	-40	
	2fo	Ant - Tx2	*9	-	-50	-45	
	3fo			-	-45	-36	
Attenuation	ATT	Tx1 - Ant	1648 to 1805 MHz	25	-	-	dB
			1805 to 1830 MHz	30	-	-	
			2472 to 2745 MHz	25	-	-	
			3296 to 12750 MHz	15	-	-	
		Tx2 - Ant	3420 to 3820 MHz	25	-	-	
			5130 to 5730 MHz	20	-	-	
			6840 to 12750 MHz	20	-	-	
Inter Modulation Product Power in Rx Band	IMD2	Ant - TRx1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12	*12, 13, 14, 17, 18, 21, 22	-	-	-105	dBm
	IMD3		*12, 15, 16, 19, 20, 23, 24	-	-	-105	
Input IP3	IIP3	Ant - TRx1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12	*12, 25, 26	-	68	-	
Switching Time	Ts	Ant - TRx1, 2, 3, 5, 6, 7, 8, 9, 10, 11, 12, Tx1, Tx2	SCLK falling edge to 90% RF in Active Mode	-	3	5	µs
		Ant - TRx4		-	4	6	µs
Wakeup Time	Tw		From Low Power Mode to Active Mode	-	-	100	µs
VIO Current	Ivio		V_{IO} = 1.80 V, Active Mode	-	0.20	0.40	mA
	Ivio		V_{IO} = 1.80 V, Low Power Mode	-	-	10	µA
Supply Current	Idd		V_{DD} = 2.5 V, Active Mode	-	0.20	0.40	mA
	Idd		V_{DD} = 2.5 V, Low Power Mode	-	-	10	µA

Isolation

Tx/TRx to Tx/TRx Isolation Matrix (Min.)

V_{DD} = 2.5 V, Ta = 25 °C

Active State	Freq. (MHz)	Isolation (dB)													
		Tx1	Tx2	TRx1	TRx2	TRx3	TRx4	TRx5	TRx6	TRx7	TRx8	TRx9	TRx10	TRx11	TRx12
Tx1	824 to 915		25	40	40	40	40	40	40	40	40	40	40	40	37
Tx2	1710 to 1910	24		40	40	40	40	30	37	40	40	40	40	38	32
TRx1	452 to 960	37	40		34	40	40	39	40	40	40	40	34	40	40
	1710 to 2170	34	35		24	31	32	29	37	40	40	40	24	30	33
	2300 to 2690	30	37		20	26	27	27	34	38	39	38	20	24	26
TRx2	452 to 960	39	40	32		31	40	39	40	40	40	40	40	40	40
	1710 to 2170	38	36	23		21	28	29	37	40	40	40	31	35	36
	2300 to 2690	33	37	19		18	23	27	34	38	40	39	26	28	28
TRx3	452 to 960	40	40	40	29		32	39	40	40	40	40	40	40	40
	1710 to 2170	40	36	29	20		21	29	37	40	40	40	35	37	37
	2300 to 2690	35	37	24	17		17	27	34	38	40	39	29	30	29
TRx4	452 to 960	40	40	40	40	31		39	40	40	40	40	40	40	40
	1710 to 2170	40	35	34	29	22		30	38	40	40	40	38	40	39
	2300 to 2690	38	35	28	24	18		27	34	37	39	38	33	33	31
TRx5	452 to 960	40	40	40	40	40	40		33	40	40	40	40	40	40
	1710 to 2170	40	40	40	40	40	35		22	31	37	40	40	40	39
	2300 to 2690	38	40	38	38	37	30		18	26	31	33	39	35	30
TRx6	452 to 960	40	40	40	40	40	40	32		34	40	40	40	40	40
	1710 to 2170	40	40	40	40	40	36	22		24	32	35	40	40	38
	2300 to 2690	37	38	38	39	38	30	17		19	27	29	39	35	30
TRx7	452 to 960	40	40	40	40	40	40	40	33		35	40	40	40	40
	1710 to 2170	40	36	40	40	40	40	31	24		25	31	40	40	39
	2300 to 2690	36	33	39	40	40	34	25	20		20	25	40	36	31
TRx8	452 to 960	40	40	40	40	40	40	40	40	33		33	40	40	40
	1710 to 2170	39	30	40	40	40	40	31	32	24		23	40	40	38
	2300 to 2690	33	27	39	40	40	35	27	27	20		19	39	35	30
TRx9	452 to 960	40	39	40	40	40	40	40	40	40	32		40	40	40
	1710 to 2170	35	27	40	40	40	40	31	35	29	22		40	40	36
	2300 to 2690	31	23	38	40	40	35	27	29	24	18		38	34	29
TRx10	452 to 960	32	36	33	40	40	40	39	40	40	40	40		31	40
	1710 to 2170	29	31	23	30	35	34	29	37	40	40	40		21	27
	2300 to 2690	26	32	18	25	29	29	27	34	37	38	35		17	21
TRx11	452 to 960	28	34	40	40	40	40	39	40	40	40	40	31		35
	1710 to 2170	25	31	29	33	37	35	29	37	40	40	40	20		23
	2300 to 2690	23	33	23	28	31	29	27	34	37	37	34	17		17
TRx12	452 to 960	24	33	40	40	40	40	39	40	40	40	40	40	34	
	1710 to 2170	20	30	31	35	37	35	29	37	40	40	40	27	22	
	2300 to 2690	18	34	25	29	31	29	27	34	36	36	33	23	17	

Corresponding Band of TRx (UMTS/CDMA/LTE)

*1 Pin = 26 dBm, 452 to 468 MHz (Band Class 5)

*2 Pin = 25 dBm, 704 to 787 MHz (Band 13, Band 17)

*3 Pin = 26 dBm, 824 to 960 MHz (Band 5, Band 8)

*4 Pin = 26 dBm, 1710 to 1990 MHz (Band 1 Tx, Band 2 Tx, Band 3 Tx, Band4 Tx)

*5 Pin = 10 dBm, 2110 to 2170 MHz (Band 1 Rx, Band 4 Rx)

*6 Pin = 26 dBm, 2300 to 2400 MHz (Band 40)

*7 Pin = 26 dBm, 2500 to 2690 MHz (Band 7)

*8 Pin = 35 dBm, 824 to 915 MHz (GSM850/900 Tx)

*9 Pin = 32 dBm, 1710 to 1910 MHz (GSM1800/1900 Tx)

*10 Pin = 10 dBm, 869 to 960 MHz (GSM850/900 Rx)

*11 Pin = 10 dBm, 1805 to 1990 MHz (GSM1800/1900 Rx)

*12 Measured with the recommended circuit

IMD Condition

Band	fRx on RF [MHz]	fTx +20 dBm on RF [MHz]	fBlocker -15 dBm on ANT [MHz]		IMD Condition
Band 1	2140	1950	IMD2 (fRx - fTx)	190	*13
			IMD2 (fRx + fTx)	4090	*14
			IMD3 (2fTx - fRx)	1760	*15
			IMD3 (2fTx + fRx)	6040	*16
Band 2	1960	1880	IMD2 (fRx - fTx)	80	*17
			IMD2 (fRx + fTx)	3840	*18
			IMD3 (2fTx - fRx)	1800	*19
			IMD3 (2fTx + fRx)	5720	*20
Band 5	880	835	IMD2 (fRx - fTx)	45	*21
			IMD2 (fRx + fTx)	1715	*22
			IMD3 (2fTx - fRx)	790	*23
			IMD3 (2fTx + fRx)	2550	*24

IIP3 Condition

Band	f1 +27 dBm on RF [MHz]	f2 +27 dBm on RF [MHz]	IIP3 Condition IIP3 = (3 × Pout - IMD3)/2 [dBm]
Band 1	1950	1951	*25
Band 5	835	836	*26

Electrical Characteristics of Triple Beat Ratio

V_{DD} = 2.5 V, Ta = 25 °C

Item	Symbol	Path	Condition				Min.	Typ.	Max.	Unit
			Tx1 at TRx 21.5 dBm [MHz]	Tx2 at TRx 21.5 dBm [MHz]	Jammer at ANT –30 dBm [MHz]	Triple Beat Product at TRx [MHz]				
Triple Beat Ratio	TBR	ANT-TRx1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12	835.5	836.5	881.5	881.5 ± 1	81	—	—	dBc
			1880	1881	1960	1960 ± 1	81	—	—	

Electrical characteristics are measured with all RF ports terminated in 50 Ω.
Measured with the recommended circuit

Electrical Characteristics of Input IP2

V_{DD} = 2.5 V, Ta = 25 °C

Item	Symbol	Path	Condition			Min.	Typ.	Max.	Unit
			Tx at TRx 24 dBm [MHz]	Jammer at ANT –20 dBm [MHz]	IM2 Product at TRx [MHz]				
Input IP2	IIP2	ANT-TRx1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12	836.61	1718.22	881.61	113.5	—	—	dBm
			836.61	45	881.61	95.5	—	—	
			1885	3850	1965	95.5	—	—	
			1885	80	1965	95.5	—	—	
			1732.5	3865	2132.5	95.5	—	—	
			1732.5	400	2132.5	95.5	—	—	

Electrical characteristics are measured with all RF ports terminated in 50 Ω.
Measured with the recommended circuit

MIPI Specification

Features

- PM_TRIG with three triggers
- Software reset and debug using the RFFE_STATUS register
- Register 0 write
- Full speed write, Half speed read
- GSID
- Programmable USID

Control Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{DD}	2.5	2.8	3.3	V
Supply current (ACTIVE) *V_{DD} = 2.5 V	IDD	-	200	400	µA
Supply current Low Power(disable) *V_{DD} = 2.5 V	IDD	-	-	10	µA
Interface Supply Voltage	V_{IO}	1.65	1.8	1.95	V
Supply current (ACTIVE) *V_{IO} = 1.8 V	Ivio	-	200	400	µA
Supply current Low Power(disable) *V_{IO} = 1.8 V	Ivio	-	-	10	µA
Signal level low	Vcl	0	-	0.2×V_{IO}	V
Signal level high	Vch	0.8×V_{IO}	-	V_{IO}	V
SCLK write Frequency	fSCLKw	0.032	19.2	26	MHz
SCLK read Frequency	fSCLKr	0.032	9.6	13	MHz
SDATA/SCLK input capacitance	Cin	-	2	3	pF
Data setup time	Ts	2	-	-	ns
Data hold time	Th	5	-	-	ns
Turn on Time *	Ton	-	-	100	µs

*Turn on time: Time to guarantee RF performance after switch activation.

Explanation of Register

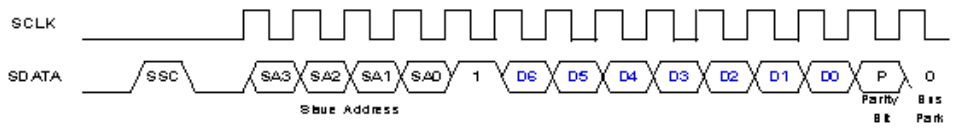
Slave Address: 1011

Register Address	Register Name	Data Bits	Notes	Read Write
0x0000	REGISTER_0 (Table A or B)	6:0	Antenna switch states (see Truth Table) Register 0 Write command sequence use. Trigger Supprt.	W
		7:0	Antenna switch states (see Truth Table) Read/Write command sequence use. Trigger Supprt.	R/W
0x001A	RFFE_STATUS (Table C)	7	SOFTWARE RESET	R/W
		6	COMMAND_FRAME_PARITY_ERR	
		5	COMMAND_LENGTH_ERR	
		4	ADDRESS_FRAME_PARITY_ERR	
		3	DATA_FRAME_PARITY_ERR	
		2	READ_UNUSED_REG	
		1	WRITE_UNUSED_REG	
		0	BID_GID_ERR	
0x001B	GROUP_ID (Table D)	7:4	RESERVED	R/W
		3:0	GROUP_SID	
0x001C	PM_TRIG (Table E)	7:6	Power mode	R/W
		5:3	Trigger_Mask_[2:0]	
		2:0	Trigger_[2:0]	
0x001D	PRODUCT_ID (Table F)	7:0	PRODUCT_ID	R
0x001E	MANUFACTURER_ID (Table G)	7:0	MANUFACTURER_ID[7:0]	R
0x001F	SPARE MANUFACTURER_ID USID (Table H)	7:6	SPARE	R
		5:4	MANUFACTURER_ID[9:8]	R
		3:0	USID	R/W

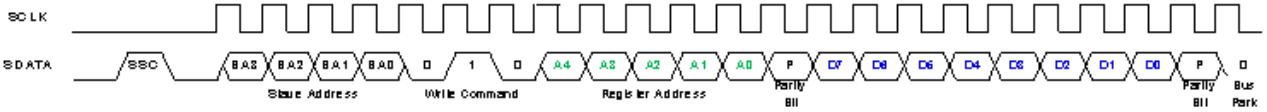
MANUFACTURER_ID[9:0] is defined by SONY ID (0x01B0)

Write and Read command sequence

– REGISTER_0 Write command sequence

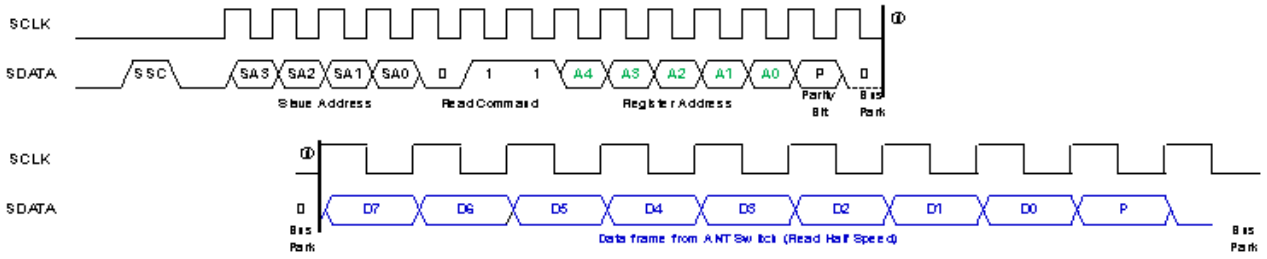


– Write command sequence (except REGISTER_0)



– Read command sequence

Data frame from ANT Switch needs Half Speed function



Register Map

・Register 0 Write command sequence use.

State	Path	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		SSC	-	Slave Address					Data							Parity Bit	Bus Park
		-	-	SA3	SA2	SA1	SA0	C0	D6	D5	D4	D3	D2	D1	D0	P	-
1	TRx1	1	0	1	0	1	1	1	0	0	0	1	0	1	0	1	0
2	TRx2	1	0	1	0	1	1	1	0	0	0	1	1	1	0	0	0
3	TRx3	1	0	1	0	1	1	1	0	0	0	1	0	1	1	0	0
4	TRx4	1	0	1	0	1	1	1	0	0	0	0	1	0	1	1	0
5	TRx5	1	0	1	0	1	1	1	0	0	0	1	0	0	1	1	0
6	TRx6	1	0	1	0	1	1	1	0	0	0	1	1	0	1	0	0
7	TRx7	1	0	1	0	1	1	1	0	0	0	0	0	0	1	0	0
8	TRx8	1	0	1	0	1	1	1	0	0	0	0	0	1	1	1	0
9	TRx9	1	0	1	0	1	1	1	0	0	0	0	1	1	1	0	0
10	TRx10	1	0	1	0	1	1	1	0	0	0	0	0	1	0	0	0
11	TRx11	1	0	1	0	1	1	1	0	0	0	0	1	1	0	1	0
12	TRx12	1	0	1	0	1	1	1	0	0	0	0	1	0	0	0	0
13	Tx1	1	0	1	0	1	1	1	0	0	0	1	1	0	0	1	0
14	Tx2	1	0	1	0	1	1	1	0	0	0	1	0	0	0	0	0
15	Isolation	1	0	1	0	1	1	1	0	0	0	0	0	0	0	1	0

・Register Read/Write command sequence use.

State	Path	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10
		SSC	-	Slave Address				Write/ Read Command Write:010 Read:011			Register Address					Parity Bit
		-	-	SA3	SA2	SA1	SA0	C2	C1	C0	A4	A3	A2	A1	A0	P
1	TRx1	1	0	1	0	1	0	0	1	1/0	0	0	0	0	0	1/0
2	TRx2	1	0	1	0	1	0	0	1	1/0	0	0	0	0	0	1/0
3	TRx3	1	0	1	0	1	0	0	1	1/0	0	0	0	0	0	1/0
4	TRx4	1	0	1	0	1	0	0	1	1/0	0	0	0	0	0	1/0
5	TRx5	1	0	1	0	1	0	0	1	1/0	0	0	0	0	0	1/0
6	TRx6	1	0	1	0	1	0	0	1	1/0	0	0	0	0	0	1/0
7	TRx7	1	0	1	0	1	0	0	1	1/0	0	0	0	0	0	1/0
8	TRx8	1	0	1	0	1	0	0	1	1/0	0	0	0	0	0	1/0
9	TRx9	1	0	1	0	1	0	0	1	1/0	0	0	0	0	0	1/0
10	TRx10	1	0	1	0	1	0	0	1	1/0	0	0	0	0	0	1/0
11	TRx11	1	0	1	0	1	0	0	1	1/0	0	0	0	0	0	1/0
12	TRx12	1	0	1	0	1	0	0	1	1/0	0	0	0	0	0	1/0
13	Tx1	1	0	1	0	1	0	0	1	1/0	0	0	0	0	0	1/0
14	Tx2	1	0	1	0	1	0	0	1	1/0	0	0	0	0	0	1/0
15	Isolation	1	0	1	0	1	0	0	1	1/0	0	0	0	0	0	1/0

State	Path	9	8	7	6	5	4	3	2	1	0
		Data								Parity Bit	Bus Park
		D7	D6	D5	D4	D3	D2	D1	D0	P	-
1	TRx1	0	0	0	0	1	0	1	0	1	0
2	TRx2	0	0	0	0	1	1	1	0	0	0
3	TRx3	0	0	0	0	1	0	1	1	0	0
4	TRx4	0	0	0	0	0	1	0	1	1	0
5	TRx5	0	0	0	0	1	0	0	1	1	0
6	TRx6	0	0	0	0	1	1	0	1	0	0
7	TRx7	0	0	0	0	0	0	0	1	0	0
8	TRx8	0	0	0	0	0	0	1	1	1	0
9	TRx9	0	0	0	0	0	1	1	1	0	0
10	TRx10	0	0	0	0	0	0	1	0	0	0
11	TRx11	0	0	0	0	0	1	1	0	1	0
12	TRx12	0	0	0	0	0	1	0	0	0	0
13	Tx1	0	0	0	0	1	1	0	0	1	0
14	Tx2	0	0	0	0	1	0	0	0	0	0
15	Isolation	0	0	0	0	0	0	0	0	1	0

*Parity Bit

A Frame shall end with a single parity bit. The parity bit shall be driven such that the total number of bits in the Frame that are driven to logic level one, including the parity bit, is odd.

Table A REGISTER_0 for ANT Switch State (0x0000)

	Items		Bit	Description	
Command Frame	Slave Address	SA3	1	Address of Antenna Switch Module	
		SA2	0		
		SA1	1		
		SA0	1		
		C0	1	REGISTER_0 Write : 1	
	Data	D6	0	Switch State See the truth table Trigger Supprt.	Initial value : [D6:D0] =000 0000
		D5	0		
		D4	0		
		D3	0/1		
		D2	0/1		
		D1	0/1		
		D0	0/1		
	Parity Bit	P	0/1	Parity bit for Frame	

Table B REGISTER_0 for ANT Switch State (0x0000)

	Items		Bit	Description	
Command Frame	Slave Address	SA3	1	Address of Antenna Switch Module	
		SA2	0		
		SA1	1		
		SA0	1		
	Read Write	C2	0	Write : 010 Read: 011	
		C1	1		
		C0	0/1		
	Register Address	A4	0	Register Address: 0x0000	
		A3	0		
		A2	0		
		A1	0		
		A0	0		
	Parity Bit	P	0/1	Parity bit for Command Frame	
Data Frame	Data	D7	0	Switch State See the truth table Trigger Supprt.	Initial value : [D7:D0] =0000 0000
		D6	0		
		D5	0		
		D4	0		
		D3	0/1		
		D2	0/1		
		D1	0/1		
		D0	0/1		
	Parity Bit	P	0/1	Parity bit for Data Frame	

Table C RFFE_STATUS (0x001A)

	Items		Bit	Description	
Command Frame	Slave Address	SA3	1	Address of Antenna Switch Module	
		SA2	0		
		SA1	1		
		SA0	1		
	Read Write	C2	0	Write : 010 Read: 011	
		C1	1		
		C0	0/1		
	Register Address	A4	1	Register Address: 0x001A	
		A3	1		
		A2	0		
		A1	1		
		A0	0		
	Parity Bit	P	0/1	Parity bit for Command Frame	
Data Frame	Data	D7	0/1	0: Normal operation 1: Software reset (reset of all configurable registers to default values, except for USID、PM_TRIG、GSID)	Initial value : [D7:D0] =0000 0000
		D6	0/1	Command sequence received with parity error – discard command.	
		D5	0/1	Command length error	
		D4	0/1	Address frame parity error = 1	
		D3	0/1	Data frame with parity error	
		D2	0/1	Read command to an invalid address	
		D1	0/1	Write command to an invalid address	
		D0	0/1	Read command with a Broadcast ID or GROUP ID	
	Parity Bit	P	0/1	Parity bit for Data Frame	

All Data bits become 0 aftter Read Command Sequence is sent.

Table D GROUP_ID (0x001B)

Items			Bit	Description	
Command Frame	Slave Address	SA3	1	Address of Antenna Switch Module	
		SA2	0		
		SA1	1		
		SA0	1		
	Read Write	C2	0	Write : 010 Read: 011	
		C1	1		
		C0	0/1		
	Register Address	A4	1	Register Address: 0x001B	
		A3	1		
		A2	0		
		A1	1		
		A0	1		
	Parity Bit	P	0/1	Parity bit for Command Frame	
Data Frame	Data	D7	0	-	
		D6	0		
		D5	0		
		D4	0		
		D3	0/1	Group slave ID	Initial value : [D3:D0] =0000
		D2	0/1		
		D1	0/1		
		D0	0/1		
	Parity Bit	P	0/1	Parity bit for Data Frame	

Table E Register for Power Mode & Trigger Mode (0x001C)

Items			Bit	Description	
Command Frame	Slave Address	SA3	1	Address of Antenna Switch Module	
		SA2	0		
		SA1	1		
		SA0	1		
	Read Write	C2	0	Write : 010 Read: 011	
		C1	1		
		C0	0/1		
	Register Address	A4	1	Register Address: 0x001C	
		A3	1		
		A2	1		
		A1	0		
		A0	0		
	Parity Bit	P	0/1	Parity bit for Command Frame	
Data Frame	Data	D7	0/1	00: Normal operation (ACTIVE) 01: Default settings (STARTUP) 10: Low power (LOW POWER) 11: Reserved	Initial value : [D7:D6] =10
		D6	0/1		
		D5	0/1	Trigger_Mask_[2:0] 111: valid other: Invalid	Initial value : [D5:D3] =000
		D4	0/1		
		D3	0/1		
		D2	0/1	Trigger_[2:0] 000: Invalid other: valid	Initial value : [D2:D0] =000
		D1	0/1		
		D0	0/1		
	Parity Bit	P	0/1	Parity bit for Data Frame	

Table F Register for Product ID (0x001D)

Items			Bit	Description
Command Frame	Slave Address	SA3	1	Address of Antenna Switch Module
		SA2	0	
		SA1	1	
		SA0	1	
	Read Write	C2	0	Read Only
		C1	1	
		C0	1	
	Register Address	A4	1	Register Address: 0x001D
		A3	1	
		A2	1	
		A1	0	
		A0	1	
	Parity Bit	P	0	Parity bit for Command Frame
Data Frame	Data	D7	0	Product ID : 06h
		D6	0	
		D5	0	
		D4	0	
		D3	0	
		D2	1	
		D1	1	
		D0	0	
	Parity Bit	P	1	Parity bit for Data Frame

Table G Register for Manufacturer ID (0x001E)

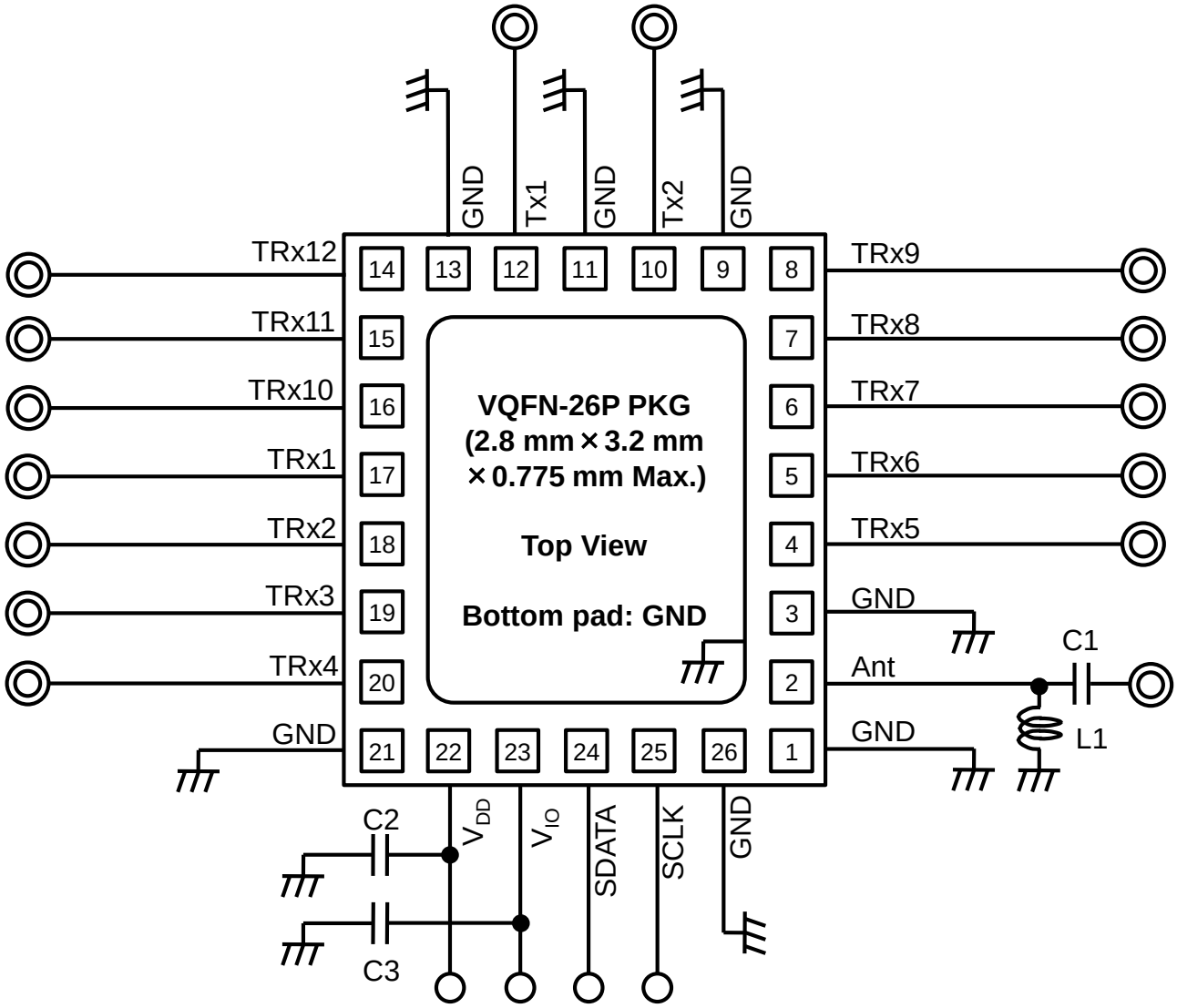
	Items		Bit	Description
Command Frame	Slave Address	SA3	1	Address of Antenna Switch Module
		SA2	0	
		SA1	1	
		SA0	1	
	Read Write	C2	0	Read Only
		C1	1	
		C0	1	
	Register Address	A4	1	Register Address: 0x001E
		A3	1	
		A2	1	
		A1	1	
		A0	0	
	Parity Bit	P	0	Parity bit for Command Frame
Data Frame	Data	D7	1	Manufacturer ID [7:0]:B0h (SONY ID)
		D6	0	
		D5	1	
		D4	1	
		D3	0	
		D2	0	
		D1	0	
		D0	0	
	Parity Bit	P	0	Parity bit for Data Frame

Table H Register for Manufacturer ID and USID (0x001F)

	Items		Bit	Description	
Command Frame	Slave Address	SA3	1	Address of Antenna Switch Module	
		SA2	0		
		SA1	1		
		SA0	1		
	Read Write	C2	0	Write : 010 Read : 011	
		C1	1		
		C0	0/1		
	Register Address	A4	1	Register Address: 0x001F	
		A3	1		
		A2	1		
		A1	1		
		A0	1		
	Parity Bit	P	0/1	Parity bit for Command Frame	
Data Frame	Data	D7	0	SPARE	
		D6	0		
		D5	0	Manufacturer ID [9:8]:01h (SONY ID)	
		D4	1		
		D3	0/1	Programmable USID	Initial value : [D3:D0] =1011
		D2	0/1		
		D1	0/1		
		D0	0/1		
	Parity Bit	P	0/1	Parity bit for Data Frame	

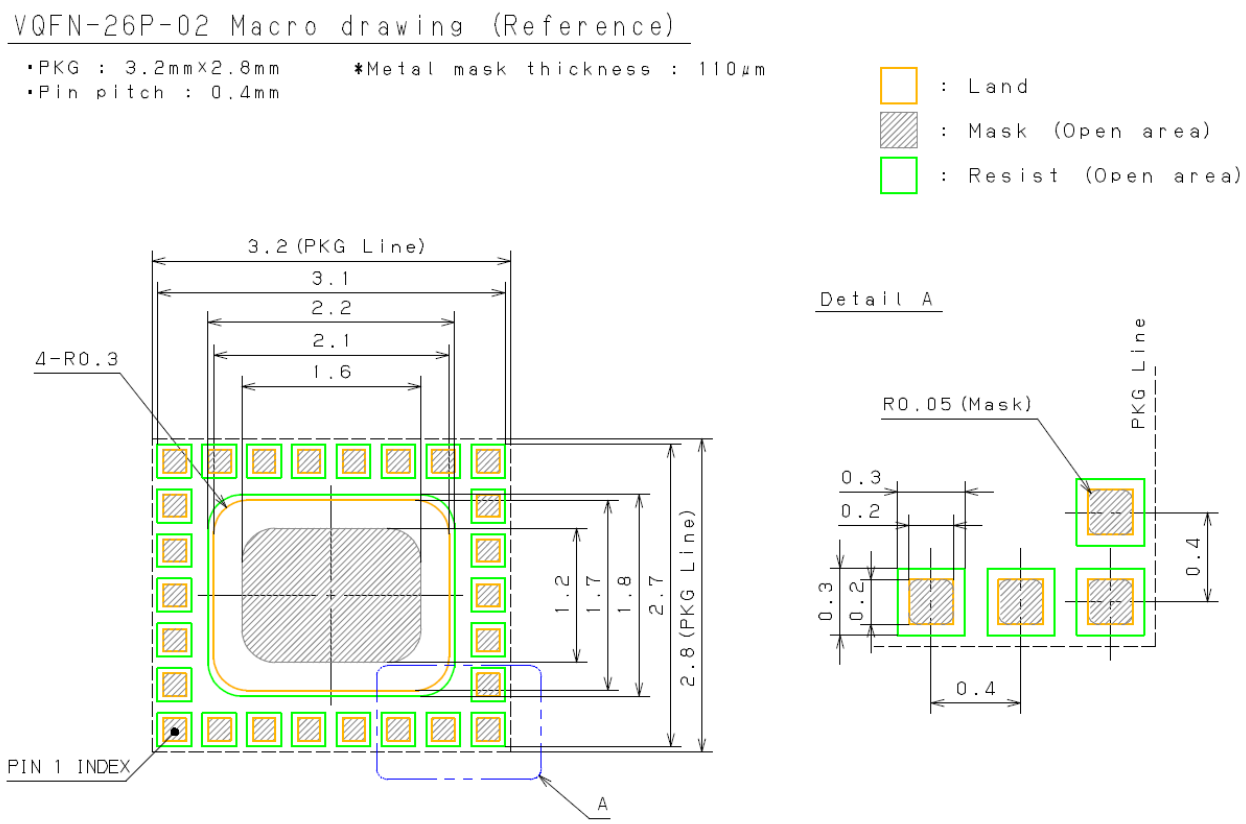
For Programmable USID
The PRODUCT_ID and the MANUFACTURER_ID match, then a new USID is programmed.

Recommended Circuit

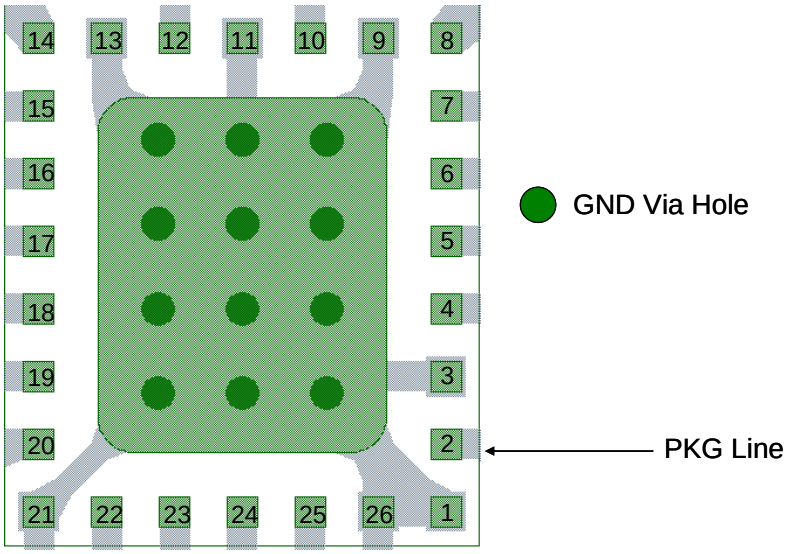


*1: No DC blocking capacitors are required on all RF ports.
*2: DC levels of all RF ports are GND.
*3: L1 (22 nH) and C1 (22 pF) are recommended on Ant port for ESD protection.
*4: C2 (100 pF) and C3 (0.1 µF) are recommended.

Recommended Land Pattern

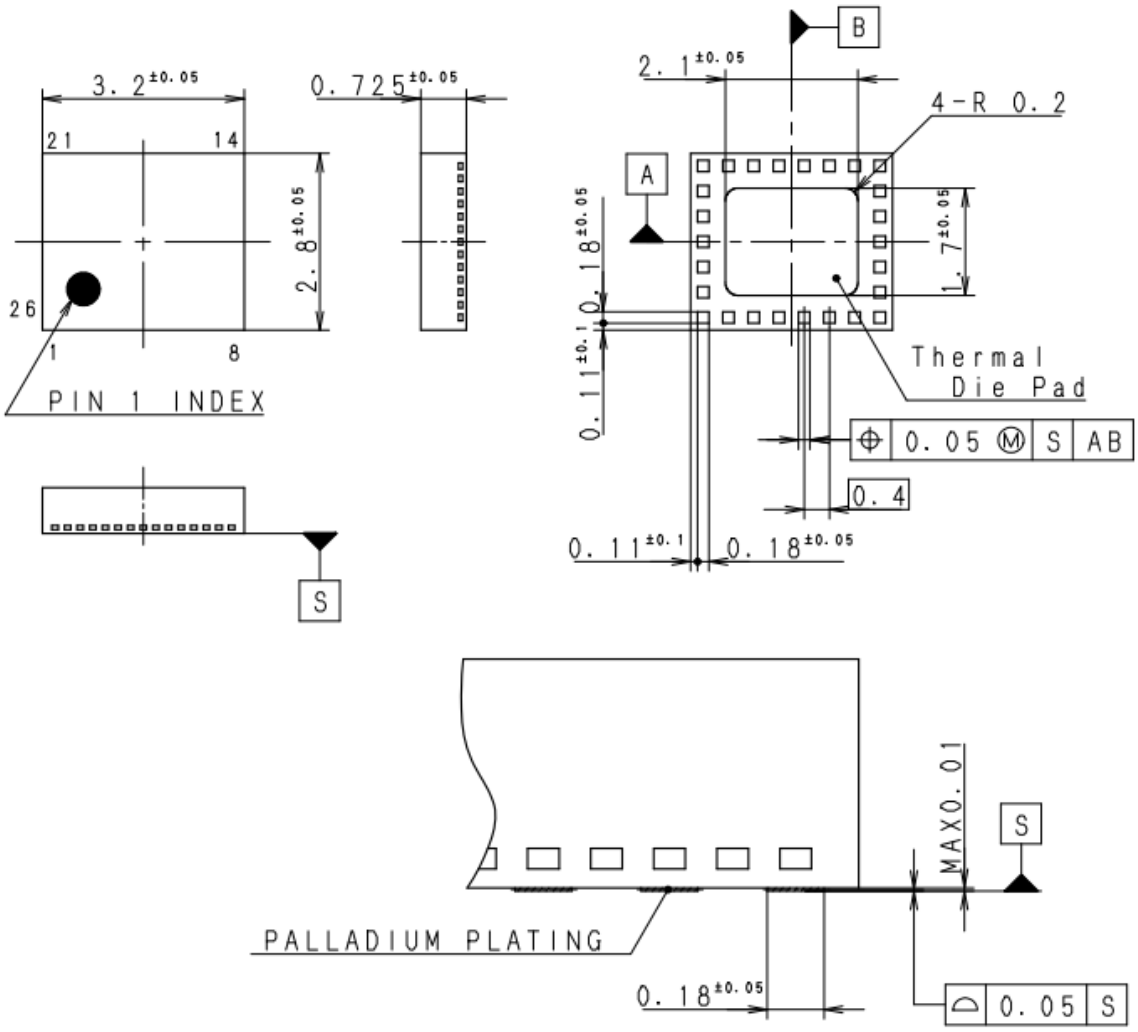


PCB GND Design for VQFN-26P (Image)



Package Outline

(Unit: mm)



TERMINAL SECTION

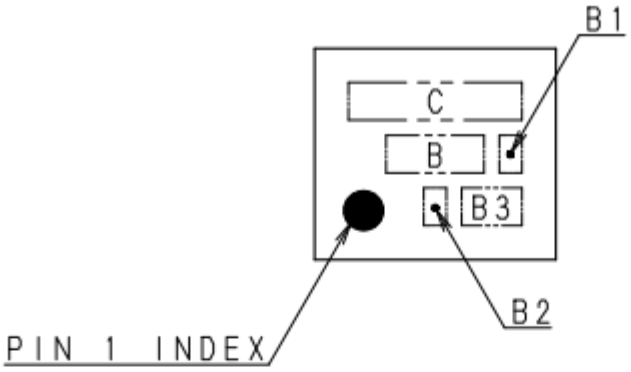
SONY CODE	VQFN-26P-02
JEITA CODE	————
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
TERMINAL TREATMENT	PALLADIUM PLATING
TERMINAL MATERIAL	COPPER ALLOY
PACKAGE MASS	0.020g

PART No. AP-4000-26013S	Rev. 0
ISSUED '13.01.08	REVISED
PRODUCTION LINE	COMPILING DIV. SONY SEMICONDUCTOR
REMARKS PKG CODE:ER-26-A1	

Marking



MARKING C: **M3617**

注1） B部はロット番号（Ｍａｘ３文字で通し記号）を配置する。
Ｂ１部は生産場所コードを配置する。
Ｂ２部は年コードを配置する。
Ｂ３部は週コード（Ｍａｘ２文字）を配置する。
（規定文字数未満につき省略は省略規定に従う。）
注2） C部は製品名（Ｍａｘ５文字）を配置する。
（５文字を超える場合は製品名省略標示規定に従う。）

< INSTRUCTIONS >
1) LOT NO. (MAX 3 CHARACTERS : SERIAL CODE) IN SECTION B.
PLANT CODE IN SECTION B1
A YEAR CODE IN SECTION B2.
A WEEK CODE (MAX 2 CHARACTERS) IN SECTION B3.
(FOLLOW RULES FOR ABBREVIATIONS.)
2) TYPE NO. (MAX 5 CHARACTERS) IN SECTION C.
(FOR MORE THAN 5 CHARACTERS FOLLOW RULES FOR ABBREVIATIONS.)

Tape and Reel Size

12mm WIDTH EMBOSSED TAPING

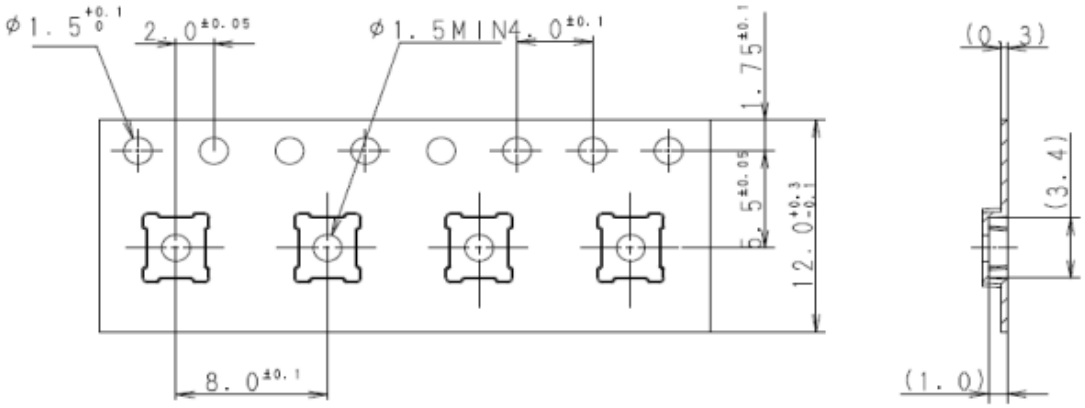
PACKAGE CODE	EMBOSSED TAPING CODE
VQFN-26P-02	R026QNR3-12-N-1

1. SCOPE

THIS SPECIFICATION DESCRIBES THE EMBOSSED TAPING FOR SMD(SURFACE MOUNTED DEVICE) IC'S. FOR SHIPMENT. THIS SPECIFICATION IS BASED ON THE STIPULATIONS OF JAPAN ELECTRONICS AND INFORMATION TECHNOLOGY INDUSTRIES ASSOCIATION(JEITA), JIS C0806-3. AND ELECTRONIC INDUSTRIES ASSOCIATION EIA-481.

2. PRODUCT INDICATION

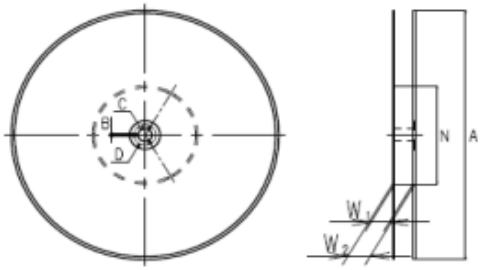
3. TAPING SPECIFICATIONS



NOTE)1. THE R MEASUREMENT WITHOUT INDICATION IS ASSUMED TO BE 0.3mm MAX. GENERAL TOLERANCE: ±0.2
2. THE FEED HOLE CUMULATIVE PITCH ERROR IS ASSUMED AT±0.2mm/10PITCH. UNIT:mm

4. REEL DIMENSIONS

φ330mm PLASTIC REEL



UNIT:mm

SYMBOL	A	N	C	D
DIMENSION	φ330±2	φ100±1	φ13±0.2	φ21±0.8
SYMBOL	B	W_1	W_2	
DIMENSION	2±0.5	13.4±1	17.4±1	

MATERIAL:POLYSTYRENE CONTAINING CARBON(ANTISTATIC)

‡INTRODUCTION OF REUSE REEL
(REEL THAT IS USED AGAIN AFTER COLLECTION)
WE USE THE REUSE REEL OF JEITA SPECIFICATION.

Moisture Sensitivity

Moisture Sensitivity Level for this part is MSL = 2