

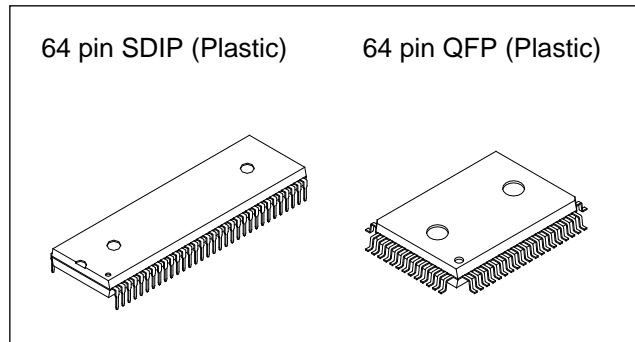
## CMOS 4-bit Single Chip Microcomputer

### Description

The CXP508L4/508L6 is a CMOS 4-bit microcomputer which consists of 4-bit CPU, ROM, RAM, I/O port, 8-bit timer, 8-bit timer/counter, 18-bit time base timer, 8-bit serial I/O, vector interruption, and a liquid crystal displayer (LCD) controller/driver. They are integrated into a single chip with the standby function etc. which are to be operated at low power consumption.

### Features

- Instruction cycle 4 $\mu$ s/2MHz (2.4V to 3.5V)
- ROM capacity 4.096  $\times$  8 bits (CXP508L4)  
6.144  $\times$  8 bits (CXP508L6)
- RAM capacity 400  $\times$  4 bits  
(24  $\times$  4 bits is used in combination with the LCD display memory)
- 32 general purpose I/O ports  
(For 16 segment outputs)
- LCD controller/driver (Direct drive possible)
  - Optical specification of 24, 20 or 16 segment outputs
  - 1/2, 1/3, 1/4 duty selectable through program
  - 1/3 bias
- 2 external interruption input pins
- 8-bit/4-bit variable serial I/O
- 8-bit timer, 8bit timer/event counter and 18-bit time base timer are independently controllable
- Arithmetic and logical operations possible between the entire RAM area, I/O area and the accumulator by means of memory mapped I/O
- Reference to the entire ROM area is possible with the table look-up instruction
- 2 types of power down models, sleep and stop
- 64-pin plastic SDIP/QFP available
- Piggy back package (CXP5080) available

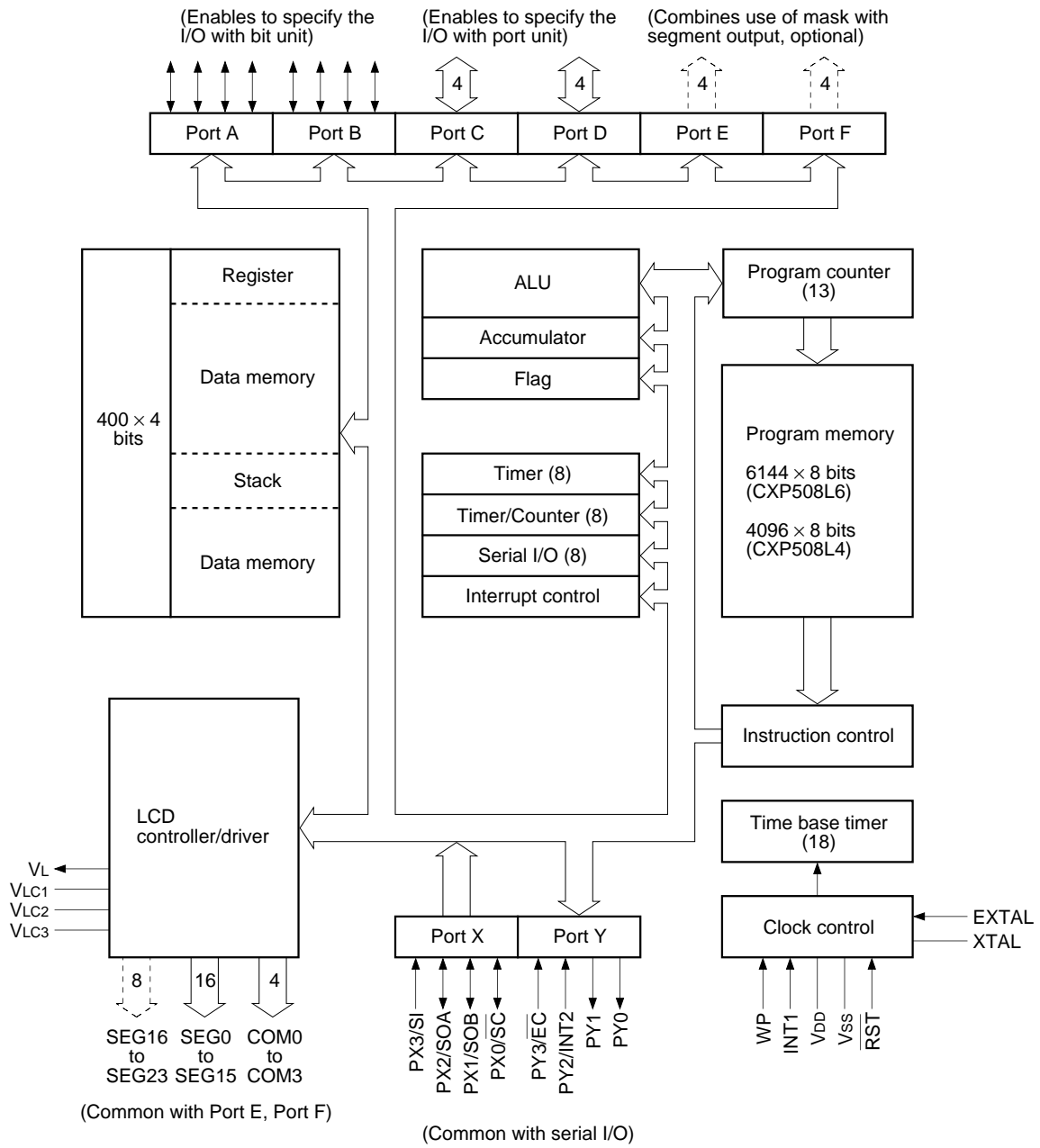


### Structure

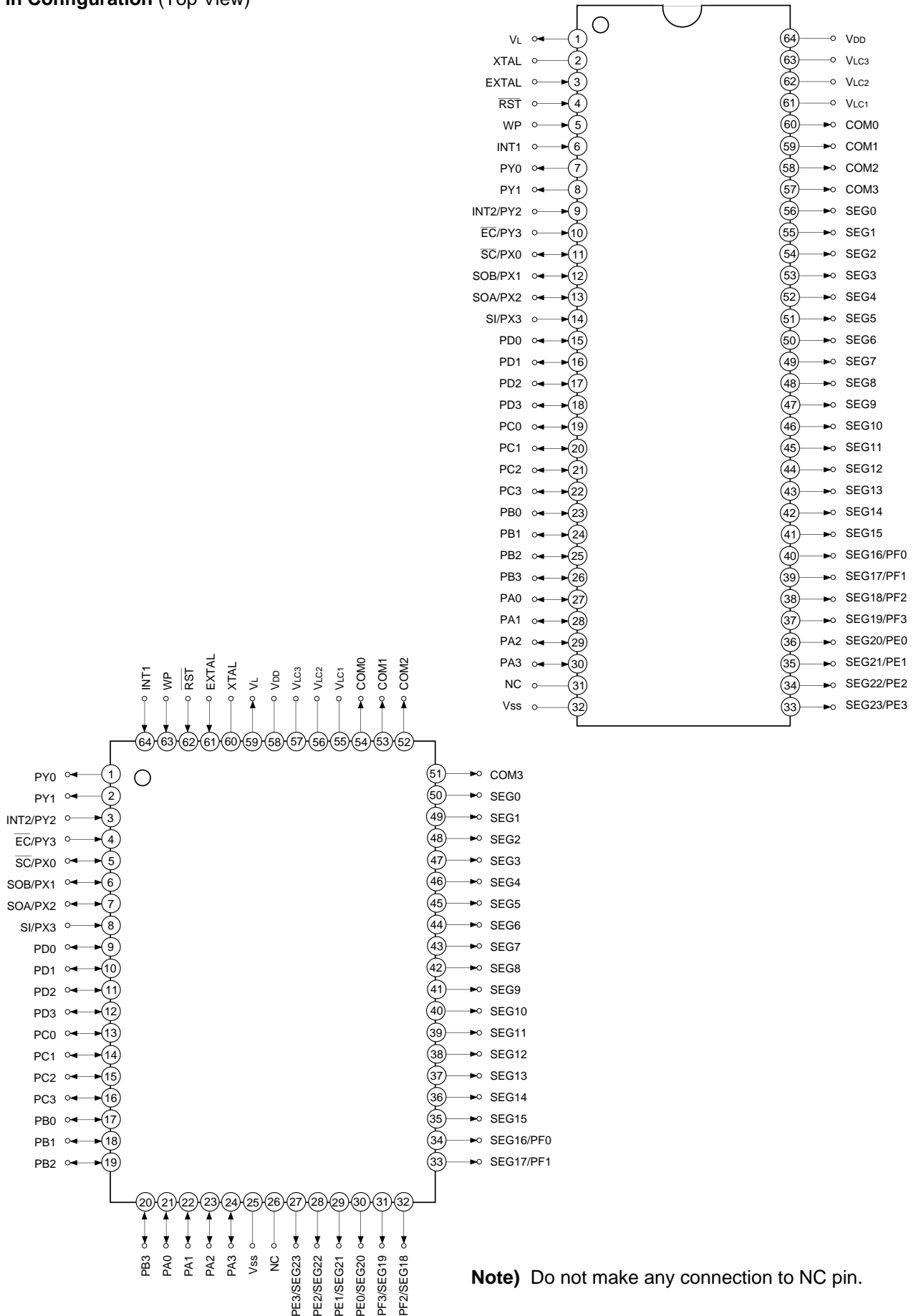
Silicon gate CMOS IC

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Block Diagram



Pin Configuration (Top View)



Note) Do not make any connection to NC pin.

**Absolute Maximum Ratings**

(Ta = -20 to +75°C, Vss = 0V)

Item	Symbol	Ratings	Unit	Remarks
Power supply voltage	VDD	-0.3 to +5.0	V	
LCD bias voltage	VLC1, VLC2, VLC3	-0.3 to +5.0*1	V	
Input voltage	VIN	-0.3 to +5.0*1	V	
Output voltage	VOUT	-0.3 to +5.0*1	V	
High level output current	IOH	-5	mA	General purpose port*2: per pin
High level total output current	∑IOH	-50	mA	Entire pin total
Low level output current	IOL	15	mA	General purpose port*2: per pin
Low level total output current	∑IOL	50	mA	Entire pin total
Operating temperature	Topr	-20 to +75	°C	
Storage temperature	Tstg	-55 to +150	°C	
Allowable power dissipation	PD	1000	mW	SDIP
		600	mW	QFP

\*1 VLC1, VLC2, VLC3, VIN and VOUT should not exceed VDD + 0.3V.

\*2 The PE and PF are specified when PA to PD, PX0 to PX2, PY0, PY1 and mask option are port selected.

**Note)** Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should better take place under the recommended operating conditions. Exceeding those conditions may adversely affect the reliability of the LSI.

**Recommended Operating Conditions**

(Vss = 0V)

Item	Symbol	Min.	Max.	Unit	Remarks
Power supply voltage	VDD	2.4	3.5	V	Guaranteed range during operation
		2.0	3.5	V	Guaranteed data hold operation range during STOP
LCD bias voltage	VLC1, VLC2, VLC3	VSS	VDD	V	Liquid crystal power supply voltage*1
High level input voltage	VIH	0.7VDD	VDD	V	
	VIHS	0.8VDD	VDD	V	Hysteresis input*2
	VIHEX	VDD - 0.4	VDD + 0.3	V	EXTAL pin*3
Low level input voltage	VIL	0	0.3VDD	V	
	VILS	0	0.2VDD	V	Hysteresis input*2
	VILEX	-0.3	0.4	V	EXTAL pin*3
Operating temperature	Topr	-20	+75	°C	

\*1 The optimum value is determined by the characteristics of the liquid crystal display element used.

\*2 They are the respective pins of INT1, WP, PX0, PX3, PY2, PY3 and  $\overline{\text{RST}}$ .

\*3 Specified only during external clock input.

**Electrical Characteristics**

**DC characteristics**

(Ta = -20 to +75°C, Vss = 0V)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
High level output voltage	VOH	PA to PF*1, PX0 to PX2, PY0, PY1, VL (VOL only)	VDD = 2.4V, IOH = -0.3mA*2	1.8			V
			VDD = 2.4V, IOH = -0.5mA*2	1.4			V
			VDD = 2.4V, IOH = -5μA*3	1.8			V
			VDD = 2.4V, IOH = -10μA*3	1.4			V
Low level output voltage	VOL		VDD = 2.4V, IOH = 1.0mA			0.4	V
			VDD = 2.4V, IOH = 2.0mA			0.6	V
Input current	I <sub>IH</sub>	EXTAL*4	VDD = 3.5V, VIH = 3.5V	0.3		20	μA
	I <sub>I<sub>LE</sub></sub>			-0.3		-20	μA
	I <sub>I<sub>LR</sub></sub>	RST*5	VDD = 3.5V, VIL = 0.4V	-1.5		-200	μA
	I <sub>I<sub>L</sub></sub>	PA to PF*6, PX0 to PX2*6, PX3*8, PY0*7, PY1*7, PY2*8, PY3*8, INT1*8, WP*8, RST*5				-1.0	mA
High impedance I/O leakage current	I <sub>I<sub>Z</sub></sub>		VDD = 3.5V VI = 0, 3.5V			±5	μA
Common output impedance	R <sub>COM</sub>	COM0 to COM3	VDD = 3.5V VLC1 = 2.65V		3	5	kΩ
Segment output impedance	R <sub>SEG</sub>	SEG0 to SEG15 SEG16 to SEG23*1	VLC2 = 1.75V VLC3 = 0.88V		5	15	kΩ
Current power supply	I <sub>DD</sub>	VDD	VDD = 3.5V During external clock 1MHz operation Entire output pins open		1.3	4	mA
	I <sub>DDSP</sub>				0.6	1.2	mA
	I <sub>DDS</sub>					7	μA
Input capacitance	C <sub>IN</sub>	VLC1 to VLC3, COM0 to COM3, SEG0 to SEG15, SEG16 to SEG23*1, Other pins than VDD, Vss	Clock 1MHz 0V other than the measured pins		10	20	pF

- \*1 The PE to PF show when the combined pins are selected as the port, and SEG16 to SEG23 show when the combined pins are selected as the segment output.
- \*2 It is when the respective pins of PA to PF and PX0 to PX2 select the 3-state output circuit, and PY0 and PY1 are when the inverter output circuit is selected.
- \*3 It is when the respective pins of PA to PF, PX0 to PX2, PY0 and PY1 select the pull-up resistance.
- \*4 It is when the crystal or ceramic oscillation circuit is selected.
- \*5 The RST pin specifies the input current when the pull-up resistance is selected, and specifies leakage current when non-resistance is selected.
- \*6 The respective pins of PA to PF and PX0 to PX2 specify the input current when the pull-up resistance is selected, and specify the leakage current when in the port state during the 3-state output circuit or standby is selected at high impedance.
- \*7 The respective pins of PY0 and PY1 specify the input current when the pull-up resistance is selected, and specify the leakage current when in the port state during standby is selected at high impedance.
- \*8 The respective pins of PX3, PY2, PY3, INT1 and WP only specify the leakage current.

**AC characteristics**

(1) Clock timing

( $T_a = -20$  to  $+75^\circ\text{C}$ ,  $V_{DD} = 2.4$  to  $3.5\text{V}$ ,  $V_{SS} = 0\text{V}$ )

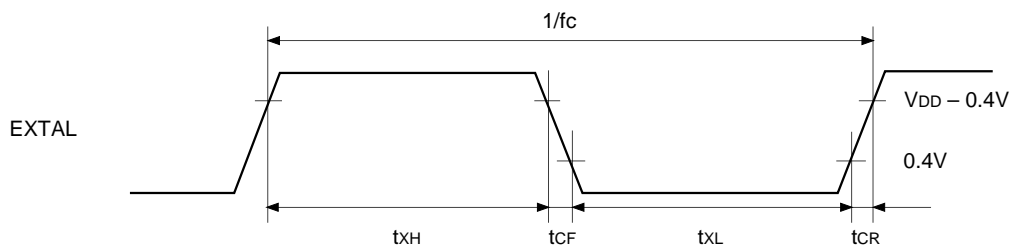
Item	Symbol	Pin	Condition	Min.	Max.	Unit
System clock frequency	$f_c$	XTAL EXTAL	Fig. 1., Fig. 2.	0.5	2	MHz
System clock input pulse width	$t_{XL}$ $t_{XH}$	EXTAL	Fig. 1., Fig. 2.*1 External clock drive	230		ns
System clock input rising and falling times	$t_{CR}$ $t_{CF}$	EXTAL	Fig. 1., Fig. 2.*1 External clock drive		200	ns
Event count clock input pulse width	$t_{EL}$ $t_{EH}$	$\overline{EC}$	Fig. 3.	$t_{sys}^{*2} + 0.05$		$\mu\text{s}$
Event count clock input rising and falling times	$t_{ER}$ $t_{EF}$	$\overline{EC}$	Fig. 3.		20	ms

\*1 The external clock in Fig. 2. specified only when the option is selected for crystal or ceramic oscillation.

\*2  $t_{sys} = 8/f_c$

**Note)** When adjusting the frequency accurately, there may be cases in which they may differ from Fig. 2.

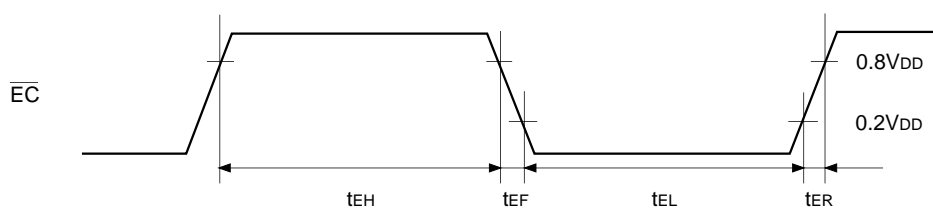
**Fig. 1. Clock timing**



**Fig. 2. Clock applying condition**



**Fig. 3. Event count clock timing**

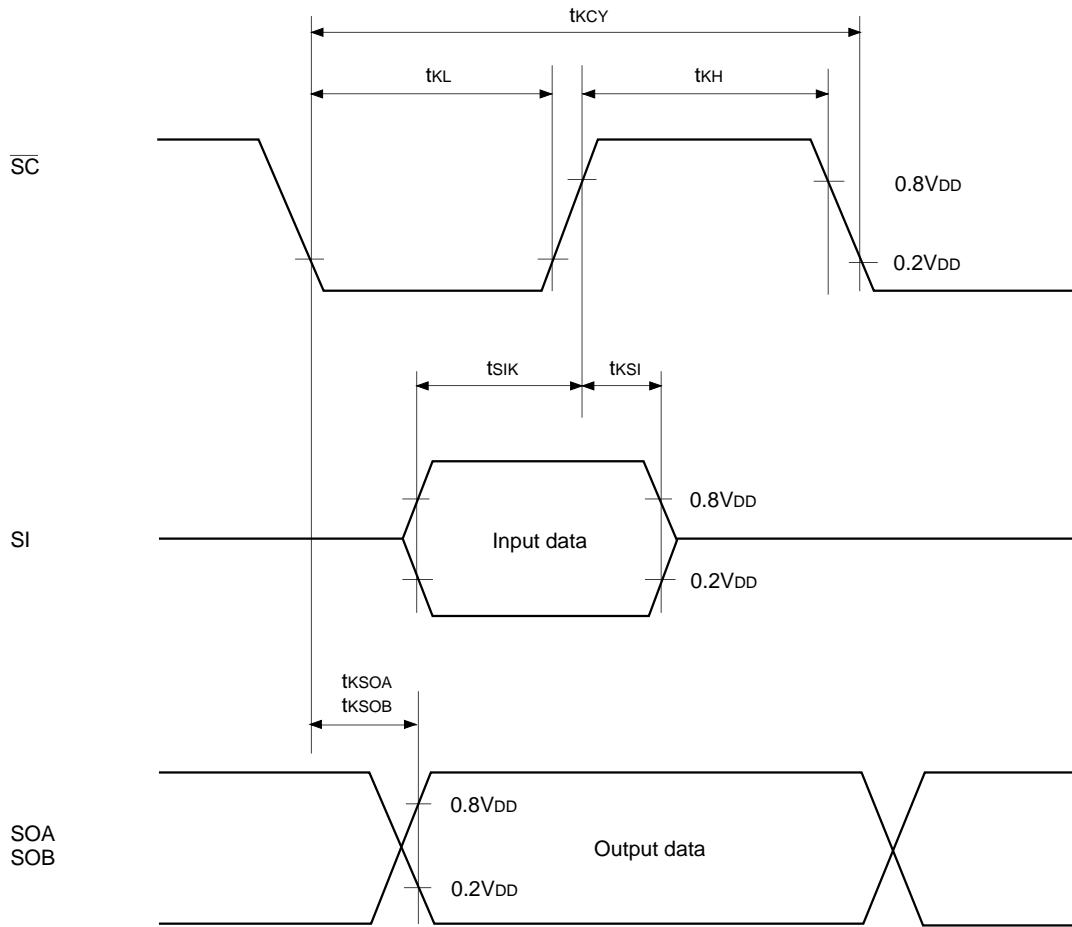


**(2) Serial transfer**(Ta = -20 to +75°C, V<sub>DD</sub> = 2.4 to 3.5V, V<sub>SS</sub> = 0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
Serial transfer clock ( $\overline{SC}$ ) cycle time	t <sub>KCY</sub>	$\overline{SC}$	Input mode	tsys/4 + 1.42		μs
			Output mode	tsys		μs
Serial transfer clock ( $\overline{SC}$ ) high and low level widths	t <sub>KH</sub> t <sub>KL</sub>	$\overline{SC}$	input mode	tsys/8 + 0.7		μs
			Output mode* <sup>1</sup>	tsys/2 - 0.1		μs
			Output mode* <sup>2</sup>	tsys/2 - 1.6		μs
Serial data input setup time (against $\overline{SC}$ ↑)	t <sub>SIK</sub>	SI	$\overline{SC}$ input mode	0.1		μs
			$\overline{SC}$ output mode	0.2		μs
Serial data input hold time (against $\overline{SC}$ ↑)	t <sub>KSI</sub>	SI	$\overline{SC}$ input mode	tsys/8 + 0.5		μs
			$\overline{SC}$ output mode	0.1		μs
High data* <sup>3</sup> output delay time from the $\overline{SC}$ falling time	t <sub>KSOA</sub>	SOA			tsys/8 + 0.5	μs
	t <sub>KSOB</sub>	SOB				
High data* <sup>4</sup> output delay time from the $\overline{SC}$ falling time	t <sub>KSOA</sub>	SOA			tsys/8 + 1.6	μs
	t <sub>KSOB</sub>	SOB				
Low data output delay time from the $\overline{SC}$ falling time	t <sub>KSOA</sub>	SOA			tsys/8 + 0.5	μs
	t <sub>KSOB</sub>	SOB				

**Note 1)** t<sub>sys</sub> = 8/f<sub>c</sub>**Note 2)** The load of data output delay time is 50pF + 1TTL.\*<sup>1</sup> It is specified when  $\overline{SC}$  pin is selected to the 3-atate output by the mask option.\*<sup>2</sup> It is specified when  $\overline{SC}$  pin is selected to the pull-up resistance by the mask option. As the t<sub>sys</sub> receives restriction by this item, take notice that it limits the upper limit of the system clock frequency f<sub>c</sub>.\*<sup>3</sup> It is specified when SOA and PX1/SOB pins are selected to the 3-state output by the mask option.\*<sup>4</sup> It is specified when SOA and PX1/SOB pins are selected to the pull-up resistance by the mask option.

Fig. 4. Serial transfer timing



(3) Others

( $T_a = -20$  to  $+75^\circ\text{C}$ ,  $V_{DD} = 2.4$  to  $3.5\text{V}$ ,  $V_{SS} = 0\text{V}$ )

Item	Symbol	Pin	Condition	Min.	Max.	Unit
External interruption high and low level widths	$t_{1H}$ , $t_{1L}$	INT1	During edge detection mode	$t_{sys} + 0.05$		$\mu\text{s}$
	$t_{2H}$ , $t_{2L}$	INT2		$t_{sys} + 0.05$		$\mu\text{s}$
Reset input low level width	$t_{RSL}$	$\overline{RST}$		$2t_{sys}$		$\mu\text{s}$
Wake-up input high level width	$t_{WPH}$	WP	STOP mode	500		ns
			SLEEP mode	$t_{sys} + 0.05$		$\mu\text{s}$

Note)  $t_{sys} = 8/f_c$



Fig. 5. Interruption input timing

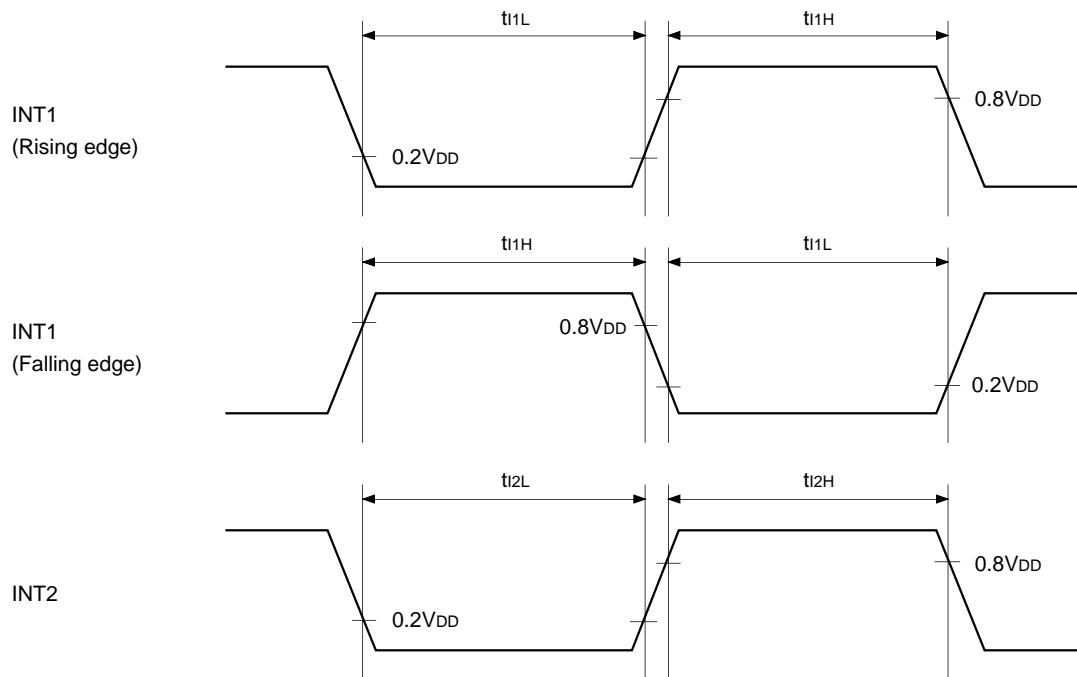


Fig. 6. Reset input timing

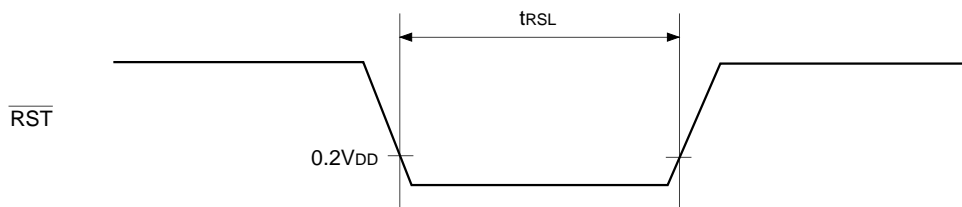
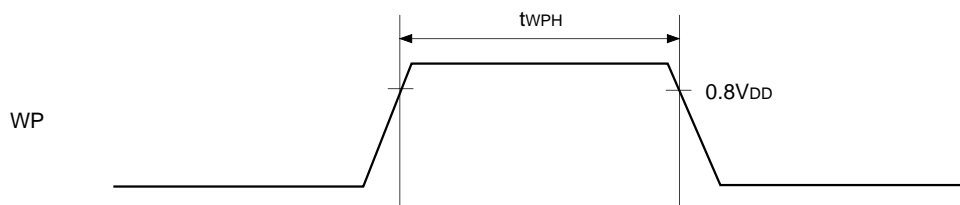


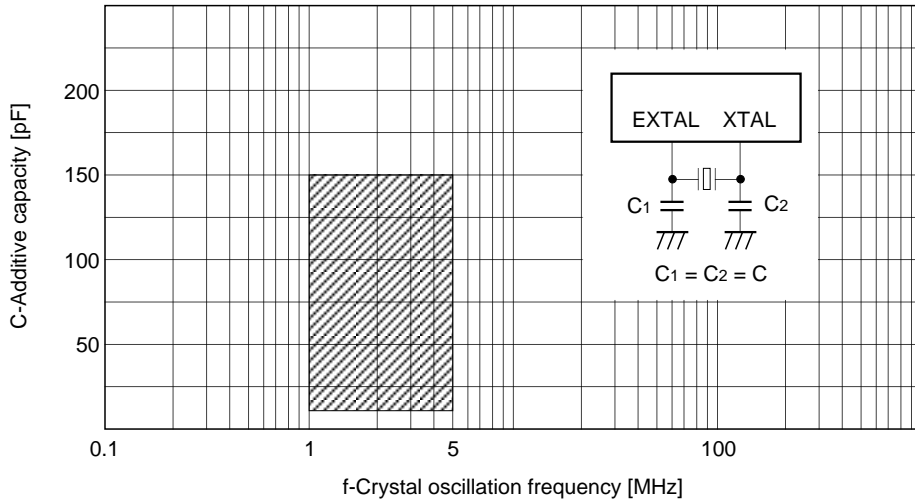
Fig. 7. Wake-up input timing



**Notes on Operation**

See Fig. 8., Additive capacity calculation chart, when using the crystal oscillator and select the appropriate capacity.

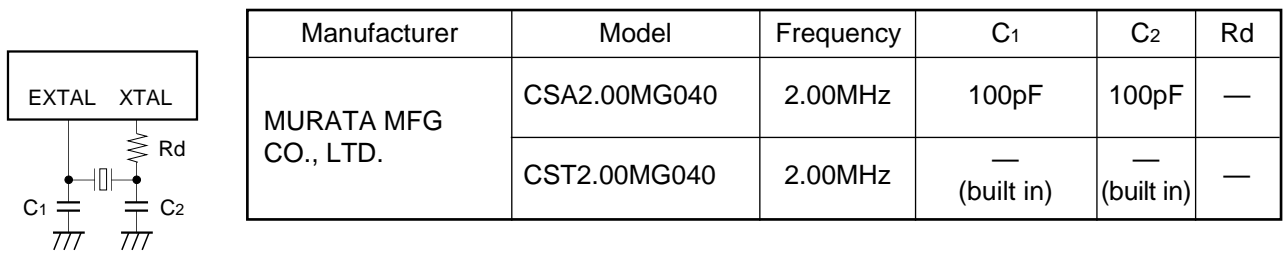
**Fig. 8. Crystal oscillation circuit additive capacity calculation chart** ( $T_a = -20$  to  $+75^\circ\text{C}$ ,  $V_{DD} = 2.4$  to  $3.5\text{V}$ )



**Note)** The above chart shows a range in which the average quartz resonator has a relatively fast oscillation rising edge and stable characteristics. The capacity should be selected to correspond to the appropriate constant for each quartz resonator, should the frequency of the quartz resonator be accurately adjusted.

Fig. 9. Shows recommended circuit and oscillators. Use the trimmer capacitor to  $C_1$ , in the case of accurate adjustment of the oscillation frequency.

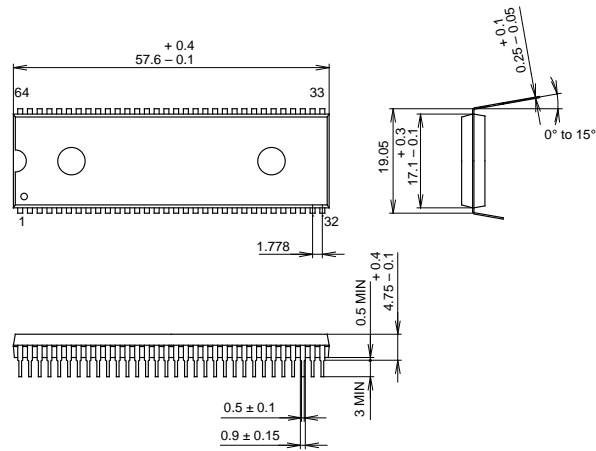
**Fig. 9. Recommended oscillation circuit**



Package Outline

Unit: mm

64PIN SDIP (PLASTIC) 750mil

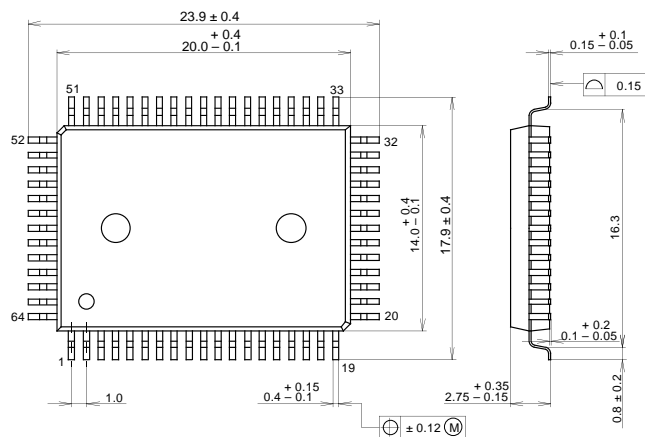


PACKAGE STRUCTURE

SONY CODE	SDIP-64P-01
EIAJ CODE	SDIP064-P-0750-A
JEDEC CODE	_____

MOLDING COMPOUND	EPOXY / PHENOL RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	8.8g

64PIN QFP(PLASTIC)



PACKAGE STRUCTURE

SONY CODE	QFP-64P-L01
EIAJ CODE	*QFP064-P-1420
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	COPPER /42 ALLOY
PACKAGE WEIGHT	1.5g