SONY®

CXP80720/80724

CMOS 8-bit Single Chip Microcomputer

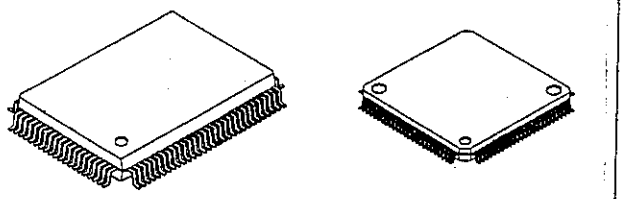
For the availability of this product, please contact the sales office

Description

The CXP80720/80724 is a CMOS 8-bit microcomputer which consists of A/D converter, serial interface, timer/counter, time base timer, vector interruption, high precision timing pattern generation circuit, PWM generator, PWM for tuner, VISS/VASS circuit, 32kHz timer/event counter, remote control receiving circuit, VCR vertical sync separation circuit and the measuring circuit which measure signals of capstan FG and drum FG/PG and other servo systems, as well as basic configurations like 8-bit CPU, ROM, RAM and I/O port. They are integrated into a single chip.

Also CXP80720/80724 provides sleep/stop function which enables to lower power consumption and ultra low speed instruction mode in 32kHz operation.

100 pin QFP (Plastic) 100 pin LQFP (Plastic)



Features

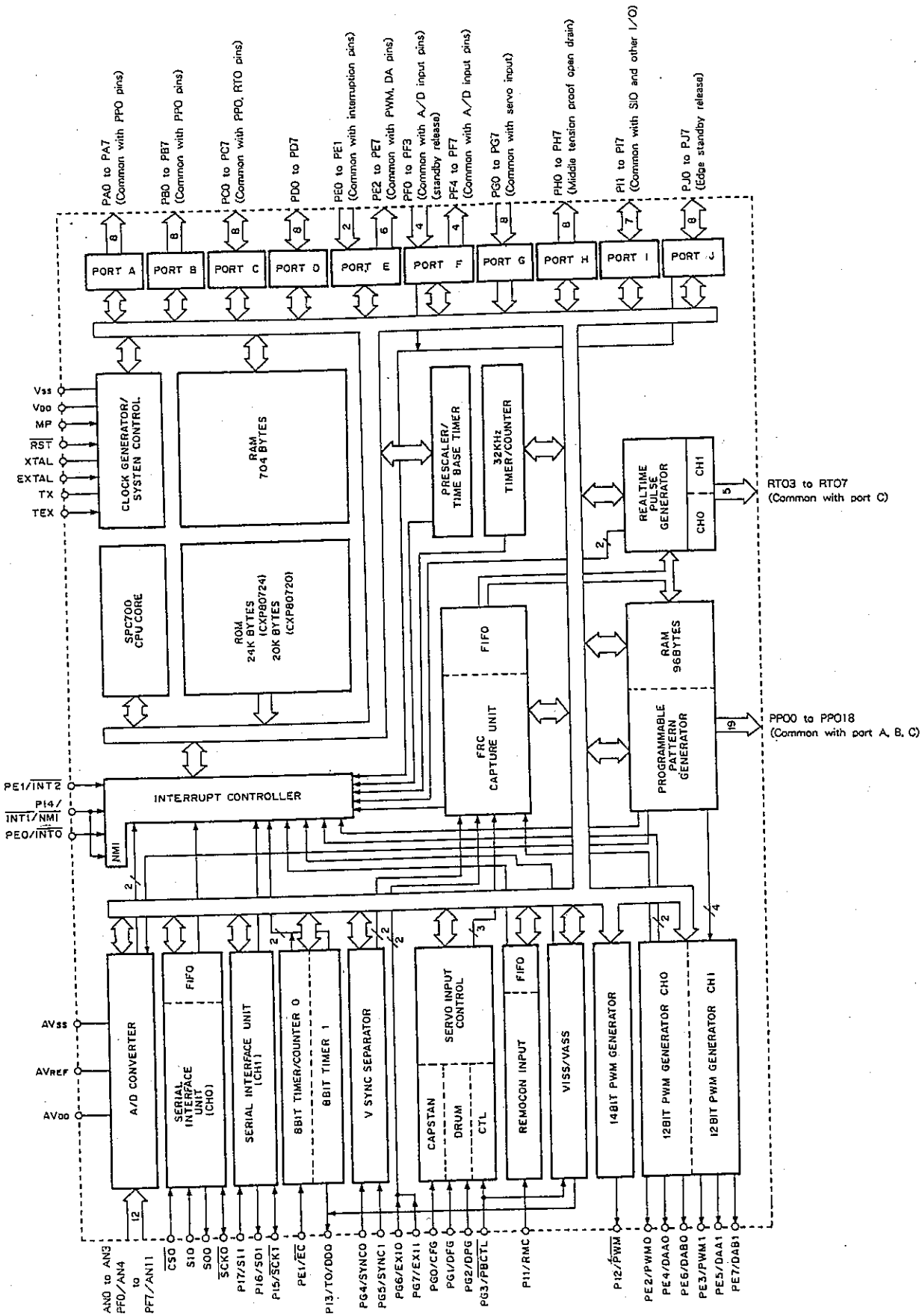
- A wide instruction set (213 instructions) which cover various types of data.
  - — 16-bit arithmetic instruction/multiplication and division instructions/boolean bit operation instruction
- Minimum instruction cycle — During operation 333ns/12MHz, During operation 122 µs/32kHz
- Incorporated ROM capacity — 20K/24Kbytes
- Incorporated RAM capacity — 800bytes
- Peripheral function
  - — A/D converter — 8-bit, 12-channel, successive approximation system (Conversion time: 26.7 µs/12MHz)
  - — Serial I/O with auto transfer mode — Incorporated 8-bit and 8-stage FIFO for data (1 to 8 bytes auto transfer)
  - — Serial I/O — 8-bit serial I/O
  - — Timer — 8-bit timer, 8-bit timer/counter, 19-bit time base timer
  - — High precision timing pattern generator — PPG 19 pins 32-stage programmable RTG 5 pins 2-channel
  - — PWM/DA gate output — 12-bit, 2-channel (Repetitive frequency 46kHz/12MHz)
  - — Servo input control — Capstan FG, Drum FG/PG, CTL input
  - — VSYNC separator
  - — FRC capture unit — Incorporated 26-bit and 8-stage FIFO
  - — PWM output for tuner — 14-bit
  - — VISS/VASS circuit — Pulse duty auto defection circuit
  - — 32kHz timer/event counter — 32kHz oscillation circuit, ultra low speed instruction mode
  - — Remote control receiving circuit — 8-bit pulse measuring counter, 6-stage FIFO
- Interruption — 21 factors, 15 vectors, multi-interruption possible
- Standby mode — SLEEP/STOP
- Package — 100-pin plastic QFP/LQFP
- Piggyback/evaluation chip — CXP80700

Structure

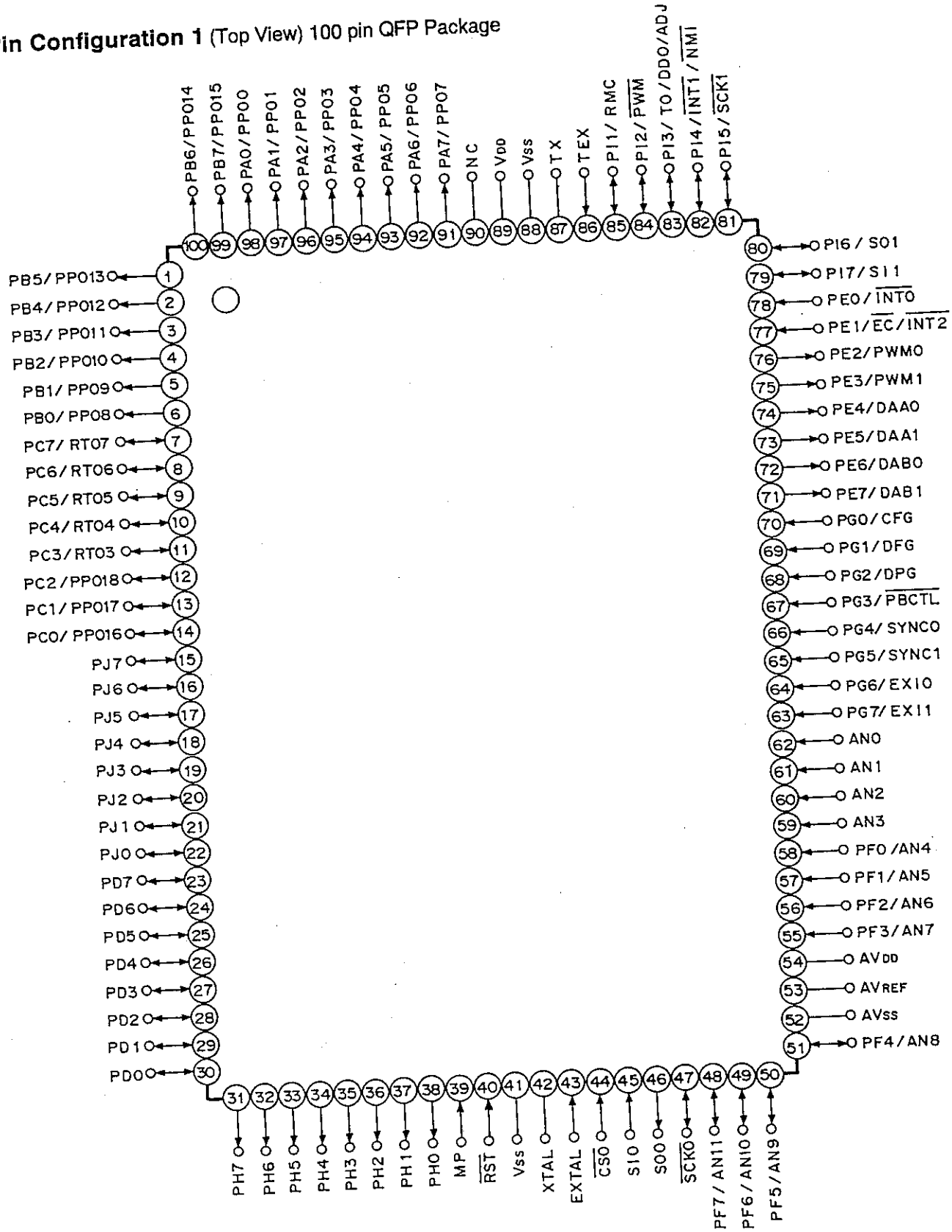
Silicon gate CMOS IC

E90539C1Y

Block Diagram

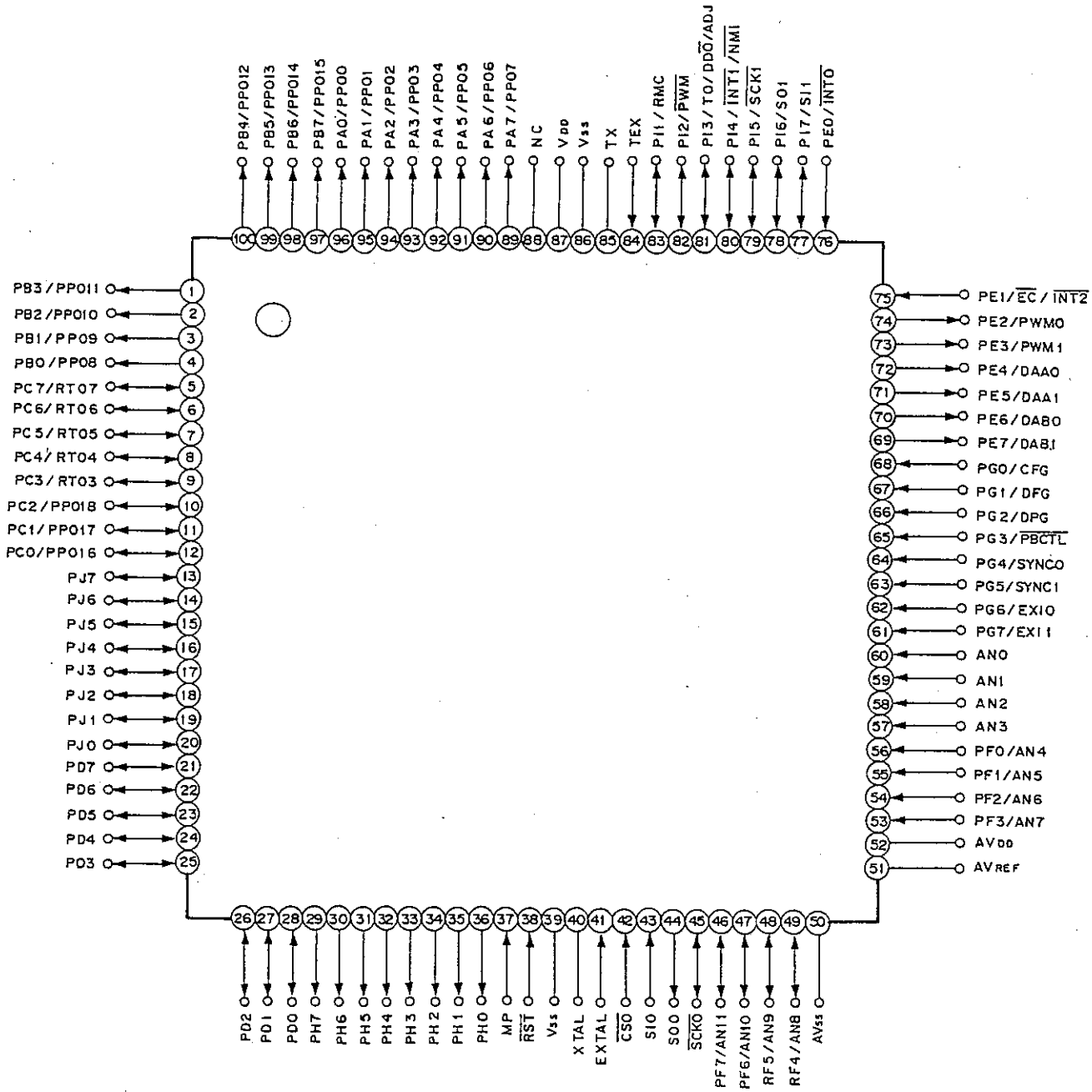


Pin Configuration 1 (Top View) 100 pin QFP Package



Note 1) NC (Pin 90) is always connected to V_{DD}.
2) Vss (Pins 41 and 88) are both connected to GND.

Pin Configuration 2 (Top View) 100 pin LQFP Package



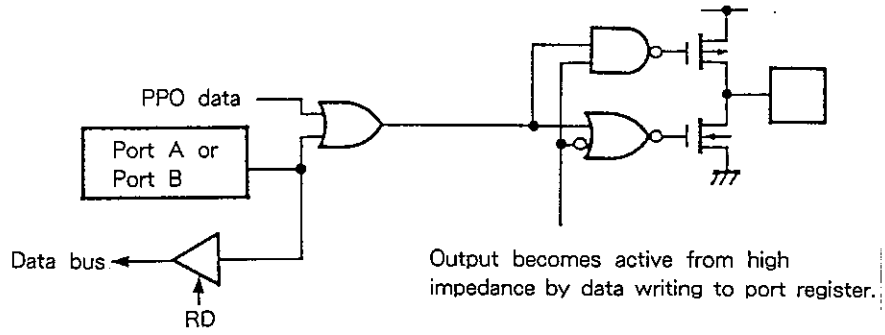
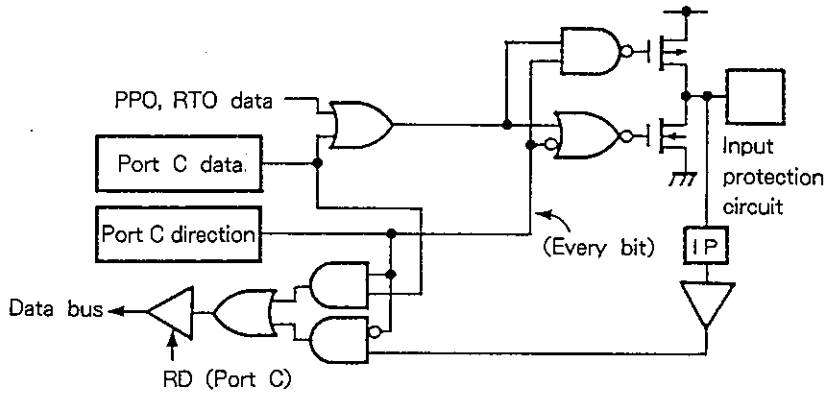
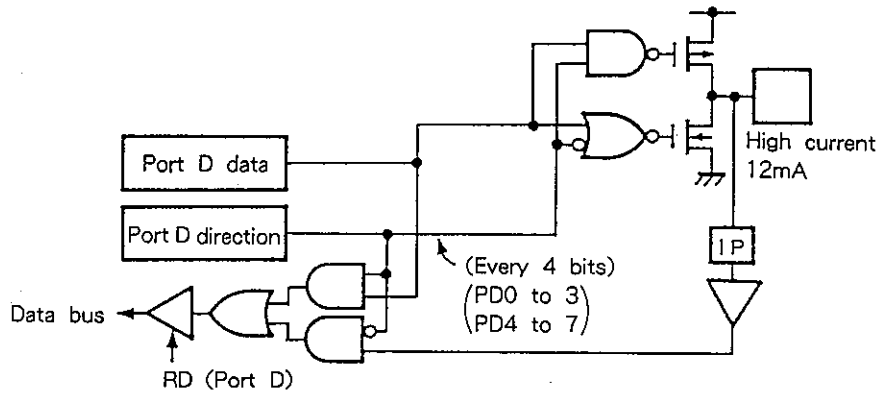
Note 1) NC (Pin 88) is always connected to V_{DD}.
2) Vss (Pins 39 and 86) are both connected to GND.

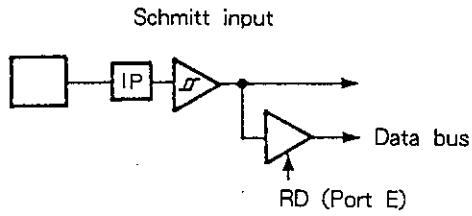
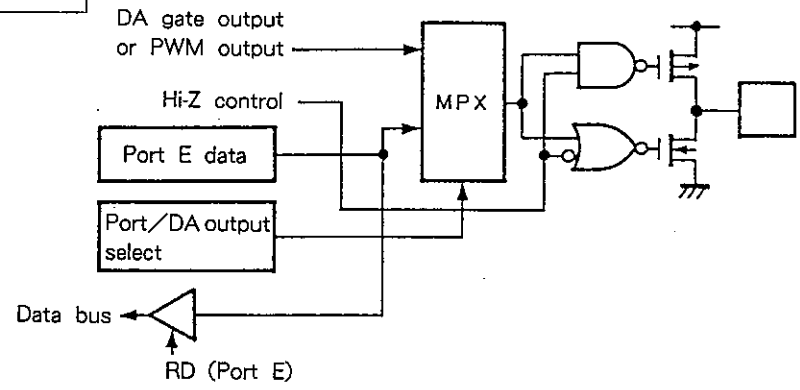
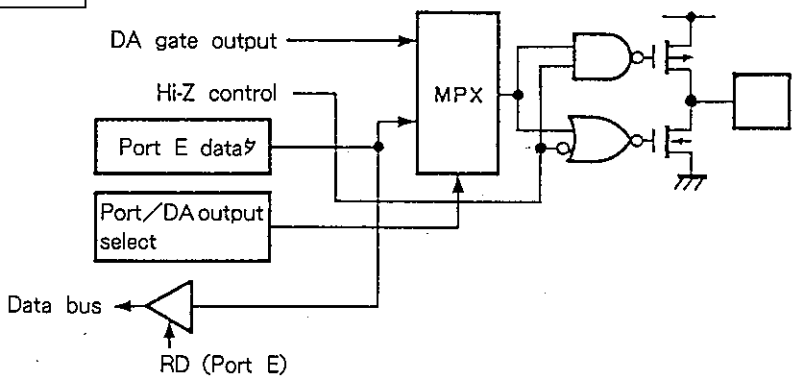
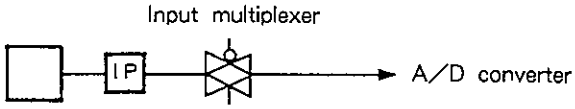
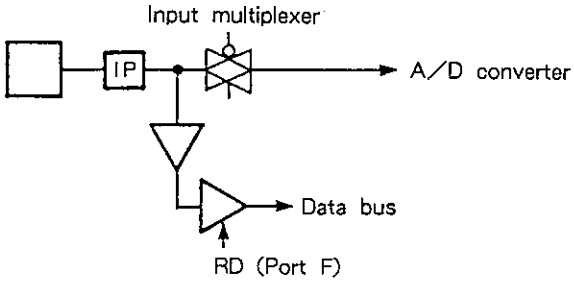
Pin Description

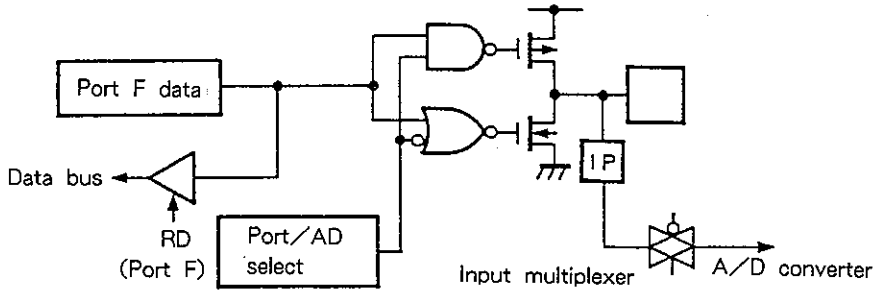
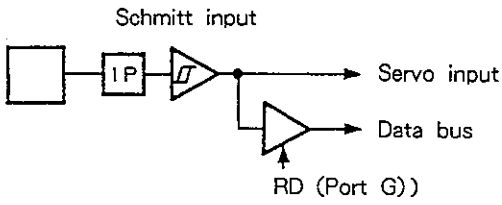
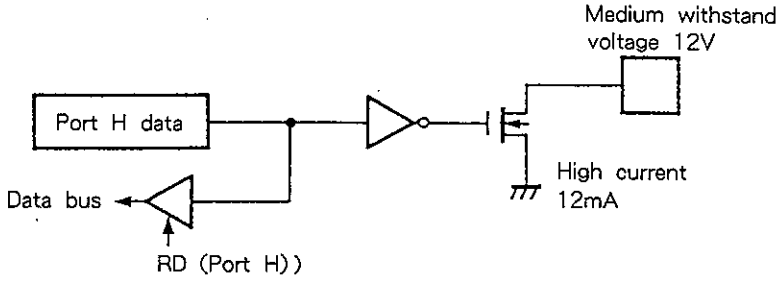
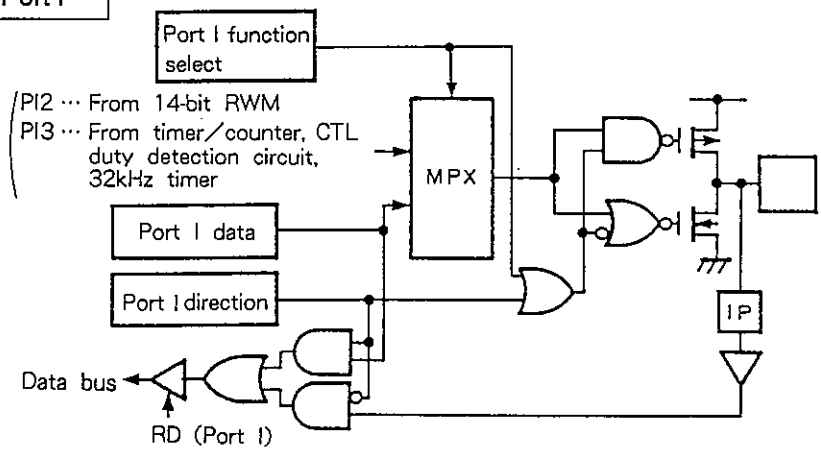
Symbol	I/O	Description	
PA0/PPO0 to PA7/PPO7	Output/ Real time Output	(Port A) 8-bit output port. Data is gated with PPO contents by OR-gate and they are output. (8 pins)	Programmable pattern generator (PPG) output. Functions as high precision real time pulse output port. (19 pins)
PB0/PPO8 to PB7/PPO15	Output/ Real time Output	(Port B) 8-bit output port. Data is gated with PPO contents by OR-gate and they are output. (8 pins)	
PC0/PPO16 to PC2/PPO18	I/O/ Real time Output	(Port C) 8-bit input/output port, enables to specify input/output by bit unit. Data is gated with PPO or RTO contents by OR-gate and they are output. (8 pins)	
PC3/RTO3 to PC7/RTO7	I/O/ Real time Output		Real time pulse generator (RTG) output. Functions as high precision real time pulse output port. (5 pins)
PD0 to PD7	I/O	(Port D) 8-bit input/output port. Enable to specify input/output by 4-bit unit. Enables to drive 12mA sink current. (8 pins)	
PE0/$\overline{INT0}$	Input	(Port E) 8-bit port. Lower 2 bits are input pins and upper 6 bits are output pins. (8 pins)	Input pin to request external interruption. Active when falling edge.
PE1/$\overline{EC}$/$\overline{INT2}$	Input		External event input pin for timer/counter. / Input pin to request external interruption. Active when falling edge.
PE2/PWM0	Output		PWM output pins. (2 pins)
PE3/PWM1	Output		
PE4/DAA0	Output		DA gate pulse output pins. (4 pins)
PE5/DAA1	Output		
PE6/DAB0	Output		
PE7/DAB1	Output		
AN0 to AN3	Input	Analog input pins to A/D converter. (12 pins)	
PF0/AN4 to PF3/AN7	Input	(Port F) Lower 4 bits are input port and upper 4 bits are output port. Lower 4 bits also serve as standby release input pin. (8 pins)	
PF4/AN8 to PF7/AN11	Output/Input		
$\overline{SCK0}$	I/O	Serial clock (CH0) input/output pin.	
SO0	Output	Serial data (CH0) output pin.	

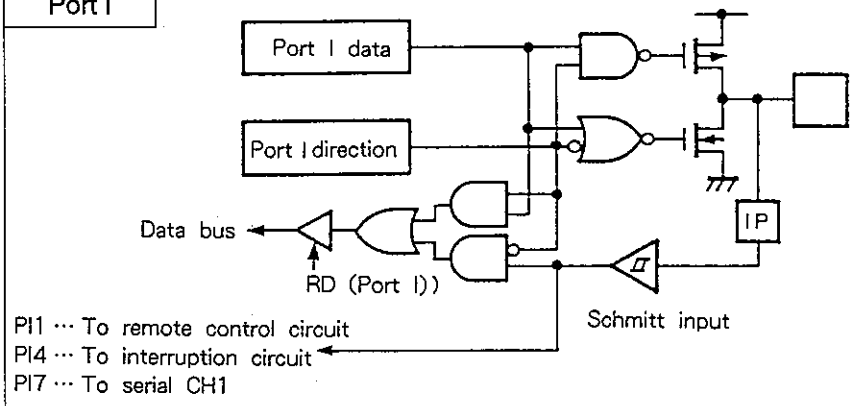
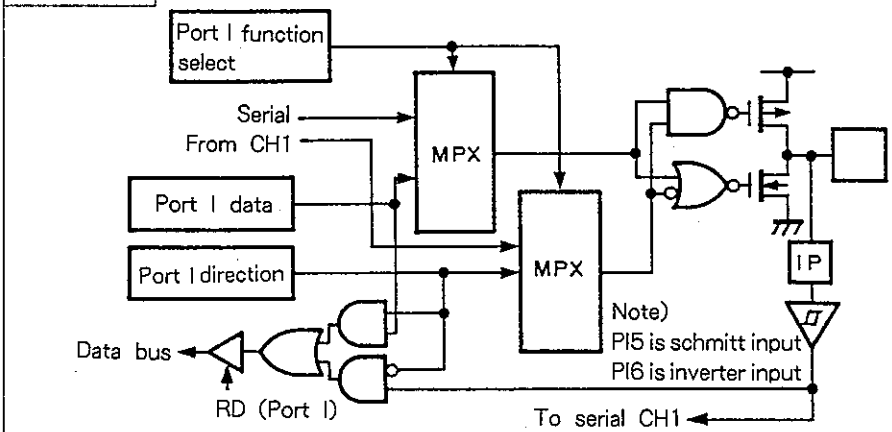
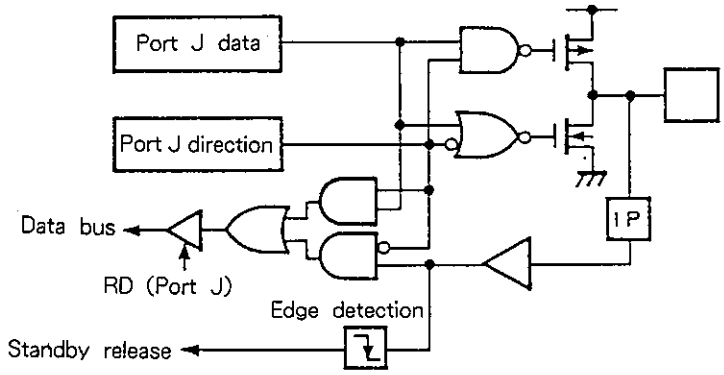
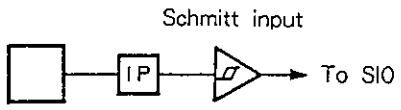
Symbol	I/O	Description	
SI0	Input	Serial data (CH0) input pin.	
$\overline{CS0}$	Input	Serial chip select (CH0) input pin.	
PG0/CFG	Input	(Port G) 8-bit input port. (8 pins)	Capstan FG input pin.
PG1/DFG	Input		Drum FG input pin.
PG2/DPG	Input		Drum PG input pin.
PG3/$\overline{PBCTL}$	Input		Playback CTL pulse input pin.
PG4/SYNC0	Input		Composite sync signal input pin.
PG5/SYNC1	Input		
PG6/EXI0	Input		External input pin to FRC capture unit.
PG7/EXI1	Input		
PH0 to PH7	Output	(Port H) 8-bit output port ; Medium withstand voltage (12V) and high current (12mA), N-ch open drain output. (8 pins)	
PI1/RMC	I/O / Input	(Port I) 7-bit input/output port. Input/output port can be specified by bit unit (7 pins).	Remote control receiving circuit input pin.
PI2/$\overline{PWM}$	I/O / Output		14-bit PWM output pin.
PI3/TO/ DDO/ADJ	I/O / Output		Timer/counter, CTL duty detection, 32kHz oscillation adjustment output pin.
PI4/$\overline{INT1}$/$\overline{NMI}$	I/O / Input		Input pin to request external interruption and non maskable interruption. Active when falling edge.
PI5/$\overline{SCK1}$	I/O / I/O		Serial clock (CH1) input/output pin.
PI6/SO1	I/O / Output		Serial data (CH1) output pin.
PI7/SI1	I/O / Input		Serial data (CH1) input pin.
PJ0 to PJ7	I/O	(Port J) 8-bit input /output port. Function as standby release input can be specified by bit unit. Input/output can be specified by bit unit.	
EXTAL	Input	Connecting pin of crystal oscillator for system clock. When supplying the external clock, input the external clock to EXTAL pin and input opposite phase clock to XTAL pin.	
XTAL	Output		
TEX	Input	Connecting pin of crystal oscillator for 32kHz timer clock. When used as event counter, input to TEX pin and leave TX pin open. (Feedback resistor is not removed)	
TX	Output		
$\overline{RST}$	Input	System reset pin of active "L" level.	
MP	Input	Microprocessor mode input pin. Always connect to GND.	
AV_{DD}		Positive power supply pin of A/D converter.	
AV_{REF}	Input	Reference voltage input pin of A/D converter.	
AV_{SS}		GND pin of A/D converter.	
V_{DD}		Positive power supply pin.	
V_{SS}		GND pin. Connect both Vss pins to GND.	

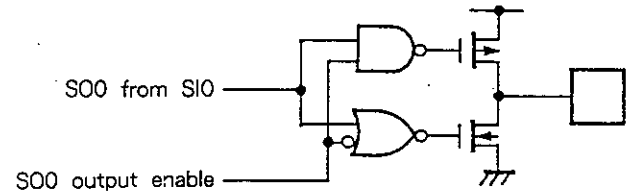
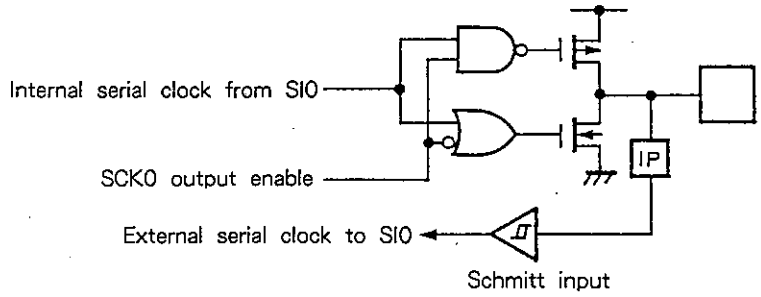
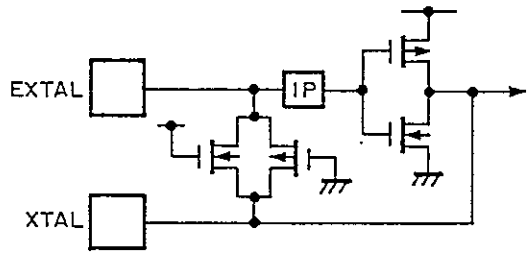
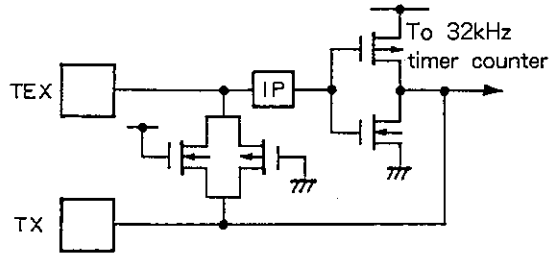
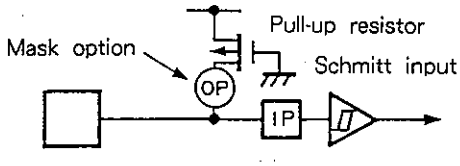
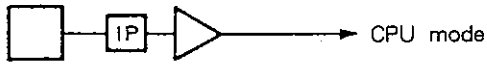
Input/Output Circuit Formats for Pins

Pin	Circuit format	When reset
PA0/PPO0 to PA7/PPO7 PB0/PPO8 to PB7/PPO15 16 pins	Port A Port B 	Hi-Z
PC0/PPO16 to PC2/PPO18 PC3/RTO3 to PC7/RTO7 8 pins	Port C 	Hi-Z
PD0 to PD7 8 pins	Port D 	Hi-Z

Pin	Circuit format	When reset
PE0/$\overline{INT0}$ PE1/$\overline{EC}$/$\overline{INT2}$ 2 pins	Port E 	Hi-Z
PE2/PWM0 PE3/PWM1 PE4/DAA0 PE5/DAA1 4 pins	Port E 	Hi-Z
PE6/DAB0 PE7/DAB1 2 pins	Port E 	H level
AN0 to AN3 4 pins		Hi-Z
PF0/AN4 to PF3/AN7 4 pins	Port F 	Hi-Z

Pin	Circuit format	When reset
PF4/AN8 to PF7/AN11 4 pins	Port F 	Hi-Z
PG0/CFG PG1/DFG PG2/DPG PG3/$\overline{\text{PBCTL}}$ PG4/SYNC0 PG5/SYNC1 PG6/EXI0 PG7/EXI1 8 pins	Port G  Note) For PG4/SYNC0, PG5/SYNC1, CMOS schmitt input and TTL schmitt input can be selected with the mask option.	Hi-Z
PH0 to PH7 8 pins	Port H 	Hi-Z
PI2/$\overline{\text{PWM}}$ PI3/TO/ DD0/ADJ 2 pins	Port I 	Hi-Z

Pin	Circuit format	When reset
PI1/RMC PI4/$\overline{INT1}$/$\overline{NMI}$ PI7/SI1 3 pins	Port I 	Hi-Z
PI5/$\overline{SCK1}$ PI6/SO1 2 pins	Port I 	Hi-Z
PJ0 to PJ7 8 pins	Port J 	Hi-Z
$\overline{CS0}$ SO1 2 pins		Hi-Z

Pin	Circuit format	When reset
SO0 1 pin		Hi-Z
$\overline{SCK0}$ 1 pin		Hi-Z
EXTAL XTAL 2 pins	 • Shows the circuit composition during oscillation. • Feedback resistor is removed during stop.	Oscillation
TEX TX 2 pins	 • Shows the circuit composition during oscillation. • Feedback resistor is removed during 32kHz oscillation circuit stop by software. At this time TEX pin outputs "L" level and TX pin outputs "H" level.	Oscillation
$\overline{RST}$ 1 pin		L level
MP 1 pin		Hi-Z

Absolute Maximum Ratings (Vss=0V)

Item	Symbol	Rating	Unit	Remarks
Power supply voltage	V_{DD}	–0.3 to +7.0	V	
	AV_{DD}	AVss to +7.0 *1	V	
	AVss	–0.3 to +0.3	V	
Input voltage	V_{IN}	–0.3 to +7.0 *2	V	
Output voltage	V_{OUT}	–0.3 to +7.0 *2	V	
Medium withstand output voltage	V_{OUTP}	–0.3 to +15.0	V	PH pin
High level output current	I_{OH}	–5	mA	
High level total output current	ΣI_{OH}	–50	mA	Total of output pins
Low level output current	I_{OL}	15	mA	Other than high current output pins: per pin
	I_{OLC}	20	mA	High current port pin *3 : per pin
Low level total output current	ΣI_{OL}	130	mA	Total of output pins
Operating temperature	Topr	–20 to +75	°C	
Storage temperature	Tstg	–55 to +150	°C	
Allowable power dissipation	P_D	600	mW	QFP Package type
		380		VQFP Package type

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should better take place under the recommended operating conditions. Exceeding those conditions may adversely affect the reliability of the LSI.

*1) AV_{DD} and V_{DD} should be set to a same voltage.

*2) V_{IN} and V_{OUT} should not exceed V_{DD}+0.3V.

*3) The high current operation transistors are the N-CH transistors of the PD and PH ports.

Recommended Operating Conditions

(Vss=0V)

Item	Symbol	Min.	Max.	Unit	Remarks
Power supply voltage	V_{DD}	4.5	5.5	V	Guaranteed range during high speed mode (1/2 dividing clock) operation
		3.5	5.5	V	Guaranteed range during low speed mode (1/16 dividing clock) operation
		2.7	5.5	V	Guaranteed operation range by TEX clock
		2.5	5.5	V	Guaranteed data hold operation range during STOP
Analog power supply	AV_{DD}	4.5	5.5	V	*1
High level input voltage	V_{IH}	$0.7V_{DD}$	V_{DD}	V	*2
	V_{IHS}	$0.8V_{DD}$	V_{DD}	V	C-MOS schmitt input *3
	V_{IHTS}	2.2	V_{DD}	V	TTL schmitt input *4
	V_{IHEX}	$V_{DD}-0.4$	$V_{DD}+0.3$	V	EXTAL pin *5
Low level input voltage	V_{IL}	0	$0.3V_{DD}$	V	*2
	V_{ILS}	0	$0.2V_{DD}$	V	C-MOS schmitt input *3
	V_{ILTS}	0	0.8	V	TTL schmitt input *4
	V_{ILEX}	−0.3	0.4	V	EXTAL pin *5
Operating temperature	Topr	−20	+75	°C	

*1) AV_{DD} and V_{DD} should be set to a same voltage.

*2) Normal input port (each pin of PC, PD, PE0 to PE1, PF0 to PF3, PG, PI and PJ), MP pin

*3) Each pin of $\overline{CS0}$, SI0, $\overline{SCK0}$, $\overline{RST}$, PE0/$\overline{INT0}$, PE1/$\overline{EC}$/$\overline{INT2}$, PG (For PG4 and PG5, when CMOS schmitt input is selected with mask option), PI1/RMC, PI4/$\overline{INT1}$/$\overline{NMI}$, PI5/$\overline{SCK1}$ and PI7/SI1.

*4) Each pin of PG4 and PG5 (When TTL schmitt input is selected with mask option)

*5) It specifies only when the external clock is input.

Electrical Characteristics

DC characteristics

(Ta=–20 to +75°C, Vss=0V)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
High level output voltage	V_{OH}	PA to PD, PE2 to PE7, PF4 to PF7, PH (V_{OL} only), PI1 to PI7, PJ, SO0, $\overline{SCK0}$	V_{DD}=4.5V, I_{OH}=–0.5mA	4.0			V
			V_{DD}=4.5V, I_{OH}=–1.2mA	3.5			V
Low level output voltage	V_{OL}		V_{DD}=4.5V, I_{OL}=1.8mA			0.4	V
			V_{DD}=4.5V, I_{OL}=3.6mA			0.6	V
		PD, PH	V_{DD}=4.5V, I_{OL}=12.0mA			1.5	V
Input current	I_{IHE}	EXTAL	V_{DD}=5.5V, V_{IH}=5.5V	0.5		40	µA
	I_{ILE}		V_{DD}=5.5V, V_{IL}=0.4V	–0.5		–40	µA
	I_{IHT}	TEX	V_{DD}=5.5V, V_{IH}=5.5V	0.1		10	µA
	I_{ILT}		V_{DD}=5.5V, V_{IL}=0.4V	–0.1		–10	µA
	I_{ILR}	$\overline{RST}$ *1	V_{DD}=5.5V, V_{IL}=0.4V	–1.5		–400	µA
I/O leakage current	I_{IZ}	PA to PG, PI, PJ, MP, AN0 to AN3, $\overline{CS0}$, SI0, SO0, $\overline{SCK0}$, $\overline{RST}$ *1	V_{DD}=5.5V V_I=0, 5.5V			± 10	µA
Open drain output leakage current (N-CH Tr OFF in state)	I_{LOH}	PH	V_{DD}=5.5V V_{OH}=12V			50	µA
Supply current *2	I_{DD1}	V_{DD}	12MHz crystal oscillation (C1=C2=15pF) V_{DD}=5V ± 10% *3		22	45	mA
	I_{DDS1}		SLEEP mode V_{DD}=5V ± 10%		1.1	8	mA
	I_{DD2}		32kHz crystal oscillation (C1=C2=47pF) V_{DD}=3V ± 10%		35	100	µA
	I_{DDS2}		SLEEP mode V_{DD}=3V ± 10%		9	30	µA
	I_{DDS3}		STOP mode (12MHz and 32kHz oscillation stop) V_{DD}=5V ± 10%			10	µA
Input capacity	C_{IN}	Other than V_{DD}, Vss, AV_{DD}, AVss pins	Clock 1MHz 0V other than the measured pins		10	20	pF

*1) $\overline{RST}$ pin specifies the input current when the pull-up resistance is selected, and specifies leakage current when non-resistance is selected.

*2) When entire output pins are open.

*3) When setting upper 2 bits (CPU clock selection) of clock control register CLC (address: 00FEH) to "00" and operating in high speed mode (1/2 dividing clock).

AC Characteristics

(1) Clock timing

(Ta=–20 to +75°C, V_{DD}=4.5 to 5.5V, Vss=0V)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
System clock frequency	fc	XTAL EXTAL	Fig. 1, Fig. 2	1		12	MHz
System clock input pulse width	t_{XL} t_{XH}	EXTAL	Fig. 1, Fig. 2 (External clock drive)	37.5			ns
System clock input rising and falling times	t_{CR} t_{CF}					200	ns
Event count clock input pulse width	t_{EL} t_{EH}	$\overline{EC}$	Fig. 3	tsys * +50			ns
Event count clock input rising and falling times	t_{ER} t_{EF}	$\overline{EC}$	Fig. 3			20	ms
System clock frequency	fc	TEX TX	V_{DD}=2.7 to 5.5V Fig. 2 (32kHz clock applying condition)		32.768		kHz
Event count clock input pulse width	t_{TL} t_{TH}	TEX	Fig. 3	10			μs
Event count clock input rising and falling times	t_{TR} t_{TF}	TEX	Fig. 3			20	ms

* tsys indicates three values according to the contents of the clock control register (address; 00FE$_H$) upper 2 bits (CPU clock selection).
tsys [ns] =2000/fc (Upper 2-bit="00"), 4000/fc (Upper 2-bit="01"), 16000/fc (Upper 2-bit="11")

Fig. 1 Clock timing

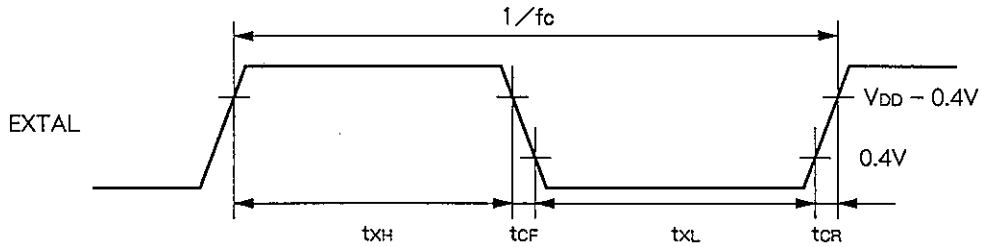


Fig. 2 Clock applying condition

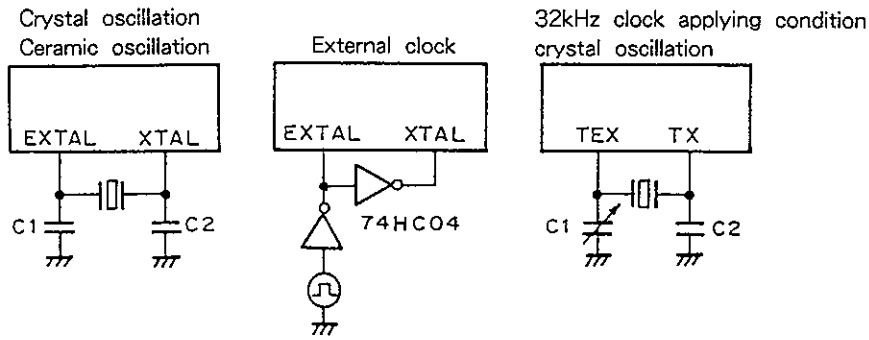
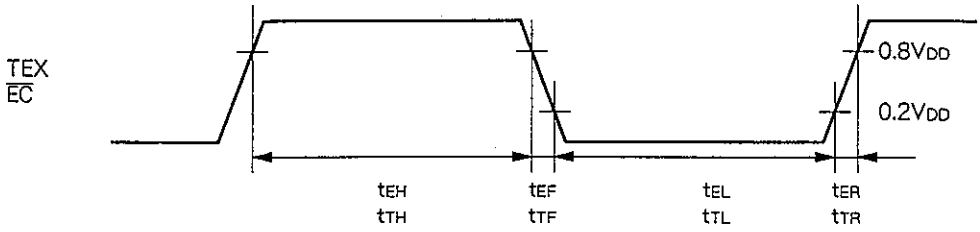


Fig. 3 Event count clock timing



(2) Serial transfer (CH0)

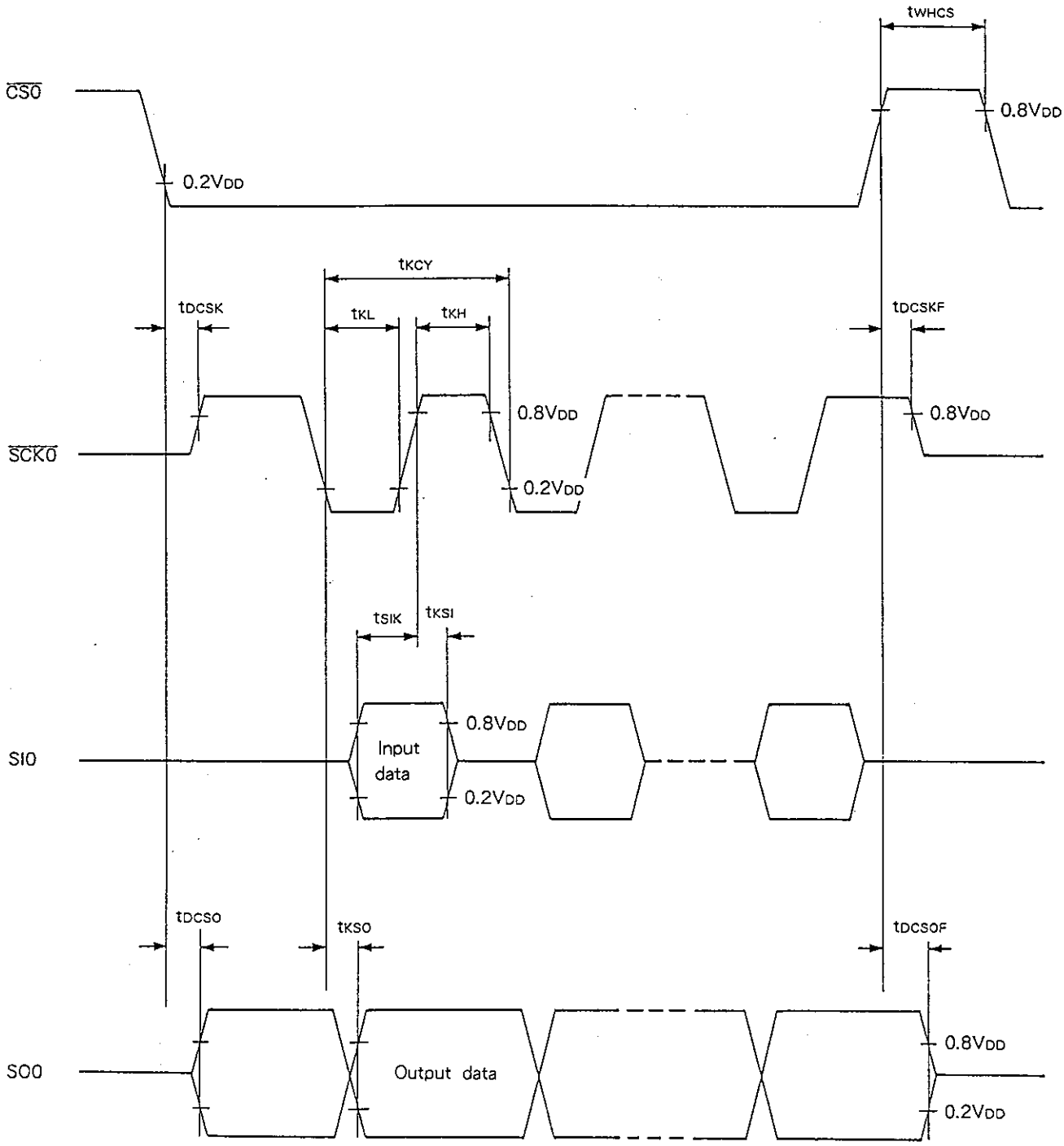
(Ta=–20 to +75°C, VDD=4.5 to 5.5V, Vss=0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{CS0}$ ↓ → $\overline{SCK0}$ delay time	tDCSK	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK0}$=output mode)		tsys+200	ns
$\overline{CS0}$ ↑ → $\overline{SCK0}$ floating delay time	tDCSKF	$\overline{SCK0}$			tsys+200	ns
$\overline{CS0}$ ↓ → SO0 delay time	tDCSO	SO0	Chip select transfer mode		tsys+200	ns
$\overline{CS0}$ ↓ → SO0 floating delay time	tDCSOF	SO0			tsys+200	ns
$\overline{CS0}$ high level width	twHCS	$\overline{CS0}$		tsys+200		ns
$\overline{SCK0}$ cycle time	tKCY	$\overline{SCK0}$	Input mode	2tsys+200		ns
			Output mode	16000/fc		ns
$\overline{SCK0}$ high and low level widths	tKH tKL	$\overline{SCK0}$	Input mode	tsys+100		ns
			Output mode	8000/fc–50		ns
SI0 input setup time (against $\overline{SCK0}$ ↑)	tSIK	SI0	$\overline{SCK0}$ input mode	100		ns
			$\overline{SCK0}$ output mode	200		ns
SI0 input hold time (against $\overline{SCK0}$ ↑)	tKSI	SI0	$\overline{SCK0}$ input mode	tsys+200		ns
			$\overline{SCK0}$ output mode	100		ns
$\overline{SCK0}$ ↓ → SO0 delay time	tKSO	SO0	$\overline{SCK0}$ input mode		tsys+200	ns
			$\overline{SCK0}$ output mode		100	ns

Note 1) tsys indicates three values according to the contents of the clock control register (address; 00FEH) upper 2 bits (CPU clock selection).
tsys [ns] =2000/fc (Upper 2-bit="00"), 4000/fc (Upper 2-bit="01"), 16000/fc (Upper 2-bit="11")

2) The Load of $\overline{SCK0}$ output mode and SO0 output delay time is 50pF+1TTL.

Fig. 4 Serial transfer CH0 timing



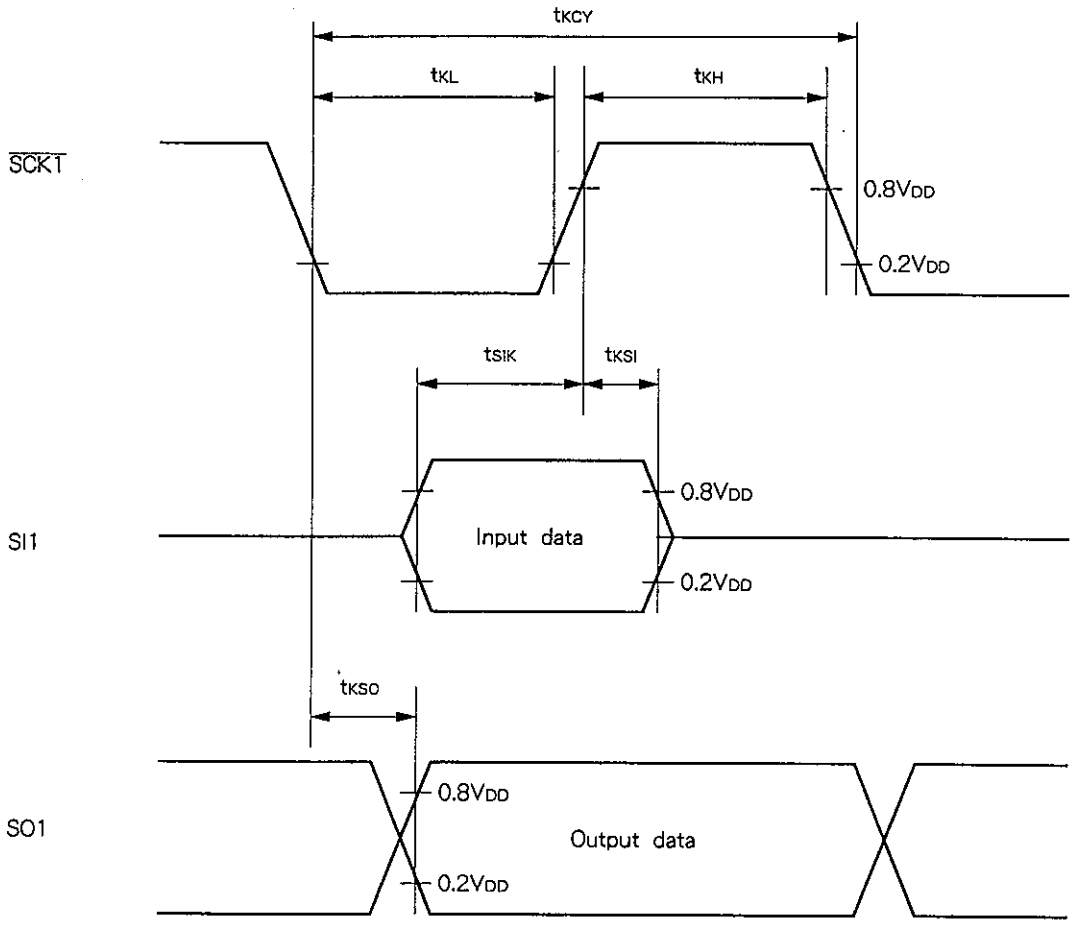
Serial transfer (CH1)

(Ta=–20 to +75°C, V_{DD}=4.5 to 5.5V, Vss=0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{SCK1}$ cycle time	t_{KCY}	$\overline{SCK1}$	Input mode	1000		ns
			Output mode	16000/fc		ns
$\overline{SCK1}$ high and low level widths	t_{KH} t_{KL}	$\overline{SCK1}$	Input mode	400		ns
			Output mode	8000/fc–50		ns
SI1 input setup time (against $\overline{SCK1}$ ↑)	t_{SIK}	SI1	$\overline{SCK1}$ input mode	100		ns
			$\overline{SCK1}$ output mode	200		ns
SI1 input hold time (against $\overline{SCK1}$ ↑)	t_{KSI}	SI1	$\overline{SCK1}$ input mode	200		ns
			$\overline{SCK1}$ output mode	100		ns
$\overline{SCK1}$ ↓ → SO1 delay time	t_{KSO}	SO1	$\overline{SCK1}$ input mode		200	ns
			$\overline{SCK1}$ output mode		100	ns

Note) The Load of $\overline{SCK1}$ output mode and SO1 output delay time is 50pF +1TTL.

Fig. 5 Serial transfer CH1 timing

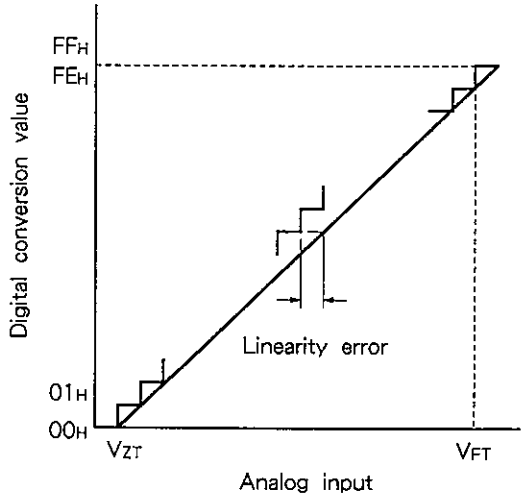


(3) A/D converter characteristics

(Ta=–20 to +75 °C, V_{DD}=AV_{DD}=4.5 to 5.5V, AV_{REF}=4.0V to AV_{DD}, V_{SS}=AV_{SS}=0V)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			Ta=25 °C V_{DD}=AV_{DD}=5.0V V_{SS}=AV_{SS}=0V			±1	LSB
Zero transition voltage	V_{ZT} *1			–10	30	70	mV
Full scale transition voltage	V_{FT} *2			4930	4970	5010	mV
Conversion time	t_{CONV}			160/f_{ADC} *3			µs
Sampling time	t_{SAMP}			12/f_{ADC} *3			µs
Reference input voltage	V_{REF}	AV_{REF}		AV_{DD}–0.5		AV_{DD}	V
Analog input voltage	V_{IAN}	AN0 to AN11		0		AV_{REF}	V
AV_{REF} current	I_{REF}	AV_{REF}	Operating mode		0.6	1.0	mA
	I_{REFS}		SLEEP mode STOP mode 32kHz operation mode			10	µA

Fig. 6. Definitions of A/D converter terms



*1) V_{ZT}: Indicates the value that digital conversion value changes from 00H to 01H and vice versa.

*2) V_{FT}: Indicates the value that digital conversion value changes from FEH to FFH and vice versa.

*3) The value of f_{ADC} is as follows by selecting ADC operation clock (MSC: Address 01FFH bit 0).

When PS2 is selected, f_{ADC}=fc/2

When PS1 is selected, f_{ADC}=fc

(4) Interruption, reset input

(Ta=–20 to +75°C, V_{DD}=4.5 to 5.5V, Vss=0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
External interruption high and low level widths	t_{IH}, t_{IL}	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$ $\overline{NMI}$, PJ0 to PJ7		1		µs
Reset input low level width	t_{RSL}	$\overline{RST}$		8/fc		µs

Fig. 7 Interruption input timing

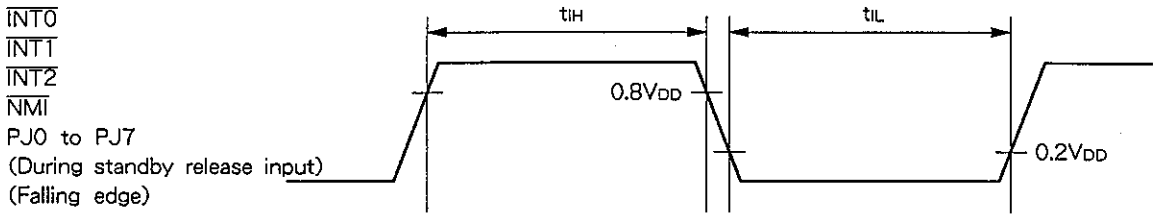
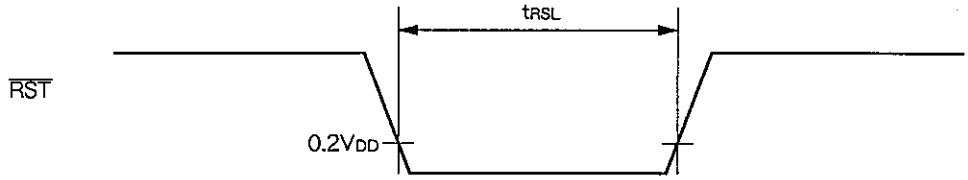


Fig. 8 Reset input timing



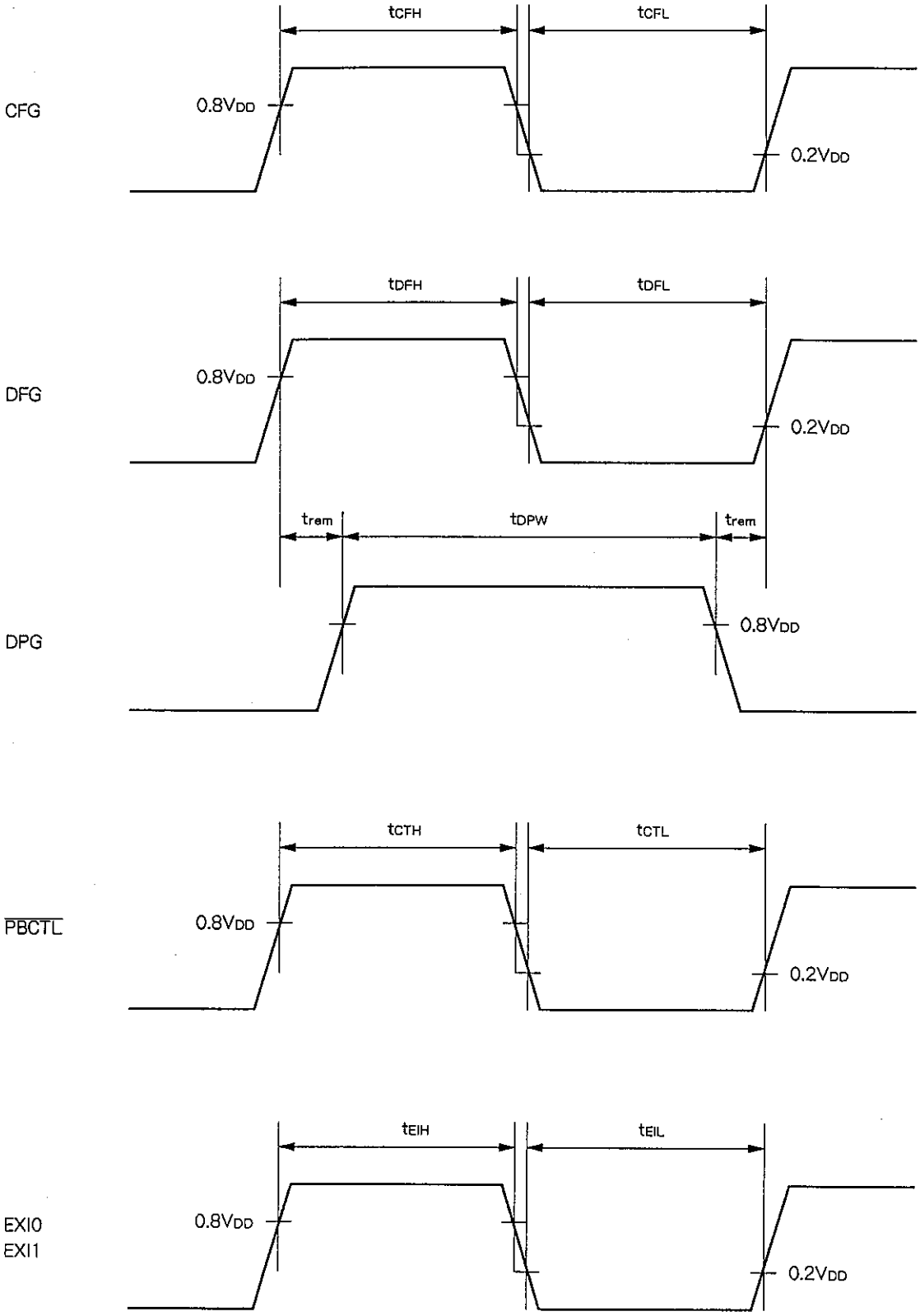
(5) Others

(Ta=–20 to +75°C, V_{DD}=4.5 to 5.5V, Vss=0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
CFG input high and low level widths	t_{CFH}, t_{CFL}	PG0/CFG		tsys+200		ns
DFG input high and low level widths	t_{DFH}, t_{DFL}	PG1/DFG		1000/fc+200		ns
DPG minimum pulse width	t_{DPW}	PG2/DPG		50		ns
DPG minimum removal time	trem	PG2/DPG		50		ns
$\overline{PBCTL}$ input high and low level widths	t_{CTH}, t_{CTL}	PG3/$\overline{PBCTL}$	tsys=2000/fc	tsys+200		ns
EXI input high and low level widths	t_{EIH}, t_{EIL}	PG6/EXI0 PG7/EXI1	tsys=2000/fc	tsys+200		ns

Note) tsys indicates three values according to the contents of the clock control register (address; 00FE$_H$) upper 2 bits (CPU clock selection).
tsys [ns] =2000/fc (Upper 2-bit="00"), 4000/fc (Upper 2-bit="01"), 16000/fc (Upper 2-bit="11")

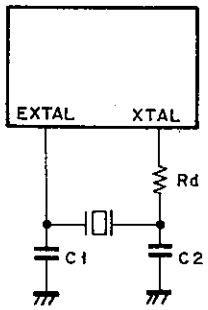
Fig. 9 Other timings



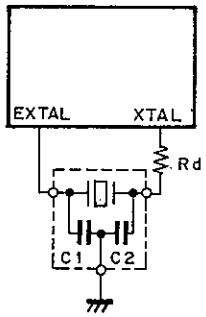
Supplement

Fig. 10 Recommended oscillation circuit

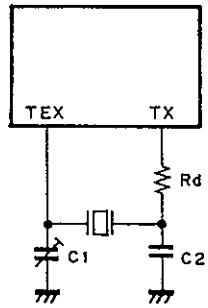
(i)



(ii)



(iii)



Manufacturer	Model	fc (MHz)	C_1 (pF)	C_2 (pF)	Rd (Ω)	Circuit example
MURATA MFG CO., LTD.	CSA8.00MTZ	8.00	30	30	0	(i)
	CST8.00MTW*					(ii)
	CSA10.0MTZ	10.00	30	30	0	(i)
	CST10.0MTW*					(ii)
	CSA12.0MTZ	12.00	30	30	0	(i)
	CST12.0MTW*					(ii)
FUJI SANGYO CO., LTD.	HC-49/U03	8.00	12	12	470	(i)
		10.00				
		12.00				
KINSEKI LTD.	HC-49/U (-S)	8.00	22	22	0	(i)
		10.00				
		12.00	18	18	0	
	P3	32.768kHz	30	39	330k	(iii)

Those marked with an asterisk (*) signify types with built-in ground capacitance (C1,C2).

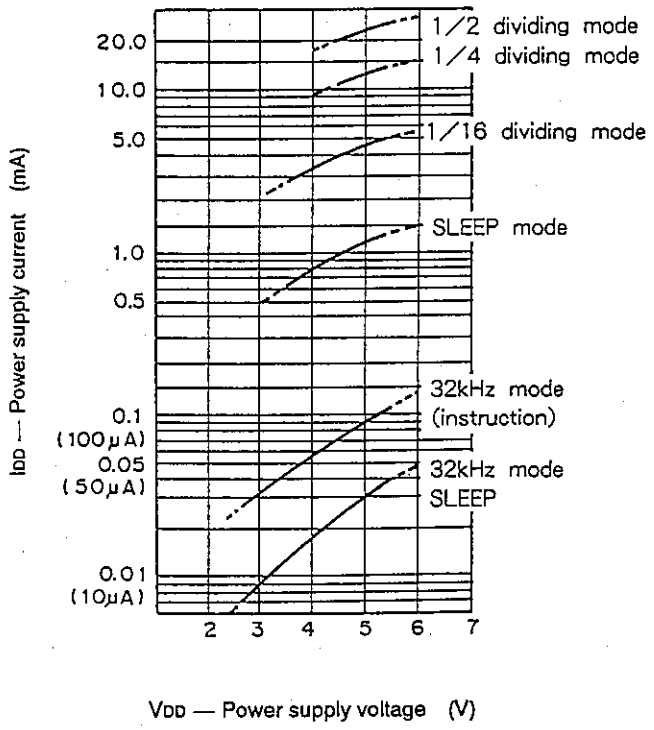
Mask option table

Item	Content	
Reset pin pull-up resistor	Non-existent	Exsistent
Input circuit format Note)	C-MOS schmitt	TTL schmitt

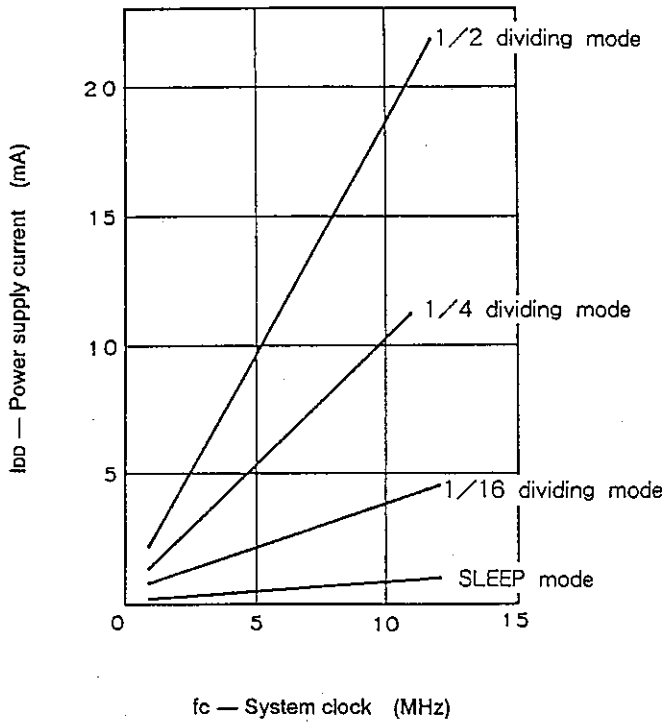
Note) In PG4/SYNC0 pin and PG5/SYNC1 pin, the input circuit format can be selected to every pin.

Characteristics Curve

I_{DD} vs. V_{DD}
(f_c=12MHz, Ta=25 °C, Typical)



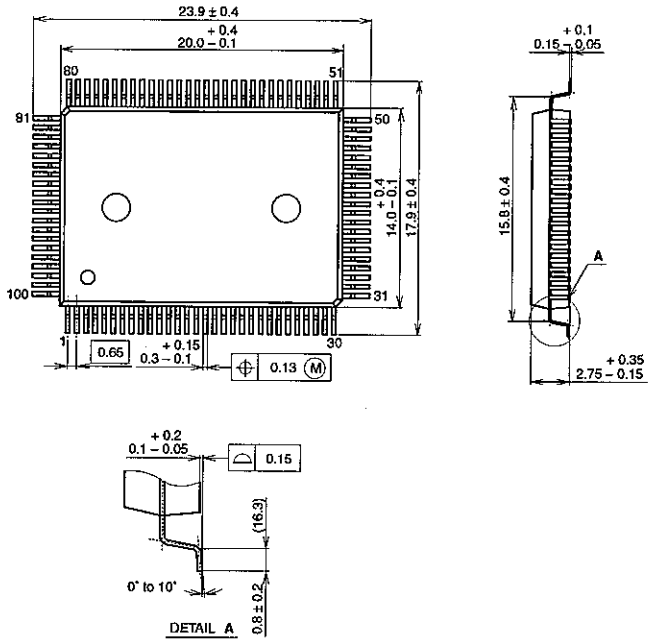
I_{DD} vs. f_c
(V_{DD}=5V, Ta=25 °C, Typical)



Package Outline

Unit: mm

100PIN QFP (PLASTIC)

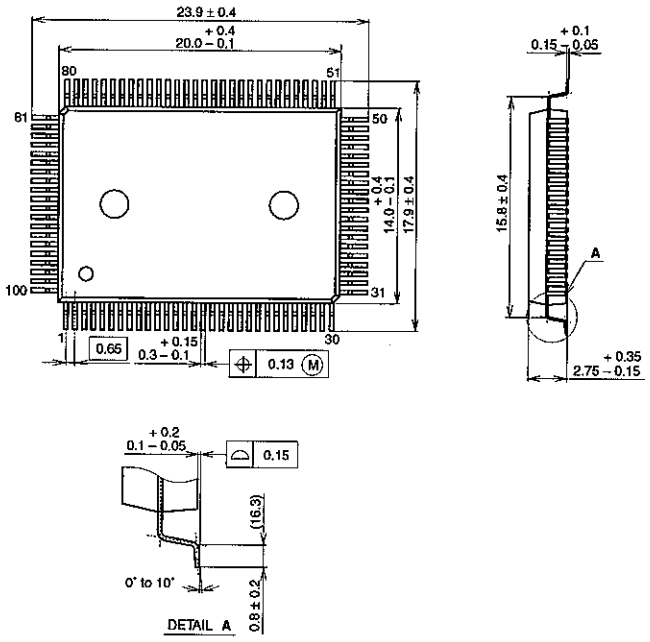


SONY CODE	QFP-100P-L01
EIAJ CODE	QFP100-P-1420
JEDEC CODE	———

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.7g

100PIN QFP (PLASTIC)



SONY CODE	QFP-100P-L01
EIAJ CODE	QFP100-P-1420
JEDEC CODE	———

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.7g

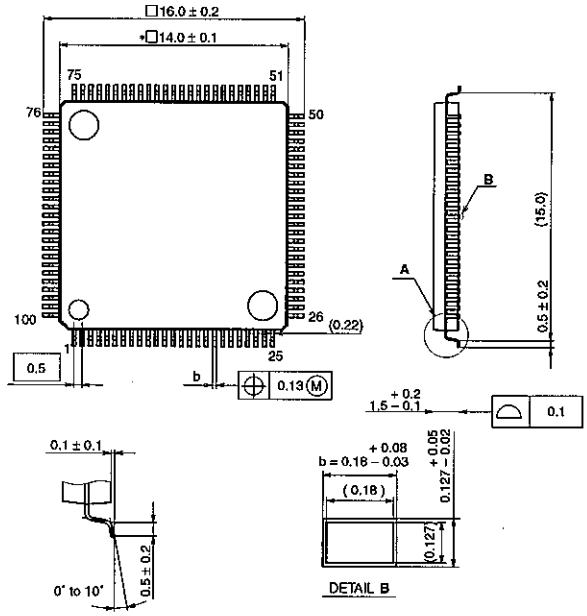
LEAD PLATING SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	42 ALLOY
SOLDER COMPOSITION	Sn-Bi Bi:1-4wt%
PLATING THICKNESS	5-18μm

Package Outline

Unit: mm

100PIN LQFP (PLASTIC)



DETAIL A

DETAIL B

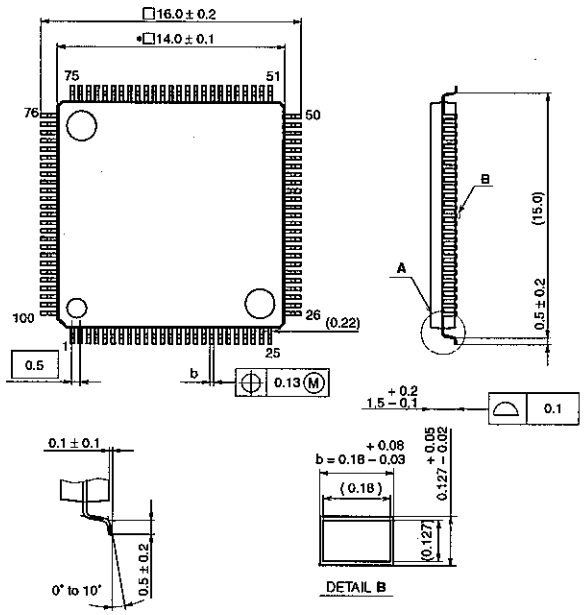
NOTE: Dimension "•" does not include mold protrusion.

SONY CODE	LQFP-100P-L01
EIAJ CODE	P-LQFP100-14x14-0.5
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 / COPPER ALLOY
PACKAGE MASS	0.7g

100PIN LQFP (PLASTIC)



DETAIL A

DETAIL B

NOTE: Dimension "•" does not include mold protrusion.

SONY CODE	LQFP-100P-L01
EIAJ CODE	P-LQFP100-14x14-0.5
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 / COPPER ALLOY
PACKAGE MASS	0.7g

LEAD PLATING SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	42 ALLOY
SOLDER COMPOSITION	Sn-Bi Bi:1-4wt%
PLATING THICKNESS	5-18μm