SONY

CXP82612/82616

## CMOS 8-bit Single Chip Microcomputer

Description

The CXP82612/82616 microcomputer is composed of a CPU, ROM, RAM, and I/O ports. These chips feature many other high-performance circuits in a single-chip CMOS design, including an A/D converter, serial interface, timer/counter, time-base timer, fluorescent display controller/driver, remote control receiver and 32kHz timer/counter.

This device also includes a power-on reset function and sleep/stop functions which can be used to achieve low power consumption.
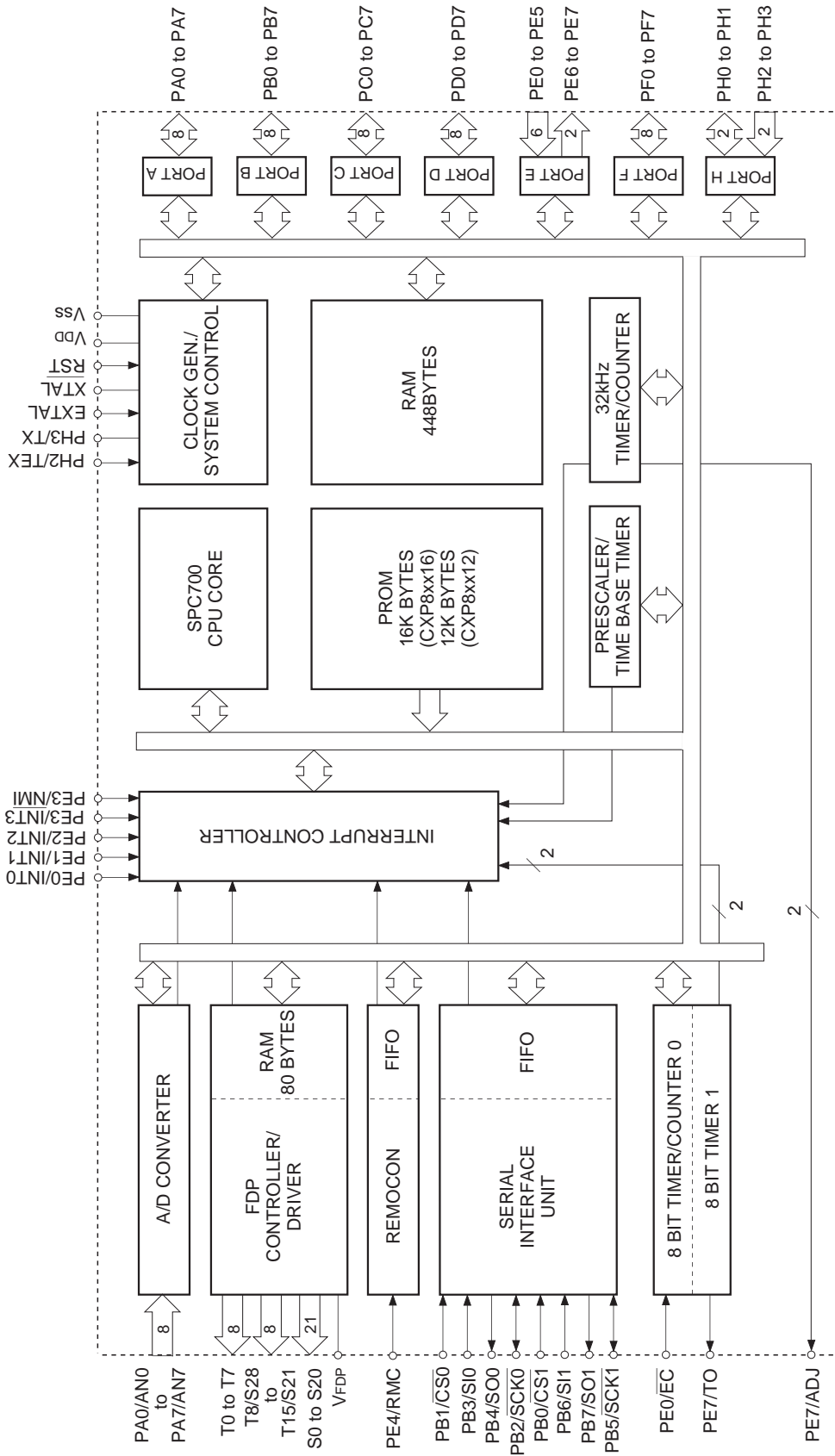
80 pin QFP (Plastic)
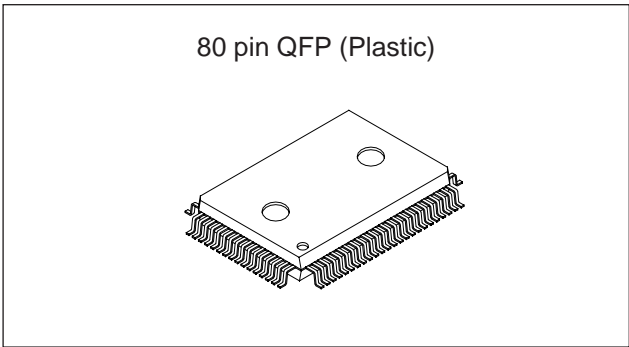
Features

• Instruction set which supports a wide array of data types
   — 213 types of instructions which include 16-bit calculations, multiplication and division arithmetic, and boolean bit operations.
• Minimum instruction cycle   400ns for 10MHz, 122µs/for 32kHz operation
• On-chip ROM   12K bytes (CXP82612)
                                       16K bytes (CXP82616)
• On-chip RAM   448 bytes (Including fluorescent display data area)
• Peripheral functions
   — A/D converter   8-bit, 8-channel, successive approximation system
                                       (conversion rate 32µs/10MHz)
   — Serial interface   On-chip 8-bit, 8-stage FIFO (1 to 8 bytes auto transfer),
                                       1 circuit 2-channel
   — Timers   8-bit timer
                                       8-bit timer/counter
                                       19-bit time base timer
                                       32kHz timer/counter
   — Fluorescent display controller/driver   Maximum of 336 segments display available
                                       1 to 16 digits dynamic display
                                       Dimmer function
                                       High voltage tolerance output (40V)
                                       On-chip pull-down resistor (Mask option)
                                       Hardware key scan function (Maximum of 8×16 key matrix available)
   — Remote control receiver circuit   On-chip 6 stage FIFO 8-bit pulse measurement counter
• Interrupts   13 factors, 13 vectors multi-interruption possible
• Standby mode   Sleep/stop
• Package   80-pin plastic QFP
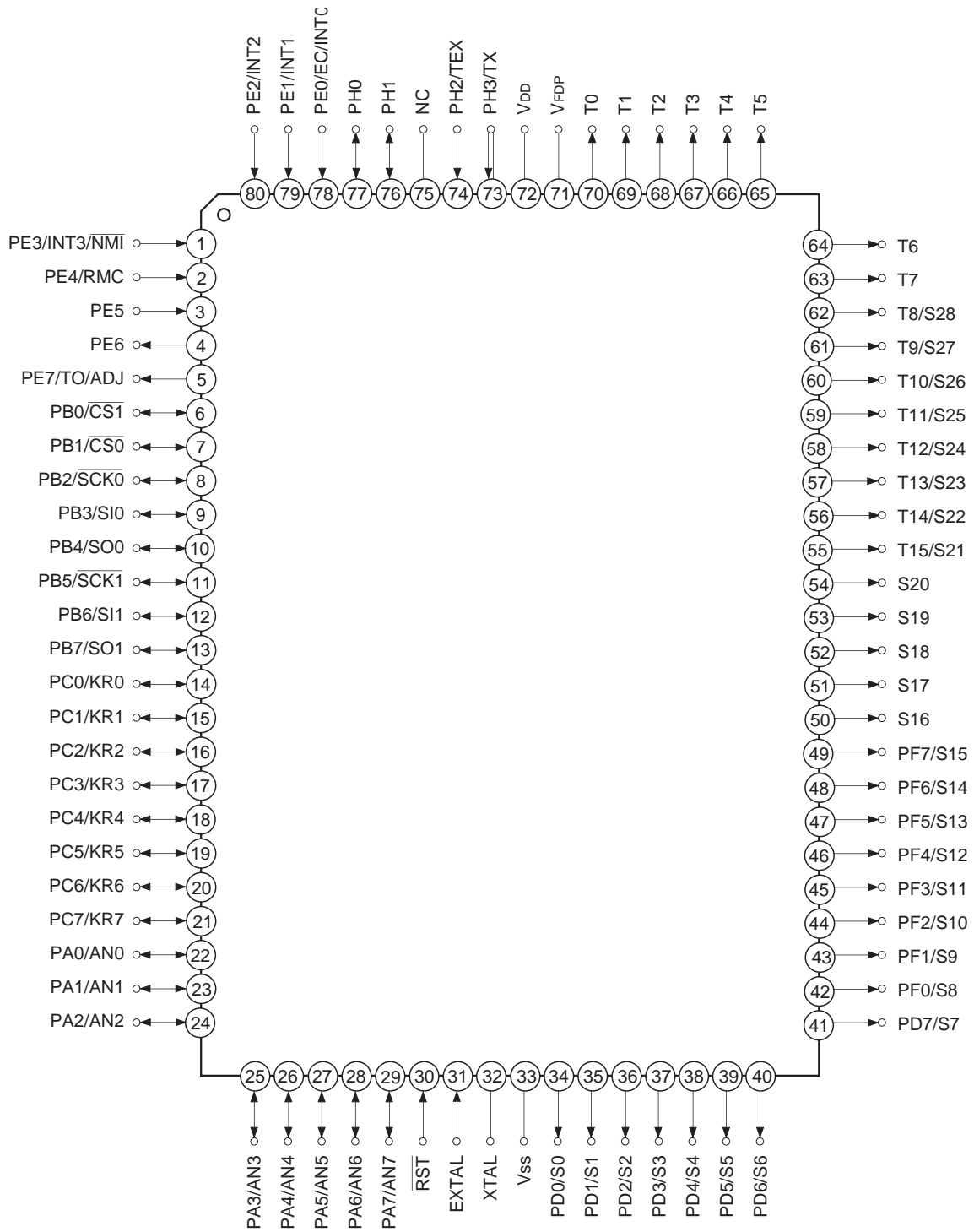• Piggyback/evaluator   CXP82600 80-pin ceramic QFP

Structure

Silicon gate CMOS IC

E93Y22A79-PS

Block Diagram

PA0 to PA7 · PB0 to PB7 · PC0 to PC7 · PD0 to PD7 · PE0 to PE5 · PE6 to PE7 · PF0 to PF7 · PH0 to PH1 · PH2 to PH3

PORT A (8) · PORT B (8) · PORT C (8) · PORT D (8) · PORT E (6) (2) · PORT F (8) · PORT H (2) (2)

CLOCK GEN./SYSTEM CONTROL

RAM 448BYTES

32kHz TIMER/COUNTER

Vss · VDD · RST · XTAL · EXTAL · PH3/TX · PH2/TEX

SPC700 CPU CORE

PROM 16K BYTES (CXP8xx16) 12K BYTES (CXP8xx12)

PRESCALER/TIME BASE TIMER

INTERRUPT CONTROLLER

PE3/NMI · PE3/INT3 · PE2/INT2 · PE1/INT1 · PE0/INT0

A/D CONVERTER

FDP CONTROLLER/DRIVER · RAM 80 BYTES

REMOCON · FIFO

SERIAL INTERFACE UNIT · FIFO

8 BIT TIMER/COUNTER 0 · 8 BIT TIMER 1

PA0/AN0 to PA7/AN7 (8)

T0 to T7 (8) · T8/S28 to T15/S21 (8) · S0 to S20 (21) · VFDP

PE4/RMC

PB1/CS0 · PB3/SI0 · PB4/SO0 · PB2/SCK0 · PB0/CS1 · PB6/SI1 · PB7/SO1 · PB5/SCK1

PE0/EC · PE7/TO · PE7/ADJ

Pin Assignment (Top View)

Pins (left side, top to bottom):
1 PE3/INT3/NMI
2 PE4/RMC
3 PE5
4 PE6
5 PE7/TO/ADJ
6 PB0/CS1
7 PB1/CS0
8 PB2/SCK0
9 PB3/SI0
10 PB4/SO0
11 PB5/SCK1
12 PB6/SI1
13 PB7/SO1
14 PC0/KR0
15 PC1/KR1
16 PC2/KR2
17 PC3/KR3
18 PC4/KR4
19 PC5/KR5
20 PC6/KR6
21 PC7/KR7
22 PA0/AN0
23 PA1/AN1
24 PA2/AN2

Pins (top, left to right):
80 PE2/INT2
79 PE1/INT1
78 PE0/EC/INT0
77 PH0
76 PH1
75 NC
74 PH2/TEX
73 PH3/TX
72 VDD
71 VFDP
70 T0
69 T1
68 T2
67 T3
66 T4
65 T5

Pins (right side, top to bottom):
64 T6
63 T7
62 T8/S28
61 T9/S27
60 T10/S26
59 T11/S25
58 T12/S24
57 T13/S23
56 T14/S22
55 T15/S21
54 S20
53 S19
52 S18
51 S17
50 S16
49 PF7/S15
48 PF6/S14
47 PF5/S13
46 PF4/S12
45 PF3/S11
44 PF2/S10
43 PF1/S9
42 PF0/S8
41 PD7/S7

Pins (bottom, left to right):
25 PA3/AN3
26 PA4/AN4
27 PA5/AN5
28 PA6/AN6
29 PA7/AN7
30 RST
31 EXTAL
32 XTAL
33 Vss
34 PD0/S0
35 PD1/S1
36 PD2/S2
37 PD3/S3
38 PD4/S4
39 PD5/S5
40 PD6/S6

Note) 1. NC (Pin 75) is always connected to V_{DD}.

2. PH3/TX (Pin 73) is input port during port selection; oscillation output during oscillation selection
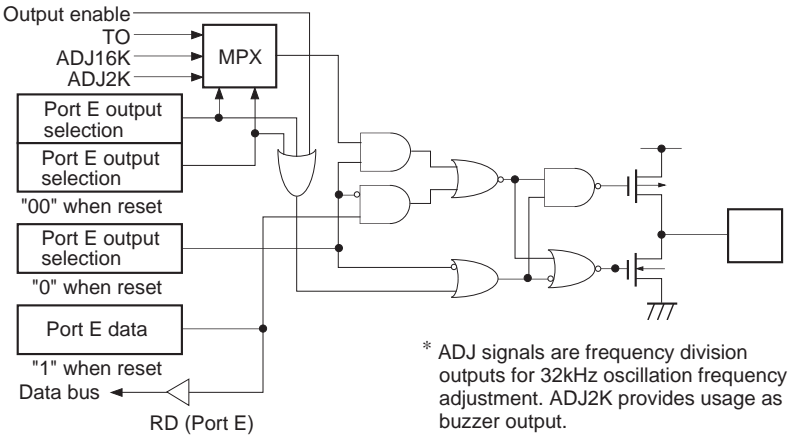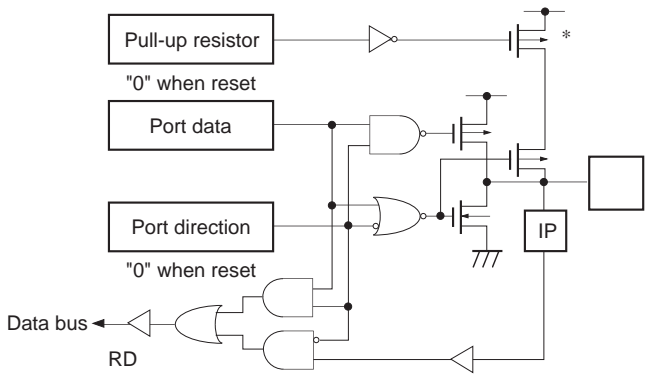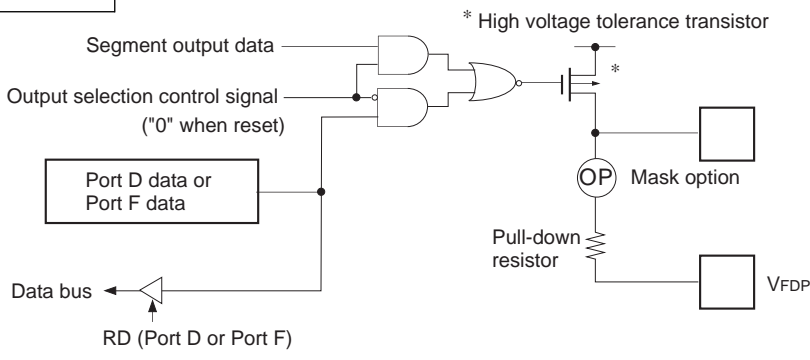
Pin Description

Symbol	I/O	Functions	
PA0/AN0 to PA7/AN7	I/O/Analog Input	(Port A) 8-bit I/O port. I/O can be set in a bit unit. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	Analog inputs to A/D converter. (8 pins)
PB0/$\overline{CS1}$	I/O/Input	(Port B) 8-bit I/O port. I/O can be set in a bit unit. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	Chip select input for serial interface (CH1).
PB1/$\overline{CS0}$	I/O/Input		Chip select input for serial interface (CH0).
PB2/$\overline{SCK0}$	I/O/I/O		Serial clock I/O (CH0).
PB3/SI0	I/O/Input		Serial data input (CH0).
PB4/SO0	I/O/Output		Serial data output (CH0).
PB5/$\overline{SCK1}$	I/O/I/O		Serial clock I/O (CH1).
PB6/SI1	I/O/Input		Serial data input (CH1).
PB7/SO1	I/O/Output		Serial data output (CH1).
PC0/KR0 to PC7/KR7	I/O/Input	(Port C) 8-bit I/O port. I/O can be set in a bit unit. Capable of driving 12mA sink current. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	Key return input for FDP segment signal which performs key scanning.
PE0/INT0/$\overline{EC0}$	Input/Input/Input	(Port E) 8-bit port. Upper 6 bits are for inputs; lower 2 bits are for outputs. (8 pins)	External interrupt requests. (4 pins) — External event input to timer/counter. (1 pin)
PE1/INT1	Input/Input		
PE2/INT2	Input/Input		
PE3/INT3/$\overline{NMI}$	Input/Input/Input		Non-maskable interruption request input.
PE4/RMC	Input/Input		Input for remote control receiver circuit.
PE5	Input		
PE6	Input		
PE7/TO/ADJ	Output/Output		Output for timer/counter rectangular waveform and 32kHz oscillation frequency division.

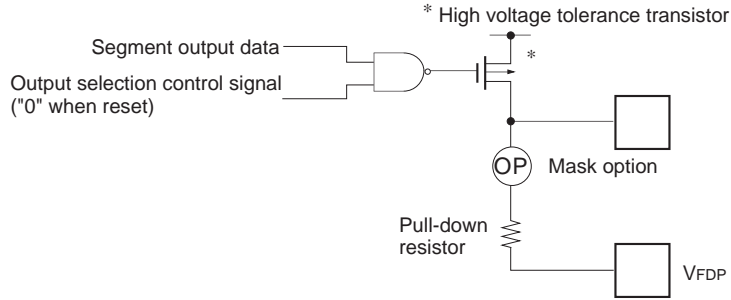| Symbol	I/O	Functions	
PH0 to PH1	I/O	(Port H) 2-bit I/O port. I/O can be set in a bit unit. Incorporation of pull-up resistor can be set through the software in a unit of 2 bits. (2 pins)	
PF0/S8 to PF7/S15	Output/Output	(Port F) 8-bit output port. (8 pins)	Segment signal output for FDP.
S16 to S20	Output	Segment signal output for FDP.	
T8/S28 to T15/S21	Output/Output	Dual purpose output for FDP timing and segment signals.	
T0 to T7	Output	Timing signal output for FDP.	
PD0/S0 to PD7/S7	Output/Output	(Port D) 8-bit output port. (8 pins)	Segment signal output for FDP.
V_{FDP}		Provides voltage for FDP when on-chip resistor is selected under mask option.	
EXTAL	Input	Crystal connectors for system clock oscillation. When the clock is supplied externally, input to EXTAL; opposite phase clock should be input to XTAL.	
XTAL	Output		
PH2/TEX	Input/Input	(Port H) 2-bit input port. (2 pins)	Crystal connectors for 32kHz timer/counter clock oscillation circuit. Connect a 32kHz crystal oscillator between TEX and TX. For usage as event input, connect clock oscillation source to TEX, and leave TX open.
PH3/TX	Input/Output		
$\overline{RST}$	Input	Low-level active. System reset. $\overline{RST}$ is input pin.	
NC		NC. Under normal operating conditions, connect to V_{DD}.	
V_{DD}		Vcc supply.	
Vss		GND	
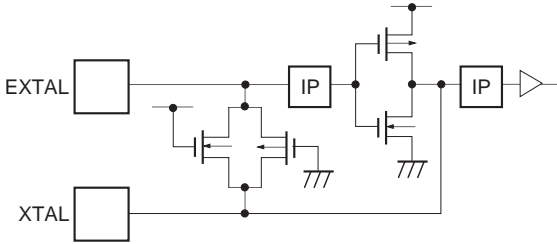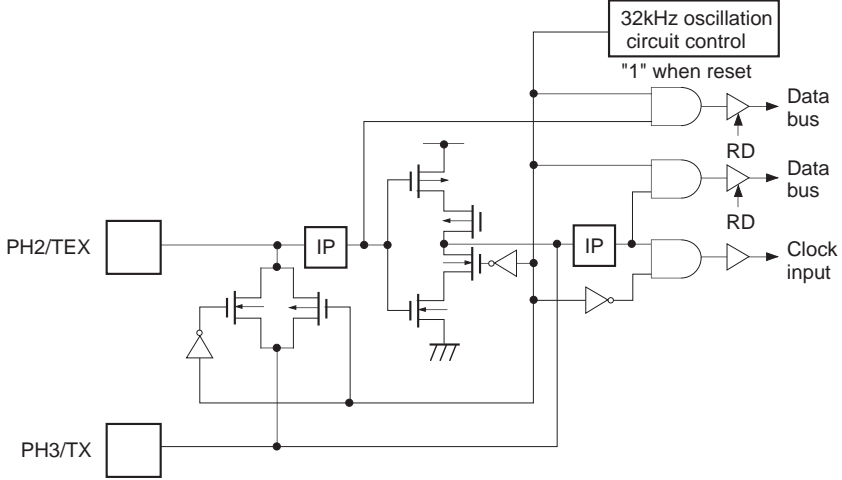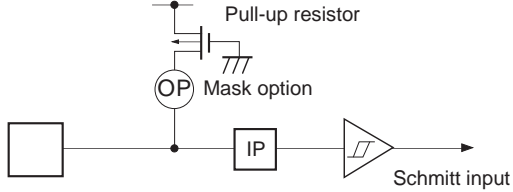
I/O Circuit Format for Pins

Pin	Circuit format	When reset
PA0/AN0 to PA7/AN7 8 pins	Port A	Hi-Z
PB0/$\overline{CS1}$ PB1/$\overline{CS0}$ PB3/SI0 PB6/SI1 4 pins	Port B	Hi-Z
PB2/$\overline{SCK0}$ PB5/$\overline{SCK1}$ 2 pins	Port B	Hi-Z

Pin	Circuit format	When reset
PB4/SO0 PB7/SO1 2 pins	**Port B** Pull-up resistor "0" when reset SO Output enable Port B output selection "0" when reset Port B data Port B direction "0" when reset Data bus ◄── RD (Port B) IP * Pull-up transistors approx. 100kΩ	Hi-Z
PC0/KR0 to PC7/KR7 8 pins	**Port C** Pull-up resistor "0" when reset Port C data Port C direction "0" when reset Data bus ◄── RD (Port C) Key input signal IP *2 *1 *1 Large current drive of 12mA possible *2 Pull-up transistors approx. 100kΩ	Hi-Z
PE0/$\overline{EC}$/INT0 PE1/INT1 PE2/INT2 PE3/INT3/$\overline{NMI}$ PE4/RMC 5 pins	**Port E** Schmitt input IP $\overline{EC}$/INT0 INT1 INT2 INT3/$\overline{NMI}$ RMC Data bus RD (Port E)	Hi-Z
PE5 1 pin	**Port E** IP Data bus RD (Port E)	Hi-Z
PE6 1 pin	**Port E** Port E data "1" when reset Data bus ◄── RD (Port E)	High level

Pin	Circuit format	When reset
PE7/TO/ADJ 1 pin	**Port E** Output enable / TO / ADJ16K / ADJ2K / MPX Port E output selection Port E output selection "00" when reset Port E output selection "0" when reset Port E data "1" when reset Data bus RD (Port E) * ADJ signals are frequency division outputs for 32kHz oscillation frequency adjustment. ADJ2K provides usage as buzzer output.	High level (High level with 150kΩ resistor when reset)
PH0 to PH1 2 pins	**Port H** Pull-up resistor "0" when reset Port data Port direction "0" when reset Data bus RD IP * Pull-up transistors approx. 100kΩ	Hi-Z
PD0/S0 to PD7/S7 PF0/S8 to PF7/S15 16 pins	**Port D** / **Port F** * High voltage tolerance transistor Segment output data Output selection control signal ("0" when reset) Port D data or Port F data OP Mask option Pull-down resistor V_FDP Data bus RD (Port D or Port F)	Hi-Z or Low level (When PD resistor is connected)

Pin	Circuit format	When reset
S16 to S20 T15/S21 to T8/S28 T0 to T7 21 pins	* High voltage tolerance transistor Segment output data Output selection control signal ("0" when reset) OP Mask option Pull-down resistor V_{FDP}	Hi-Z or Low level (When PD resistor is connected)
EXTAL XTAL 2 pins	EXTAL IP IP XTAL • Diagram shows circuit construction for oscillation. • During STOP feedback resistor is disconnected.	Oscillation
PH2/TEX PH3/TX 2 pins	32kHz oscillation circuit control "1" when reset Data bus RD Data bus RD Clock input PH2/TEX IP IP PH3/TX	Oscillation halted port input
$\overline{RST}$ 1 pin	Pull-up resistor OP Mask option IP Schmitt input	High level

Absolute Maximum Ratings

(Vss = 0V)

Item		Symbol	Rating	Unit	Remarks
Supply voltage		V_{DD}	−0.3 to +7.0	V	
Input voltage		V_{IN}	−0.3 to +7.0[*1]	V	
Output voltage		V_{OUT}	−0.3 to +7.0[*1]	V	
Display output voltage		V_{OD}	V_{DD} − 40 to V_{DD} + 0.3	V	As P channel transistor is open drain, V_{DD} voltage is determined as standard.
High level output current		I_{OH}	−5	mA	Other than display output pins[*2]: per pin
		I_{ODH1}	−15	mA	Display output S0 to S20: per pin
		I_{ODH2}	−35	mA	Display output T0 to T7 T8/S28 to T15/S21: per pin
High level total output current		ΣI_{OH}	−40	mA	Total of other than display output pins
		ΣI_{ODH}	−100	mA	Total of display output pins
Low level output current		I_{OL}	15	mA	Port 1 pin
		I_{OLC}	20	mA	Large current port pin[*3]
Low level total output current		ΣI_{OL}	100	mA	Entire pin toral
Operating temperature		Topr	−20 to +75	°C	
Storage temperature		Tstg	−55 to +150	°C	
Allowable power dissipation		P_D	600	mW	

[*1] V_{IN} and V_{OUT} must not exceed V_{DD} + 0.3V.

[*2] Specifies output current of general-purpose I/O ports.

[*3] The large current drive transistor is an N-ch transistor of Port C (PC).

Note) If the absolute maximum ratings are exceed, the LSI could reach permanent breakdown. Also, observing recommended operating conditions is desirable; otherwise, the LSI's reliability could be affected.

SONY

CXP82612/82616

Recommended Operating Conditions (Vss = 0V)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V_{DD}	4.5	5.5	V	High speed mode (1/2, 1/4 clock) guaranteed operation range
		3.5	5.5	V	Low speed mode (1/16 clock) guaranteed operation range
		2.7	5.5	V	Guaranteed operation range with TEX clock
		2.5	5.5	V	Guaranteed data hold operation range during stop
High level input voltage	V_{IH}	$0.7V_{DD}$	V_{DD}	V	*1
	V_{IHS}	$0.8V_{DD}$	V_{DD}	V	Hysteresis input*2
	V_{IHEX}	$V_{DD} - 0.4$	$V_{DD} + 0.3$	V	EXTAL pin*3
Low level input voltage	V_{IL}	0	$0.3V_{DD}$	V	*1
	V_{ILS}	0	$0.2V_{DD}$	V	Hysteresis input*2
	V_{ILEX}	−0.3	0.4	V	EXTAL pin*3
Operating temperature	Topr	−20	+75	°C	

*1 All regular input port (PA, PB3, PB4, PB6, PB7, PC, PE5, PH).

*2 For pins $\overline{RST}$, $\overline{CS0}$, $\overline{CS1}$, $\overline{SCK0}$, $\overline{SCK1}$, $\overline{EC}$/INT0, INT1, INT2, INT3/$\overline{NMI}$, RMC.

*3 Specifies only for external clock input.

9

Electrical Characteristics

DC Characteristics (Ta = −20 to +75°C, Vss = 0V)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
High level output voltage	V_{OH}	PA, PB, PC, PE6, PE7, PH0, PH1	V_{DD} = 4.5V, I_{OH} = −0.5mA	4.0			V
			V_{DD} = 4.5V, I_{OH} = −1.2mA	3.5			V
Low level output voltage	V_{OL}		V_{DD} = 4.5V, I_{OL} = 1.8mA			0.4	V
			V_{DD} = 4.5V, I_{OL} = 3.6mA			0.6	V
		PC	V_{DD} = 4.5V, I_{OL} = 12.0mA			1.5	V
Input current	I_{IHE}	EXTAL	V_{DD} = 5.5V, V_{IH} = 5.5V	0.5		40	μA
	I_{ILE}		V_{DD} = 5.5V, V_{IL} = 0.4V	−0.5		−40	μA
	I_{IHT}	TEX	V_{DD} = 5.5V, V_{IL} = 5.5V	0.1		10	μA
	I_{ILT}		V_{DD} = 5.5V, V_{IL} = 0.4V	−0.1		−10	μA
	I_{ILR}	$\overline{RST}$[1]	V_{DD} = 5.5V, V_{IL} = 0.4V	−1.5		−400	μA
	I_{IL}	PA to PC[2] PH0[2], PH1[2]				−50	μA
			V_{DD} = 4.5V, V_{IL} = 4.0V	−3.3			μA
Display output current	I_{OH}	S0 to S20	V_{DD} = 4.5V V_{OH} = V_{DD} − 2.5V	−8			mA
		S21/T15 to S28/T8 T0 to T7		−20			mA
Open drain output leak current (P-CH Tr off state)	I_{LOL}	S0 to S20 S21/T15 to S28/T8 T0 to T7	V_{DD} = 5.5V V_{OL} = V_{DD} − 35V V_{FDP} = V_{DD} − 35V			−20	μA
Pull down resistor[3]	R_L	S0 to S20 S21/T15 to S28/T8 T0 to T7	V_{DD} = 5V V_{OD} − V_{FDP} = 30V	60	100	270	kΩ
Input/Output leak current	I_{IZ}	PA to PC[2], PH0[2], PH1[2], $\overline{RST}$[2]	V_{DD} = 5.5V V_I = 0, 5.5V			±10	μA

Item	Symbol	Pin	Codition	Min.	Typ.	Max.	Unit
Supply current[*4]	I_{DD1}	V_{DD}	High-speed mode operation (1/2 frequency divider clock)		20	40	mA
			V_{DD} = 5.5V, 10MHz crystal oscillation (C_1 = C_2 = 15pF)				
	I_{DD2}		V_{DD} = 3V, 32kHz crystal oscillation (C_1 = C_2 = 47pF)		35	100	μA
	I_{DDS1}		Sleep mode		1.2	8	mA
			V_{DD} = 5.5V, 10MHz crystal oscillation (C_1 = C_2 = 15pF)				
	I_{DDS2}		V_{DD} = 3V, 32kHz crystal oscillation (C_1 = C_2 = 47pF)		9	30	μA
	I_{DDS3}		Stop mode V_{DD} = 5.5V, termination of 32kHz and 10MHz crystal oscillation.			30	μA
Input capacitance	C_{IN}	For pins other than S0 to S28, T0 to T7, PE6, PE7, V_{DD}, Vss, V_{FDP}	1MHz clock 0V other than the measured pins		10	20	pF

[*1] $\overline{RST}$ specifies the input current when pull-up resistor has been selected; leakage current when no resistor has been selected.

[*2] Pins PA to PC, PH0, and PH1 specifies the input current when pull-up resistor has been selected; leakage current when no resistor has been selected.

[*3] Applies when the on-chip pull-down resistor is selected under the mask option.

[*4] All output pins are left open.

AC Characteristics

(1) Clock timing　　　　　　　　　　　　　　　　(Ta = −20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
System clock frequency	f_C	XTAL EXTAL	Fig. 1, Fig. 2	1		10	MHz
System clock input pulse width	t_{XL}, t_{XH}	EXTAL	Fig. 1, Fig. 2 External clock drive	37.5			ns
System clock input rise and fall time	t_{CR}, t_{CF}	EXTAL	Fig. 1, Fig. 2 External clock drive			200	ns
Event count input clock pulse width	t_{EH}, t_{EL}	$\overline{EC}$	Fig. 3	t_{sys} + 50*			ns
Event count input clock rise and fall time	t_{ER}, t_{EF}	$\overline{EC}$	Fig. 3			20	ms
System clock frequency	f_C	TEX TX	V_{DD} = 2.7 to 5.5V Fig. 2 (32kHz clock applied condition)		32.768		kHz
Event count input clock input pulse width	t_{TL}, t_{TH}	TEX	Fig. 3	10			µs
Event count input clock rise and fall time	t_{TR}, t_{TF}	TEX	Fig. 3			20	ms

* t_{sys} indicates the three values below according to the upper two bits (CPU clock selection) of the clock control register (address: 00FE$_H$).

　t_{sys} [ns] = 2000/fc (upper two bits = "00"), 4000/fc (upper two bits = "01"), 16000/fc (upper two bits = "11")
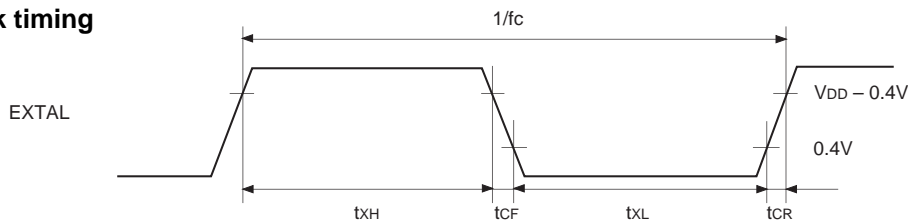
Fig. 1. Clock timing
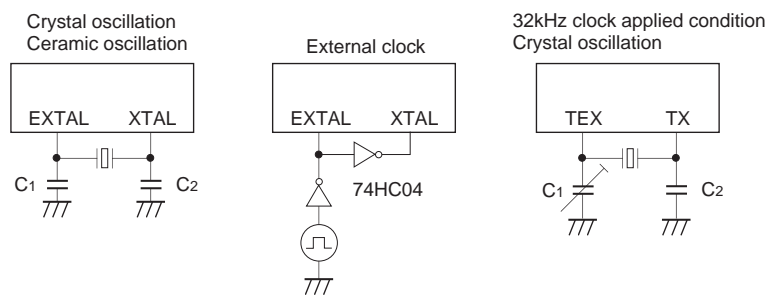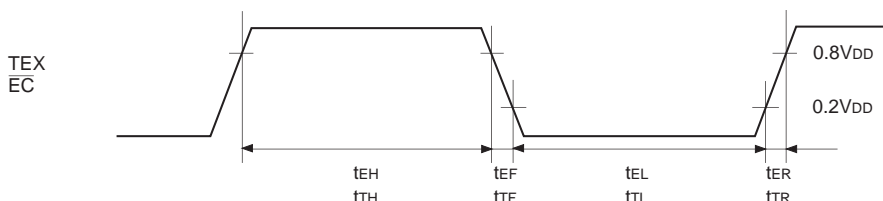

Fig. 2. Clock applied conditions

Fig. 3. Event count clock timing

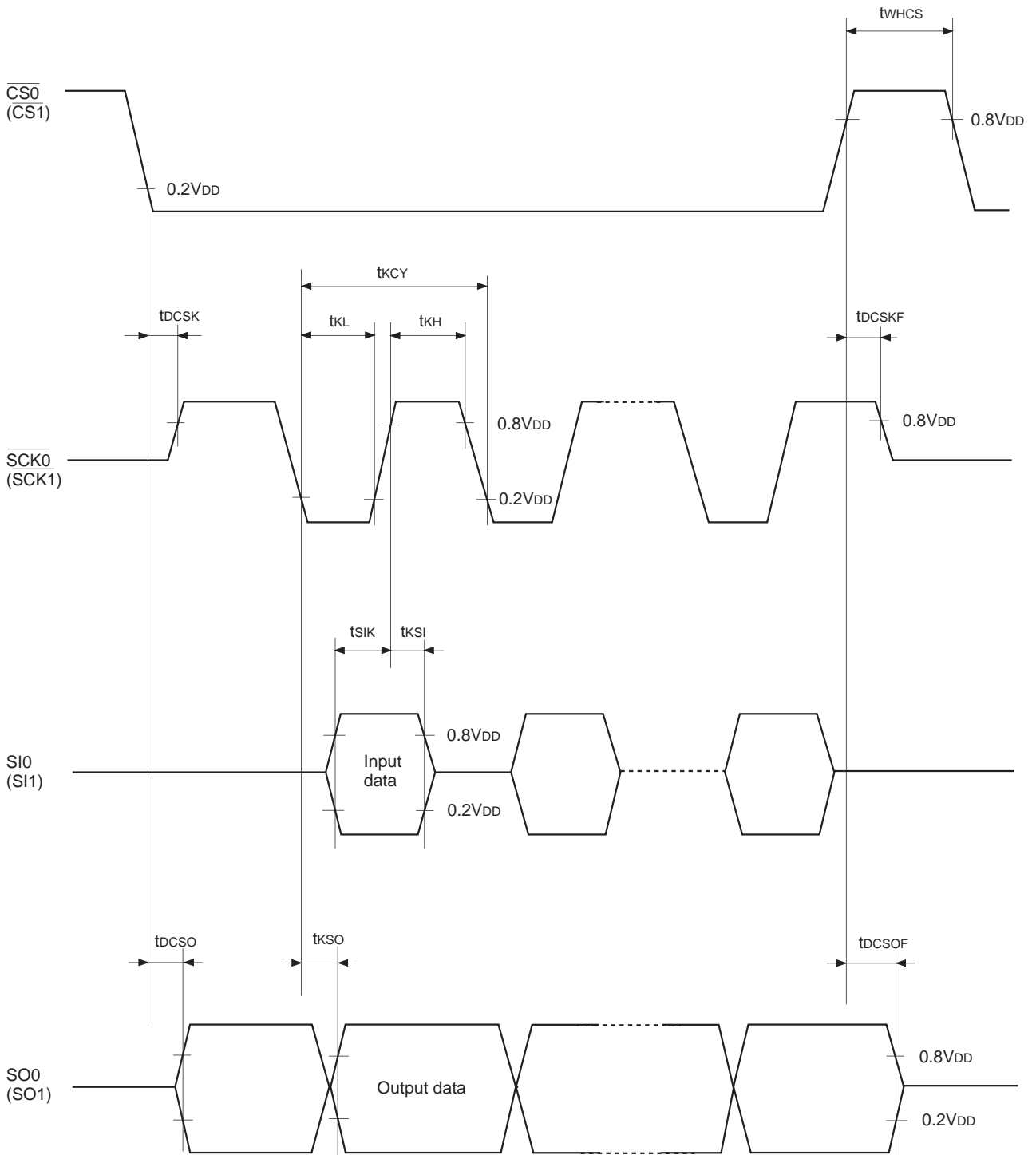**(2) Serial transfer**   (Ta = −20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{CS0}\downarrow\rightarrow\overline{SCK0}$ ($\overline{CS1}\downarrow\rightarrow\overline{SCK1}$) delay time	t_{DCSK}	$\overline{SCK0}$ ($\overline{SCK1}$)	Chip select transfer mode ($\overline{SCK0}$ ($\overline{SCK1}$) = output mode)		tsys + 200	ns
$\overline{CS0}\uparrow\rightarrow\overline{SCK0}$ ($\overline{CS1}\uparrow\rightarrow\overline{SCK1}$) float delay time	t_{DCSKF}	$\overline{SCK0}$ ($\overline{SCK1}$)	Chip select transfer mode ($\overline{SCK0}$ ($\overline{SCK1}$) = output mode)		tsys + 200	ns
$\overline{CS0}\downarrow\rightarrow SO0$ ($\overline{CS1}\downarrow\rightarrow SO1$) delay time	t_{DCSO}	SO0 (SO1)	Chip select transfer mode		tsys + 200	ns
$\overline{CS0}\uparrow\rightarrow SO0$ ($\overline{CS1}\uparrow\rightarrow SO1$) float delay time	t_{DCSOF}	SO0 (SO1)	Chip select transfer mode		tsys + 200	ns
$\overline{CS0}$ ($\overline{CS1}$) high level width	t_{WHCS}	$\overline{CS0}$ ($\overline{CS1}$)	Chip select transfer mode	tsys + 200		ns
$\overline{SCK0}$ ($\overline{SCK1}$) cycle time	t_{KCY}	$\overline{SCK0}$ ($\overline{SCK1}$)	Input mode	2tsys + 200		ns
			Output mode	16000/fc		ns
$\overline{SCK0}$ ($\overline{SCK1}$) high and low level widths	t_{KH} t_{KL}	$\overline{SCK0}$ ($\overline{SCK1}$)	Input mode	tsys + 100		ns
			Output mode	8000/fc − 50		ns
SI0 (SI1) input setup time (for SCK0 $\uparrow$ ($\overline{SCK1}$ $\uparrow$))	t_{SIK}	SI0 (SI1)	$\overline{SCK0}$ ($\overline{SCK1}$) input mode	100		ns
			$\overline{SCK0}$ ($\overline{SCK1}$) output mode	200		ns
SI0 (SI1) input hold time (for SCK0 $\uparrow$ ($\overline{SCK1}$ $\uparrow$))	t_{KSI}	SI0 (SI1)	$\overline{SCK0}$ ($\overline{SCK1}$) input mode	tsys + 200		ns
			$\overline{SCK0}$ ($\overline{SCK1}$) output mode	100		ns
$\overline{SCK0}\downarrow\rightarrow SO0$ ($\overline{SCK1}\downarrow\rightarrow SO1$) delay time	t_{KSO}	SO0 (SO1)	$\overline{SCK0}$ ($\overline{SCK1}$) input mode		tsys + 200	ns
			$\overline{SCK0}$ ($\overline{SCK1}$) output mode		100	ns

Note 1) tsys indicates the three values below according to the upper two bits (CPU clock selection) of the control register clock (address: 00FE$_H$).

tsys [ns] = 2000/fc (upper two bits = "00"), 4000/fc (upper two bits = "01"), 16000/fc (upper two bits = "11")

Note 2) The load condition for the $\overline{SCK0}$ ($\overline{SCK1}$) output mode, SO0 (SO1) output delay time is 50pF + 1TTL.

**Fig. 4. Serial transfer CH0 timing**

(3) A/D converter characteristics   (Ta = −20 to +75°C, V_{DD} = 4.5 to 5.5V, AV_{REF} = 4.0 to AV_{DD}, Vss = 0V)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error						±3	LSB
Zero transition voltage	V_{ZT}*1		Ta = 25°C V_{DD} = 5.0V Vss = 0V	−10	−70	150	mV
Full-scale transition voltage	V_{FT}*2			4930	5050	5120	mV
Conversion time	t_{CONV}			160/f_{ADC}*3			μs
Sampling time	t_{SAMP}			12/f_{ADC}*3			μs
Analog input voltage	V_{IAN}	AN0 to AN7		0		AV_{REF}	V

Fig. 5. Definition of A/D converter terms
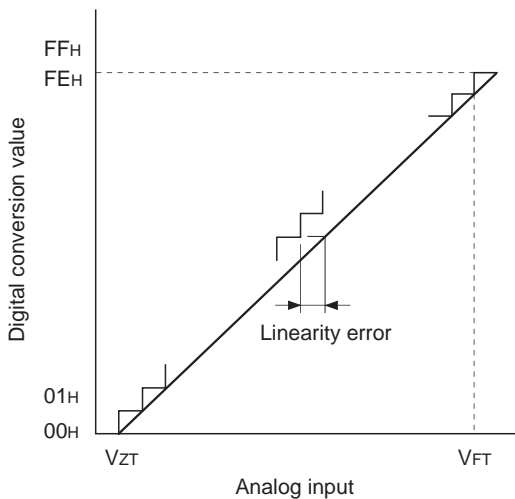
*1 V_{ZT} : Value at which the digital conversion value changes from 00H to 01H and vice versa.
*2 V_{FT} : Value at which the digital conversion value changes from FEH to FFH and vice versa.
*3 f_{ADC} indicates the below values due to the bit6 (CKS) of A/D control register (address: 00F9H) and the Bit7 (PCK1) and Bit6 (PCK0) of clock control register (address: 00FEH)

CKS / PCK1, 0	0 (φ/2 selection)	1 (φ selection)
00 (φ = f_{EX}/2)	f_{ADC} = f_C/2	f_{ADC} = f_C
01 (φ = f_{EX}/4)	f_{ADC} = f_C/4	f_{ADC} = f_C/2
11 (φ = f_{EX}/16)	f_{ADC} = f_C/16	f_{ADC} = f_C/8

– 17 –

SONY

CXP82612/82616

(4) Interruption, reset input   (Ta = −20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
External interruption high and low level widths	t_{IH} t_{IL}	INT0 INT1 INT2 INT3 $\overline{NMI}$		1		μs
Reset input low level width	t_{RSL}	$\overline{RST}$		32/fc		μs

Fig 6. Interruption input timing
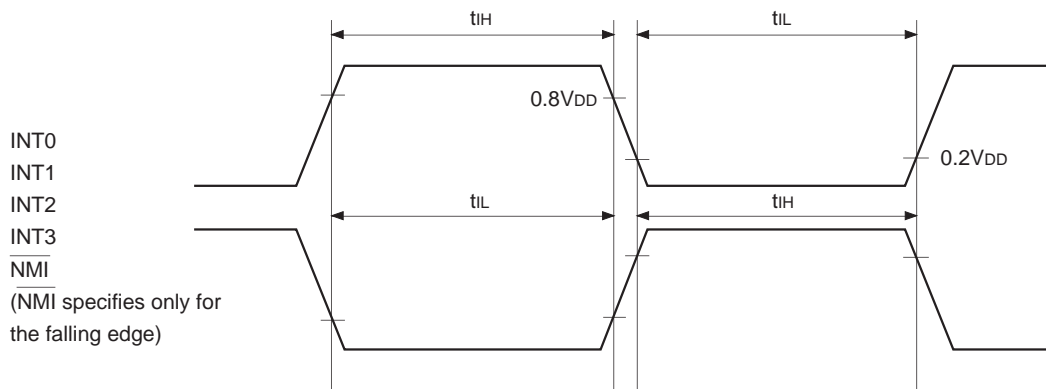
Fig. 7. $\overline{RST}$ input timing

– 18 –
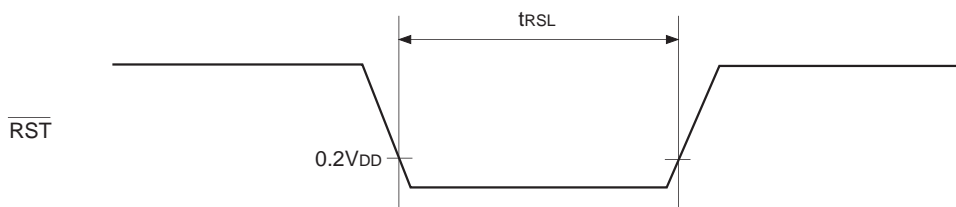
Appendix

Fig. 8. Recommended oscillation circuit
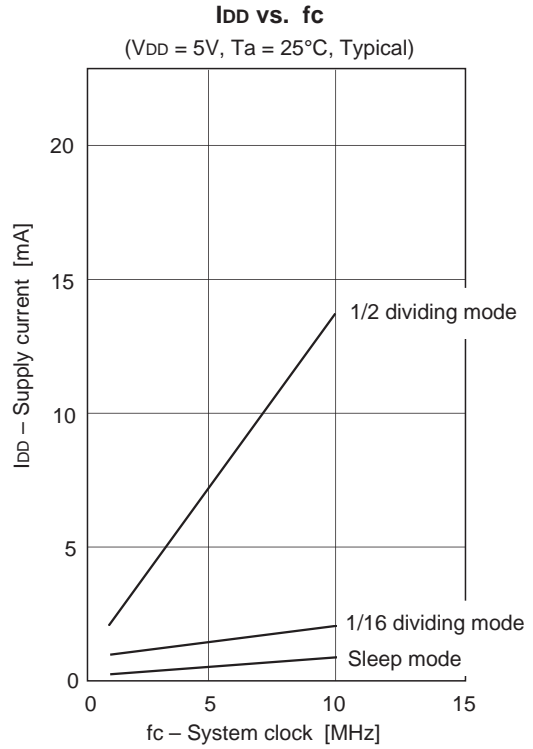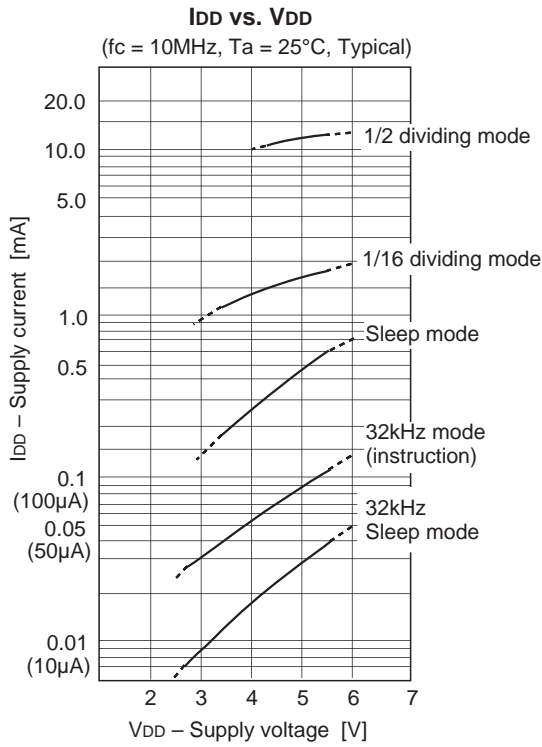
(i) Main clock   (ii) Main clock   (iii) Sub clock
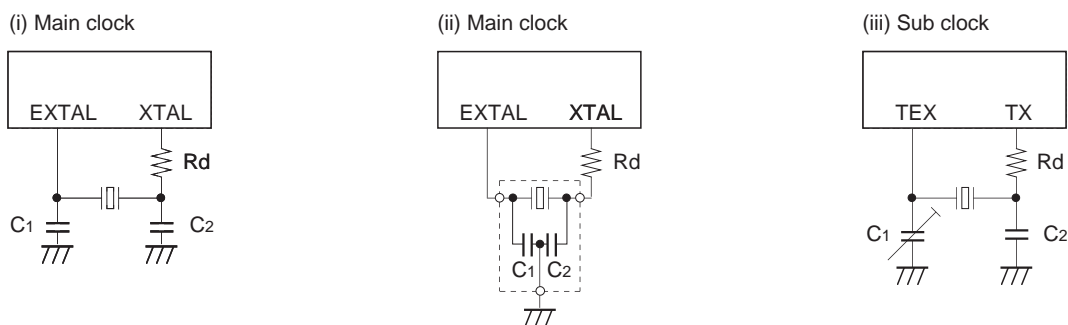
Manufacturer	Model	fc (MHz)	C_1 (pF)	C_2 (pF)	Rd (Ω)	Circuit example
MURATA MFG CO., LTD.	CSA4.19MG	4.19	30	30	0	(i)
	CSA8.00MTZ	8.00				
	CSA10.0MTZ	10.00				
	CST4.19MGW*	4.19				(ii)
	CST8.00MTW*	8.00				
	CST10.0MTW*	10.00				
RIVER ELETEC CORPORATION	HC-49/U03	4.19	12	12	0	(i)
		8.00				
		10.00				
KINSEKI LTD.	HC-49/U (-S)	4.19	27	27	0	
		8.00				
		10.00	20	20		
	P3	32.768kHz	50	22	1M	(iii)

Those marked with an asterisk (∗) signify types with built-in ground capacitance (C_1, C_2).

Mask Option Table
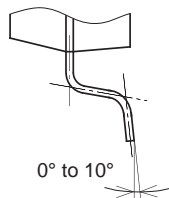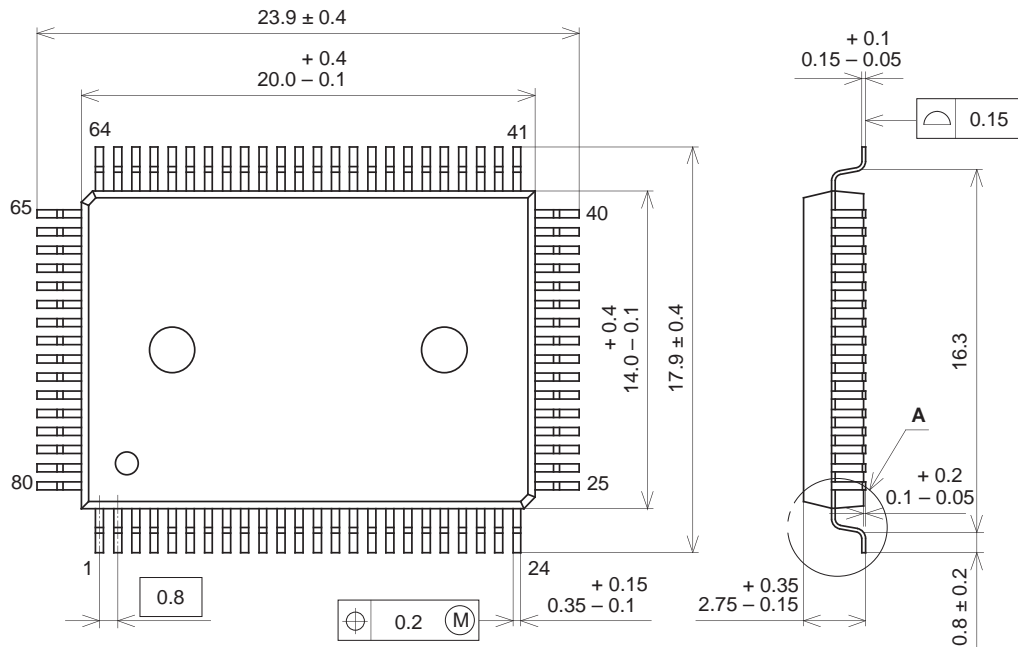
Item	Content	
Reset pin pull-up resistor	Non-existent	Existent
High voltage tolerance pull-down resistor	Non-existent	Existent (selected every pin)

Charactreistics Curves

I_{DD} vs. V_{DD}
(fc = 10MHz, Ta = 25°C, Typical)

I_{DD} – Supply current [mA]

- 1/2 dividing mode
- 1/16 dividing mode
- Sleep mode
- 32kHz mode (instruction)
- 32kHz Sleep mode

V_{DD} – Supply voltage [V]

I_{DD} vs. fc
(V_{DD} = 5V, Ta = 25°C, Typical)

I_{DD} – Supply current [mA]

- 1/2 dividing mode
- 1/16 dividing mode
- Sleep mode

fc – System clock [MHz]

Package Outline   Unit : mm

80PIN QFP (PLASTIC)

23.9 ± 0.4

+ 0.4
20.0 − 0.1

+ 0.1
0.15 − 0.05

△ 0.15

64   41

65   40

+ 0.4
14.0 − 0.1

17.9 ± 0.4

16.3

A

+ 0.2
0.1 − 0.05

80   25

1   24

0.8

⊕ 0.2 ⓜ

+ 0.15
0.35 − 0.1

+ 0.35
2.75 − 0.15

0.8 ± 0.2

0° to 10°

DETAIL **A**

SONY CODE	QFP-80P-L01
EIAJ CODE	QFP080-P-1420
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.6g