

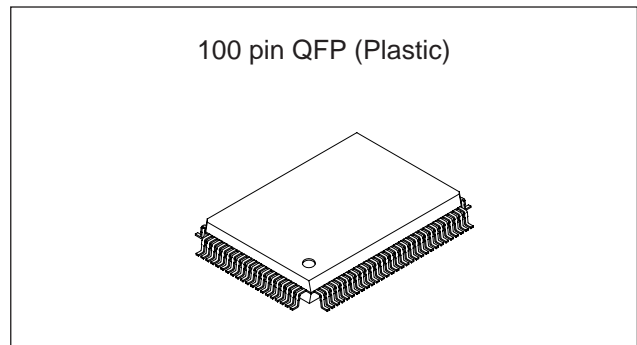
CMOS 8-bit Single Chip Microcomputer

Description

The CXP828P60 is a CMOS 8-bit single chip microcomputer integrating on a single chip an A/D converter, serial interface, timer/counter, time base timer, capture timer/counter, fluorescent display panel controller/driver, remote control reception circuit, and PWM output circuit besides the basic configurations of 8-bit CPU, PROM, RAM, and I/O port.

The CXP828P60 also provides sleep/stop function that enables lower power consumption.

CXP828P60 is the PROM-incorporated version of the CXP82860 with built-in mask ROM. This provides the additional feature of being able to write directly into the program. Thus, it is most suitable for evaluation use during system development and for small-quantity production.



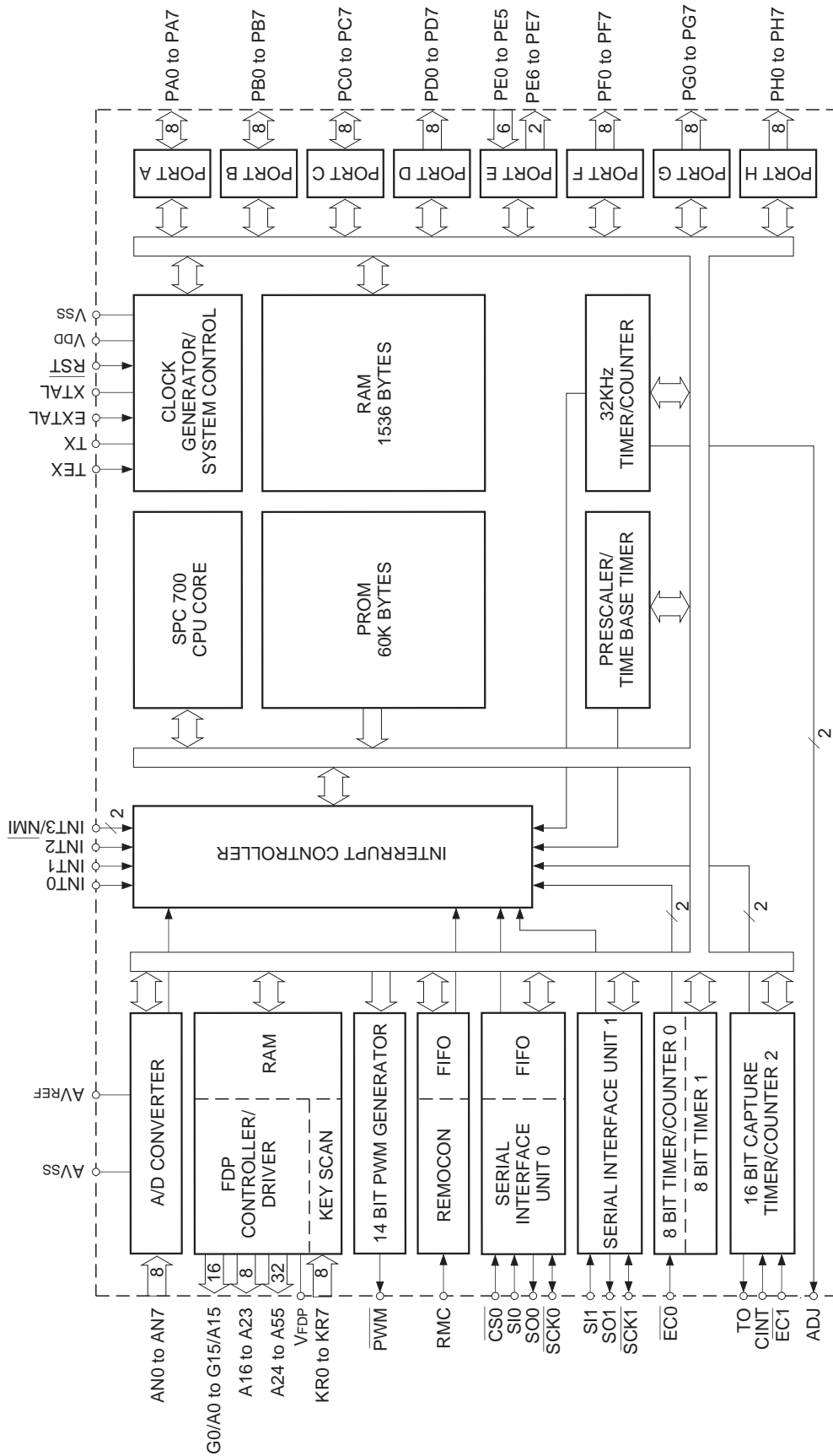
Structure

Silicon gate CMOS IC

Features

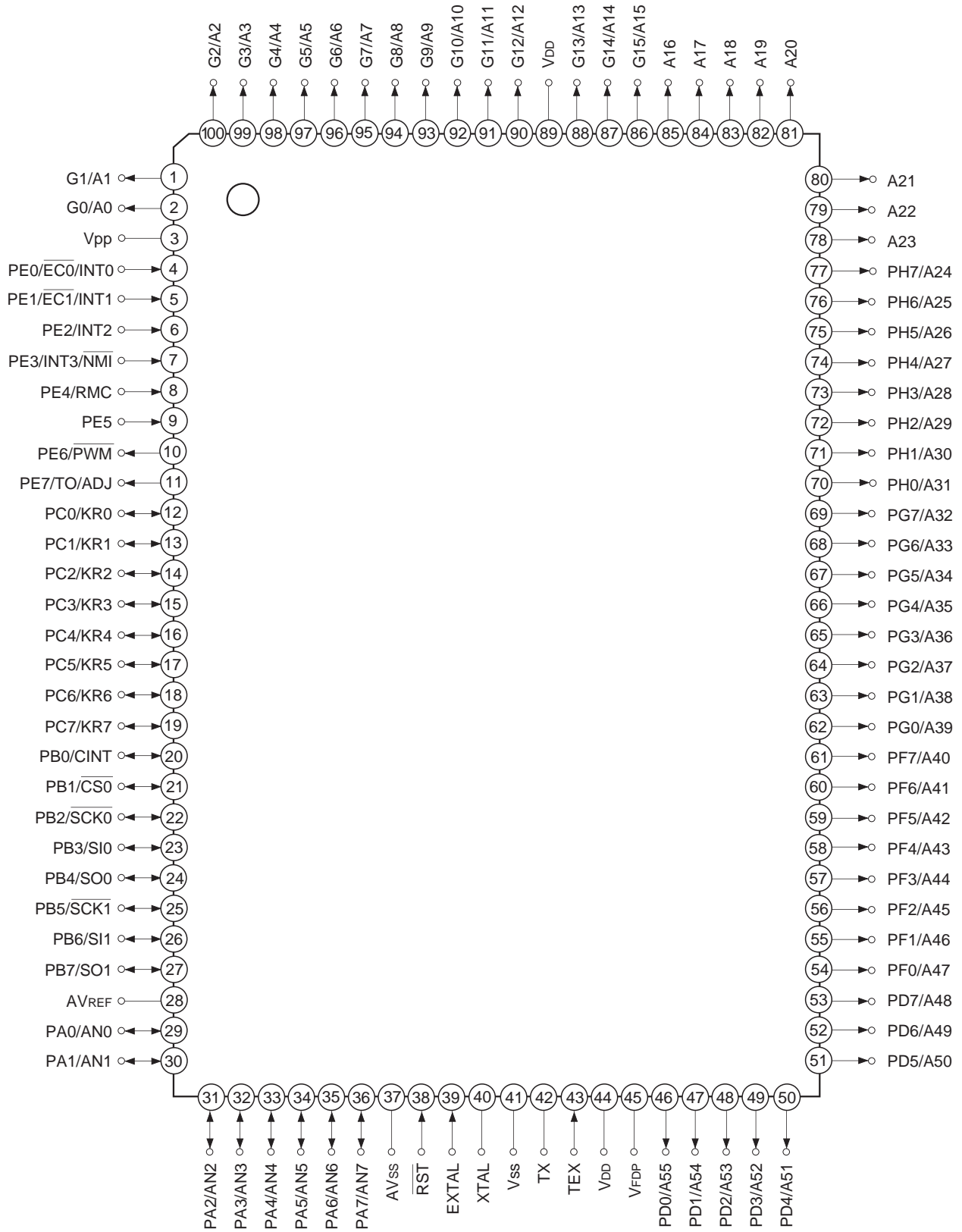
- Wide-range instruction system (213 instructions) to cover various types of data
 - 16-bit arithmetic/multiplication and division/Boolean bit operation instructions
- Minimum instruction cycle
 - 400ns at 10MHz operation
 - 122μs at 32kHz operation
- Incorporated PROM capacity
 - 60K bytes
- Incorporated RAM capacity
 - 1536 bytes (including fluorescent display area)
- Peripheral functions
 - A/D converter
 - 8 bit, 8 channels, successive approximation method (Conversion time of 32μs/10MHz)
 - Serial interface
 - 8-bit, 8-stage FIFO incorporated (Auto transfer for 1 to 8 bytes), 1 channel
 - 8-bit clock synchronized type, 1 channel
 - Timer
 - 8-bit timer, 8-bit timer/counter, 19-bit time base timer
 - 16-bit capture timer/counter, 32kHz timer/counter
 - Fluorescent display panel controller/driver
 - Supports the universal grid fluorescent display panel.
 - High voltage drive output port of 56 pins (40V)
 - Maximum of 640 segments display possible
 - Display timing number of 1 to 20
 - Dimmer function
 - Incorporated pull-down resistor
 - Hardware key scan function (Maximum of 16 x 8 key matrix supportable)
 - Remote control reception circuit
 - 8-bit pulse measurement counter, 6-stage FIFO
 - PWM output
 - 14 bits, 1 channel
- Interruption
 - 16 factors, 15 vectors, multi-interruption possible
- Standby mode
 - SLEEP/STOP
- Package
 - 100-pin plastic QFP

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Block Diagram

Pin Assignment (Top View)



Note) V_{pp} (Pin 3) must be connected to V_{DD}.

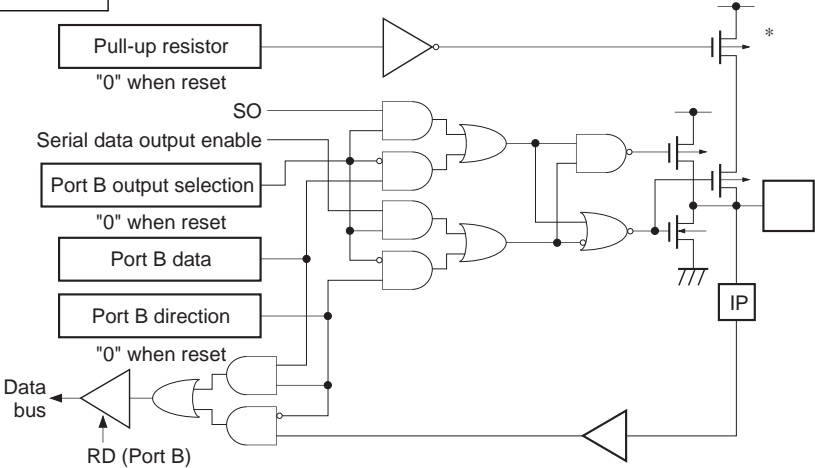
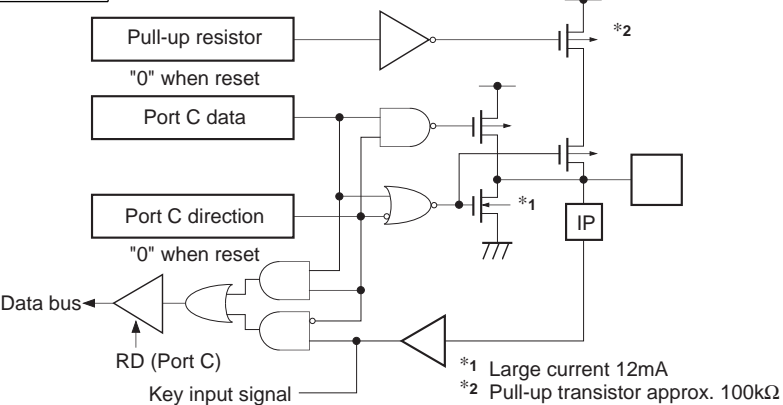
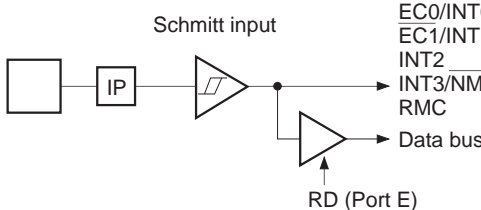
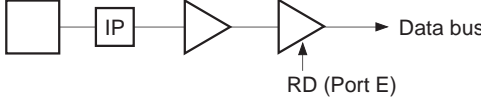
Pin Description

Pin code	I/O	Functions		
PA0/AN0 to PA7/AN7	I/O/ Analog input	(Port A) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of the pull-up resistance can be set through the software in a unit of 4 bits. (8pins)	Analog inputs to A/D converter. (8 pins)	
PB0/CINT	I/O/Input	(Port B) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of the pull-up resistance can be set through the software in a unit of 4 bits. (8 pins)	Capture input to 16-bit timer/counter.	
PB1/ $\overline{\text{CS}}_0$	I/O/Input		Chip select input for serial interface (CH0).	
PB2/ $\overline{\text{SCK}}_0$	I/O/I/O		Serial clock I/O (CH0).	
PB3/SI0	I/O/Input		Serial data input (CH0).	
PB4/SO0	I/O/Output		Serial data output (CH0).	
PB5/ $\overline{\text{SCK}}_1$	I/O/I/O		Serial clock I/O (CH1).	
PB6/SI1	I/O/Input		Serial data input (CH1).	
PB7/SO1	I/O/Output		Serial data output (CH1).	
PC0/KR0 to PC7/KR7	I/O/Input	(Port C) 8-bit I/O port. I/O can be set in a unit of single bits. Capable of driving 12mA sync current. Incorporation of the pull-up resistance can be set through the software in a unit of 4 bits. (8 pins)	Serves as key return inputs when operating key scan with fluorescent display panel (FDP) segment signal. (8 pins)	
PD0/A55 to PD7/A48	Output/Output	(Port D) 8-bit output port. (8 pins)	FDP segment signal (anode connection) outputs.	
PE0/INT0/ $\overline{\text{EC}}_0$	Input/Input/Input	(Port E) 8-bit port. Lower 6 bits are for inputs; upper 2 bits are for outputs. (8 pins)	Inputs for external interruption request. (4 pins)	External event inputs for timer/counter. (2 pins)
PE1/INT1/ $\overline{\text{EC}}_1$	Input/Input/Input			Non-maskable interruption request input.
PE2/INT2	Input/Input		Remote control reception circuit input.	
PE3/INT3/ NMI	Input/Input/Input		14-bit PWM output.	
PE4/RMC	Input/Input		Output for the 16-bit timer/counter rectangular waves, and 32kHz oscillation frequency division.	
PE5	Input			
PE6/ $\overline{\text{PWM}}$	Output/Output			
PE7/TO/ADJ	Output/Output/ Output			
PF0/A47 to PF7/A40	Output/Output	(Port F) 8-bit output port. (8pins)	FDP segment signal (anode connection) outputs.	

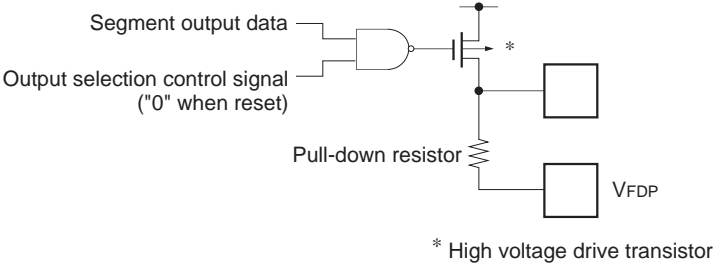
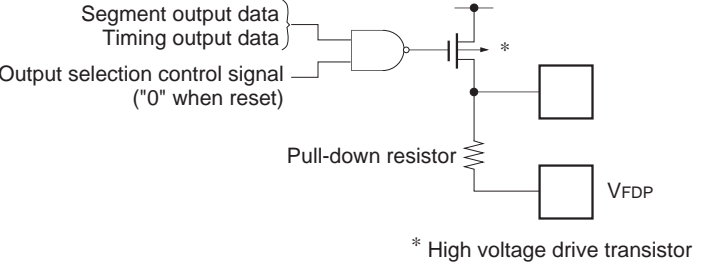
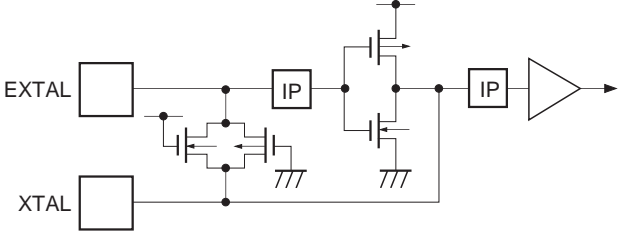
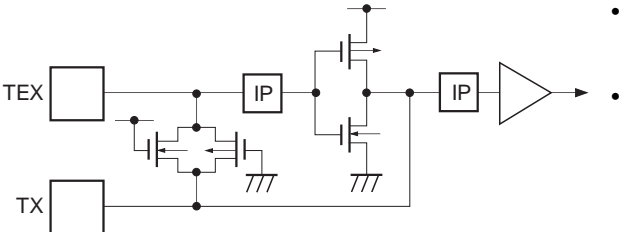
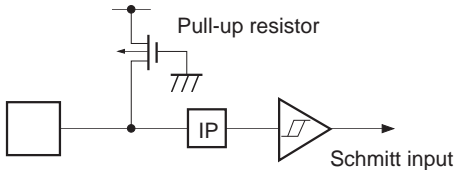
Pin code	I/O	Functions	
PG0/A39 to PG7/A32	Output/Output	(Port G) 8-bit output port. (8 pins)	FDP segment signal (anode connection) outputs.
PH0/A31 to PH7/A24	Output/Output	(Port H) 8-bit output port. (8 pins)	FDP segment signal (anode connection) outputs. (8 pins)
A16 to A23	Output	FDP segment signal (anode connection) outputs. (8 pins)	
G0/A0 to G15/A15	Output/Output	Outputs for FDP timing signals (grid connection)/segment signals (anode connection). (16 pins)	
V _{FDP}		FDP voltage supply for incorporated pull-down (PD) resistor.	
EXTAL	Input	Crystal connectors for system clock oscillation. When the clock is supplied externally, input to EXTAL; opposite phase clock should be input to XTAL.	
XTAL	Output		
TEX	Input	Crystal connectors for 32kHz timer/counter clock oscillation. For usage as event input, input to TEX, and open TX.	
TX	Output		
$\overline{\text{RST}}$	Input	Low-level active, system reset.	
AV _{REF}	Input	Reference voltage input for A/D converter.	
AV _{SS}		A/D converter GND.	
V _{DD}		V _{CC} supply.	
V _{pp}		V _{CC} supply for incorporated PROM writing. Connect to V _{DD} during normal operation.	
V _{SS}		GND.	

I/O Circuit Format for Pins

Pin	Circuit format	When reset
<p>PA0/AN0 to PA7/AN7</p> <p>8 pins</p>	<p>Port A</p> <p>Pull-up resistor "0" when reset</p> <p>Port A data</p> <p>Port A direction "0" when reset</p> <p>Data bus</p> <p>RD (Port A)</p> <p>Port A input selection "0" when reset</p> <p>Input multiplexer</p> <p>A/D converter</p> <p>* Pull-up transistor approx. 100kΩ</p>	<p>Hi-Z</p>
<p>PB0/CINT PB1/$\overline{\text{CS0}}$ PB3/SI0 PB6/SI1</p> <p>4 pins</p>	<p>Port B</p> <p>Pull-up resistor "0" when reset</p> <p>Port B data</p> <p>Port B direction "0" when reset</p> <p>Data bus</p> <p>RD (Port B)</p> <p>CINT CS0 SI0 SI1</p> <p>Schmitt input</p> <p>* Pull-up transistor approx. 100kΩ</p>	<p>Hi-Z</p>
<p>PB2/$\overline{\text{SCK0}}$ PB5/$\overline{\text{SCK1}}$</p> <p>2 pins</p>	<p>Port B</p> <p>Pull-up resistor "0" when reset</p> <p>SCK OUT</p> <p>Serial clock output enable</p> <p>Port B output selection "0" when reset</p> <p>Port B data</p> <p>Port B direction "0" when reset</p> <p>Data bus</p> <p>RD (Port B)</p> <p>SCK in</p> <p>Schmitt input</p> <p>* Pull-up transistor approx. 100kΩ</p>	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>PB4/SO0 PB7/SO1</p> <p>2 pins</p>	<p>Port B</p>  <p>* Pull-up transistor approx. 100kΩ</p>	<p>Hi-Z</p>
<p>PC0/KR0 to PC7/KR7</p> <p>8 pins</p>	<p>Port C</p>  <p>*1 Large current 12mA *2 Pull-up transistor approx. 100kΩ</p>	<p>Hi-Z</p>
<p>PE0/$\overline{EC0}$/INT0 PE1/$\overline{EC1}$/INT1 PE2/INT2 PE3/INT3/\overline{NMI} PE4/RMC</p> <p>5 pins</p>	<p>Port E</p> 	<p>Hi-Z</p>
<p>PE5</p> <p>1 pin</p>	<p>Port E</p> 	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>PE6/PWM</p> <p>1 pin</p>	<p>Port E</p>	<p>High level</p>
<p>PE7/TO/ADJ</p> <p>1 pin</p>	<p>Port E</p>	<p>High level (with approx. 150kΩ resistor when reset)</p>
<p>PD0/A55 to PD7/A48 PF0/A47 to PF7/A40 PG0/A39 to PG7/A32 PH0/A31 to PH7/A24</p> <p>32 pins</p>	<p>Port D Port F Port G Port H</p>	<p>Hi-Z or Low level (when PD resistor is connected)</p>

Pin	Circuit format	When reset
<p>A16 to A23</p> <p>8 pins</p>	 <p>* High voltage drive transistor</p>	<p>Hi-Z or Low level (when PD resistor is connected)</p>
<p>G0/A0 to G15/A15</p> <p>16 pins</p>	 <p>* High voltage drive transistor</p>	<p>Hi-Z or Low level (when PD resistor is connected)</p>
<p>EXTAL XTAL</p> <p>2 pins</p>	 <ul style="list-style-type: none"> • Diagram shows circuit composition during oscillation. • Feedback resistor is removed and XTAL becomes High level during stop. 	<p>Oscillation</p>
<p>TEX TX</p> <p>2 pins</p>	 <ul style="list-style-type: none"> • Diagram shows circuit composition during oscillation. • When the operation of the oscillation circuit is stopped by the software, the feedback resistor is removed, and TEX becomes Low level and TX becomes High level. 	<p>Oscillation</p>
<p>$\overline{\text{RST}}$</p> <p>1 pin</p>	 <p>Pull-up resistor</p> <p>Schmitt input</p>	<p>Low level</p>

Absolute Maximum Ratings

(V_{SS} = 0V reference)

Item	Symbol	Rating	Unit	Remarks
Supply voltage	V _{DD}	-0.3 to +7.0	V	
	V _{pp}	-0.3 to +13.0	V	Incorporated PROM
	AV _{SS}	-0.3 to +0.3	V	
A/D converter GND voltage	AV _{SS}	-0.3 to +0.3	V	
A/D converter reference voltage	AV _{REF}	-0.3 to +7.0* ¹	V	
FDP display supply voltage	V _{FDP}	-40* ² to +7.0* ¹	V	
Input voltage	V _{IN}	-0.3 to +7.0* ¹	V	
Output voltage	V _{OUT}	-0.3 to +7.0* ¹	V	
Display output voltage	V _{OD}	-40* ² to +7.0* ¹	V	
High level output current	I _{OH}	-5	mA	All pins excluding display outputs* ³ (value per pin)
	I _{ODH1}	-15	mA	Display outputs A20 to A55 (value per pin)
	I _{ODH2}	-50	mA	Display outputs G0/A0 to G15/A15, and A16 to A19 (value per pin)
High level total output current	∑I _{OH}	-30	mA	Total for all pins excluding display outputs
	∑I _{ODH}	-120	mA	Total for all display outputs
Low level output current	I _{OL}	15	mA	Port (value per pin)
	I _{OLC}	20	mA	Large current port (value per pin)* ⁴
Low level total output current	∑I _{OL}	100	mA	Total for all output pins
Operating temperature	T _{opr}	-20 to +75	°C	
Storage temperature	T _{stg}	-55 to +150	°C	
Allowable power dissipation	P _D	600	mW	

*1) V_{IN}, V_{OUT}, V_{OD} and AV_{REF} must not exceed V_{DD} + 0.3V.

*2) V_{FDP} and V_{OD} must not exceed V_{DD} - 40V.

*3) Specifies output current of general-purpose I/O ports.

*4) The large current drive transistor is the N-CH transistor of Port C (PC).

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should be conducted under the recommended operating conditions. Exceeding these conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions

(V_{SS} = 0V reference)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V _{DD}	4.5	5.5	V	Guaranteed operation range during high-speed mode (1/2, 1/4 frequency dividing clock)
		3.5	5.5	V	Guaranteed operation range during low-speed mode or SLEEP mode (1/16 frequency dividing clock)
		2.7	5.5	V	Guaranteed operation range with TEX clock
		2.5	5.5	V	Guaranteed data hold range during STOP
High level input voltage	V _{IH}	0.7V _{DD}	V _{DD}	V	*1
	V _{IHS}	0.8V _{DD}	V _{DD}	V	Hysteresis input*2
	V _{IHEX}	V _{DD} - 0.4	V _{DD} + 0.3	V	EXTAL*3
Low level input voltage	V _{IL}	0	0.3V _{DD}	V	*1
	V _{ILS}	0	0.2V _{DD}	V	Hysteresis input*2
	V _{ILEX}	-0.3	0.4	V	EXTAL*3
Operating temperature	Topr	-10	+75	°C	

*1) Value for each pin of normal input port (PA, PB4, PB7, PC).

*2) Value of the following pins: $\overline{\text{RST}}$, $\overline{\text{CINT}}$, $\overline{\text{CS0}}$, $\overline{\text{SCK0}}$, $\overline{\text{SCK1}}$, $\overline{\text{EC0/INT0}}$, $\overline{\text{EC1/INT1}}$, INT2, INT3/ $\overline{\text{NMI}}$, RMC.

*3) Specifies only during external clock input.

Electrical Characteristics

DC Characteristics

(Ta = -10 to +75°C, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output current	VOH	PA, PB, PC, PE6, PE7	VDD = 4.5V, IOH = -0.5mA	4.0			V
			VDD = 4.5V, IOH = -1.2mA	3.5			V
Low level output current	VOL		VDD = 4.5V, IOL = 1.8mA			0.4	V
			VDD = 4.5V, IOL = 3.6mA			0.6	V
Input current	IIHE	EXTAL	VDD = 5.5V, VIH = 5.5V	0.5		40	μA
			VDD = 5.5V, VIL = 0.4V	-0.5		-40	μA
	IIHT	TEX	VDD = 5.5V, VIH = 5.5V	0.1		10	μA
			VDD = 5.5V, VIL = 0.4V	-0.1		-10	μA
	IILR	RST	VDD = 5.5V, VIL = 0.4V	-1.5		-400	μA
				IIL	PA to PC*1	-50	
		VDD = 4.5V, VIL = 4.0V	-3.3				μA
Display output current	IOH	A20 to A55		-8			mA
		G0/A0 to G15/A15 A16 to A19	VDD = 4.5V VOH = VDD - 2.5V	-30			mA
Open drain output leakage current (P-CH Tr off state)	ILOL	G0/A0 to G15/A15 A16 to A55	VDD = 5.5V VOL = VDD - 35V VFDP = VDD - 35V			-20	μA
Pull-down resistance	RL	G0/A0 to G15/A15 A16 to A55	VDD = 5V VOD - VFDP = 30V	60	100	270	kΩ
I/O leakage current	IIZ	PA to PC*1 PE0 to PE5 RST	VDD = 5.5V VI = 0, 5.5V			±10	μA

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Power supply current*2	I _{DD1}	V _{DD}	High-speed mode operation (1/2 frequency dividing clock)		22	50	mA
			V _{DD} = 5.5V, 10MHz crystal oscillation (C ₁ = C ₂ = 15pF)				
	I _{DD2}		V _{DD} = 3V, 32kHz crystal oscillation (C ₁ = C ₂ = 47pF)		45	130	μA
	I _{DDS1}		SLEEP mode		2.3	10	mA
			V _{DD} = 5.5V, 10MHz crystal oscillation (C ₁ = C ₂ = 15pF)				
	I _{DDS2}		V _{DD} = 3V, 32kHz crystal oscillation (C ₁ = C ₂ = 47pF)		11	30	μA
I _{DDS3}	STOP mode V _{DD} = 5.5V, termination of 10MHz and 32kHz oscillation				30	μA	
Input capacity	C _{IN}	PA to AC, PE0 to 5, XTAL, EXTAL, TEX, $\overline{\text{RST}}$	Clock 1MHz 0V for all pins excluding measured pins		10	20	pF

*1) PA to PC pins specify the input current when pull-up resistance has been selected; leakage current when no resistance has been selected.

*2) When all pins are open.

AC Characteristics

(1) Clock timing

(Ta = -10 to +75°C, VDD = 4.5 to 5.5V, VSS = 0V reference)

Item	Symbol	Pin	Conditions	Min.	Typ.	Max.	Unit
System clock frequency	fc	XTAL EXTAL	Fig. 1, Fig. 2	1		10	MHz
System clock input pulse width	tXL tXH	EXTAL	Fig. 1, Fig. 2 External clock drive	37.5			ns
System clock input rise time, fall time	tCR tCF	EXTAL	Fig. 1, Fig. 2 External clock drive	tsys + 50*1		200	ns
Event count input clock pulse width	tEH tEL	EC0, EC1	Fig. 3				ns
Event count input clock rise time, fall time	tER tEF	EC0, EC1	Fig. 3			20	ms
System clock frequency	fc	TEX TX	VDD = 2.7 to 5.5V Fig. 2 (32kHz clock applied condition)		32.768		kHz
Event count input pulse width	tTL tTH	TEX	Fig. 3	10			µs
Event count input rise time, fall time	tTR tTF	TEX	Fig. 3			20	ms

*1) tsys indicates the three values below according to the upper two bits (CPU clock selection) of the control clock register (CLC: 00FEH).

tsys (ns)=2000/fc (upper two bits="00"), 4000/fc (upper two bits="01"), 16000/fc (upper two bits="11")

Fig. 1. Clock timing

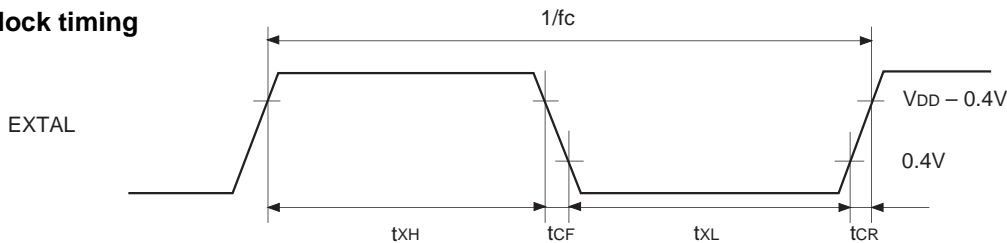


Fig. 2. Clock applied conditions

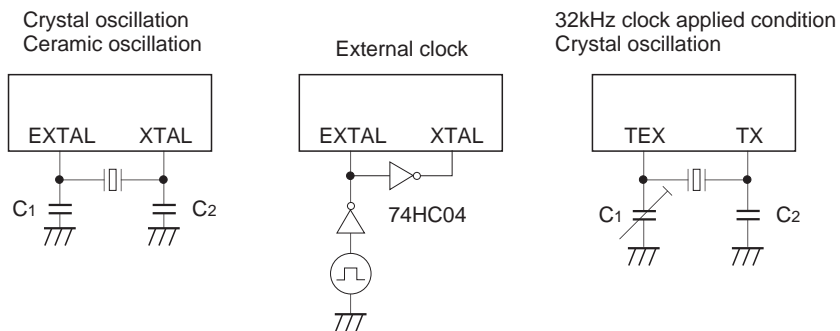
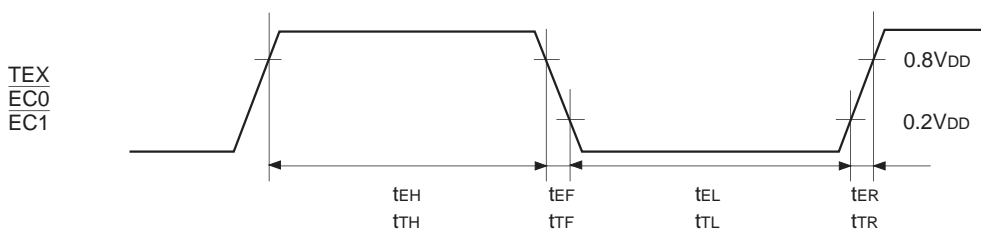


Fig. 3. Event count clock timing



(2) Serial transfer (CH0)

(Ta = -10 to +75°C, V_{DD} = 4.5 to 5.5V, V_{SS} = 0V reference)

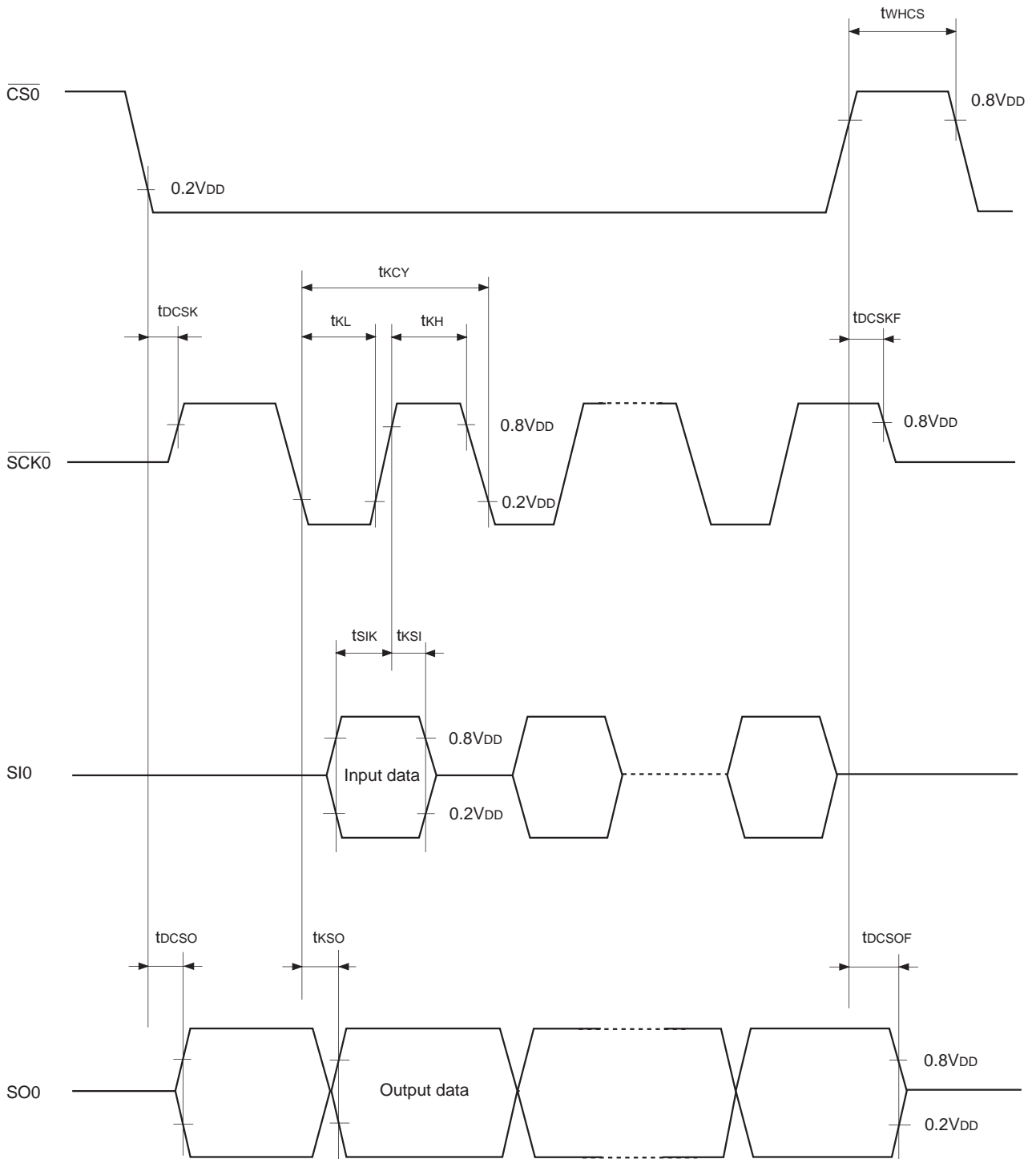
Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{\text{CS0}} \downarrow \rightarrow \overline{\text{SCK0}}$ delay time	t _{DCSK}	$\overline{\text{SCK0}}$	Chip select transfer mode ($\overline{\text{SCK0}}$ = output mode)		t _{sys} + 200	ns
$\overline{\text{CS0}} \uparrow \rightarrow \overline{\text{SCK0}}$ float delay time	t _{DCSKF}	$\overline{\text{SCK0}}$	Chip select transfer mode ($\overline{\text{SCK0}}$ = output mode)		t _{sys} + 200	ns
$\overline{\text{CS0}} \downarrow \rightarrow \text{SO0}$ delay time	t _{DCSO}	SO0	Chip select transfer mode		t _{sys} + 200	ns
$\overline{\text{CS0}} \uparrow \rightarrow \text{SO0}$ float delay time	t _{DCSOF}	SO0	Chip select transfer mode		t _{sys} + 200	ns
$\overline{\text{CS0}}$ High level width	t _{WHCS}	$\overline{\text{CS0}}$	Chip select transfer mode	t _{sys} + 200		ns
$\overline{\text{SCK0}}$ cycle time	t _{KCY}	$\overline{\text{SCK0}}$	Input mode	2t _{sys} + 200		ns
			Output mode	16000/fc		ns
$\overline{\text{SCK0}}$ High, Low level width	t _{KH} t _{KL}	$\overline{\text{SCK0}}$	Input mode	t _{sys} + 100		ns
			Output mode	8000/fc-50		ns
SI0 input set-up time (for $\overline{\text{SCK0}} \uparrow$)	t _{SIK}	SI0	$\overline{\text{SCK0}}$ input mode	100		ns
			$\overline{\text{SCK0}}$ output mode	200		ns
SI0 input hold time (for $\overline{\text{SCK0}} \uparrow$)	t _{KSI}	SI0	$\overline{\text{SCK0}}$ input mode	t _{sys} + 200		ns
			$\overline{\text{SCK0}}$ output mode	100		ns
$\overline{\text{SCK0}} \downarrow \rightarrow \text{SO0}$ delay time	t _{KSO}	SO0	$\overline{\text{SCK0}}$ input mode		t _{sys} + 200	ns
			$\overline{\text{SCK0}}$ output mode		100	ns

Note 1) t_{sys} indicates the three values below according to the upper two bits (CPU clock selection) of the control clock register (CLC: 00FEH).

t_{sys} (ns)=2000/fc (upper two bits="00"), 4000/fc (upper two bits="01"), 16000/fc (upper two bits="11")

Note 2) The load condition for the $\overline{\text{SCK0}}$ output mode, SO0 output delay time is 50pF + 1TTL.

Fig. 4. Serial transfer CH0 timing



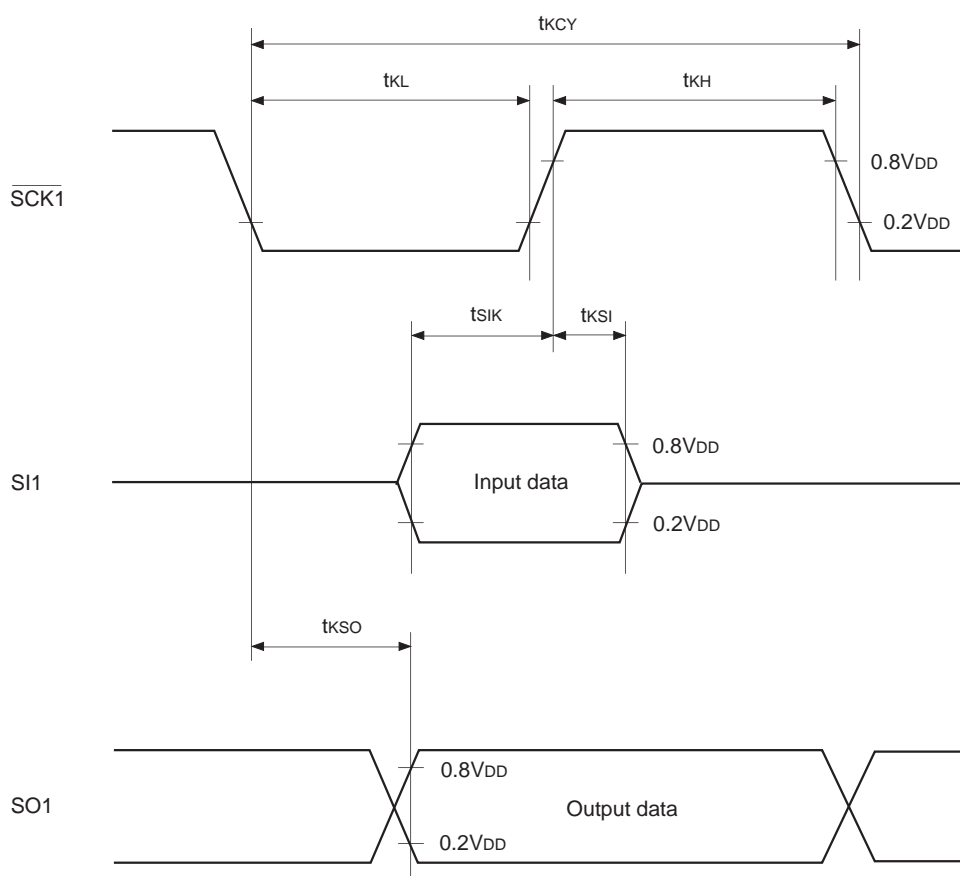
Serial transfer (CH1)

($T_a = -10$ to $+75^\circ\text{C}$, $V_{DD} = 4.5$ to 5.5V , $V_{SS} = 0\text{V}$ reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{\text{SCK1}}$ cycle time	t_{KCY}	$\overline{\text{SCK1}}$	Input mode	1000		ns
			Ouput mode	$16000/f_c$		ns
$\overline{\text{SCK1}}$ High, Low level width	t_{KH} t_{KL}	$\overline{\text{SCK1}}$	Input mode	400		ns
			Ouput mode	$8000/f_c - 50$		ns
SI1 input set-up time (for $\overline{\text{SCK1}} \uparrow$)	t_{SIK}	SI1	$\overline{\text{SCK1}}$ input mode	100		ns
			$\overline{\text{SCK1}}$ ouput mode	200		ns
SI1 input hold time (for $\overline{\text{SCK1}} \uparrow$)	t_{KSI}	SI1	$\overline{\text{SCK1}}$ input mode	200		ns
			$\overline{\text{SCK1}}$ ouput mode	100		ns
$\overline{\text{SCK1}} \downarrow \rightarrow \text{SO1}$ delay time	t_{KSO}	SO1	$\overline{\text{SCK1}}$ input mode		200	ns
			$\overline{\text{SCK1}}$ ouput mode		100	ns

Note) The load condition for the $\overline{\text{SCK1}}$ output mode, SO1 output delay time is $50\text{pF} + 1\text{TTL}$.

Fig. 5. Serial transfer CH1 timing

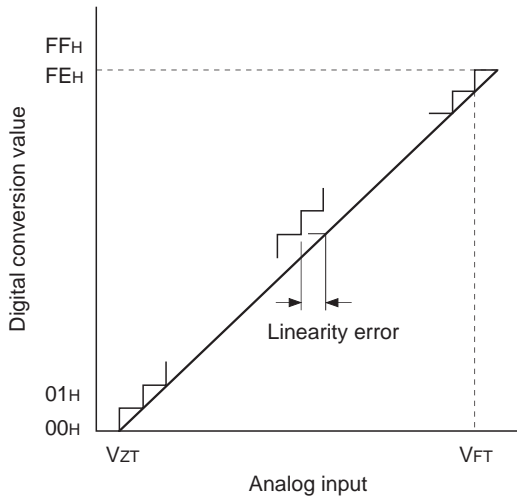


(3) A/D converter characteristics

($T_a = -10$ to $+75^\circ\text{C}$, $V_{DD} = 4.5$ to 5.5V , $AV_{REF} = 4.0$ to V_{DD} , $V_{SS} = AV_{SS} = 0\text{V}$ reference)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error						± 3	LSB
Zero transition voltage	V_{ZT}^{*1}		$T_a = 25^\circ\text{C}$ $V_{DD} = AV_{REF} = 5.0\text{V}$ $V_{SS} = AV_{SS} = 0\text{V}$	-50	10	70	mV
Full-scale transition voltage	V_{FT}^{*2}			4910	4970	5030	mV
Conversion time	t_{CONV}			$160/f_{ADC}^{*3}$			μs
Sampling time	t_{SAMP}			$12/f_{ADC}^{*3}$			μs
Reference input voltage	V_{REF}	AV_{REF}		$V_{DD} - 0.5$		V_{DD}	V
Analog input voltage	V_{IAN}	$AN0$ to $AN7$		0		AV_{REF}	V
AV_{REF} current	I_{REF}	AV_{REF}	Operation mode		0.6	1.0	mA
	I_{REFS}		SLEEP mode STOP mode 32kHz operation mode			10	μA

Fig. 6. Definition of A/D converter terms



- *1) V_{ZT} : Value at which the digital transfer value changes from 00H to 01H and vice versa.
- *2) V_{FT} : Value at which the digital transfer value changes from FEH to FFH and vice versa.
- *3) f_{ADC} indicates the below values due to the contents of bit 6 (CKS) of the A/D control register (ADC: 00F9H) and bits 7 (PCK1) and 6 (PCK0) of the clock control register (CLC: 00FEH).

PCK1, PCK0	CKS	
	0 ($\phi/2$ selection)	1 (ϕ selection)
00 ($\phi = f_{EX}/2$)	$f_{ADC} = f_c/2$	$f_{ADC} = f_c$
01 ($\phi = f_{EX}/4$)	$f_{ADC} = f_c/4$	$f_{ADC} = f_c/2$
11 ($\phi = f_{EX}/16$)	$f_{ADC} = f_c/16$	$f_{ADC} = f_c/8$

(4) Interruption, reset input (Ta = -10 to +75°C, VDD = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
External interruption High, Low level width	t _{iH} t _{iL}	INT0 INT1 INT2 $\overline{\text{NMI/INT3}}$		1		μs
Reset input Low level width	t _{rSL}	$\overline{\text{RST}}$		32/fc		μs

Fig. 7. Interruption input timing

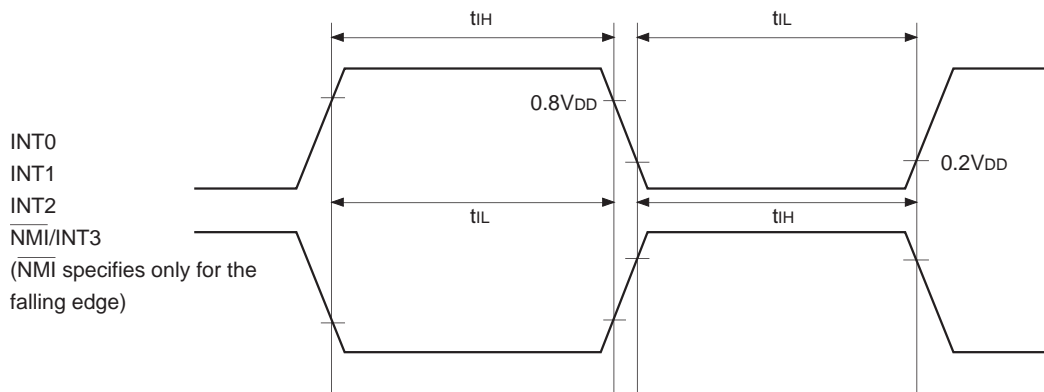
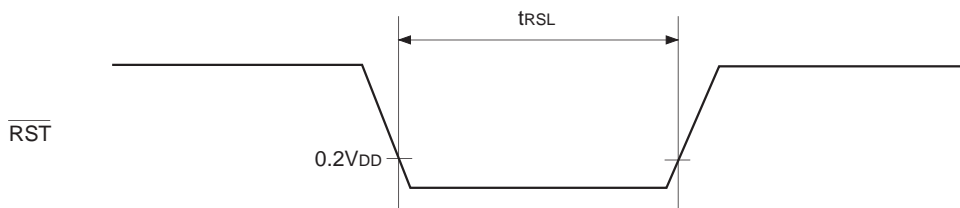
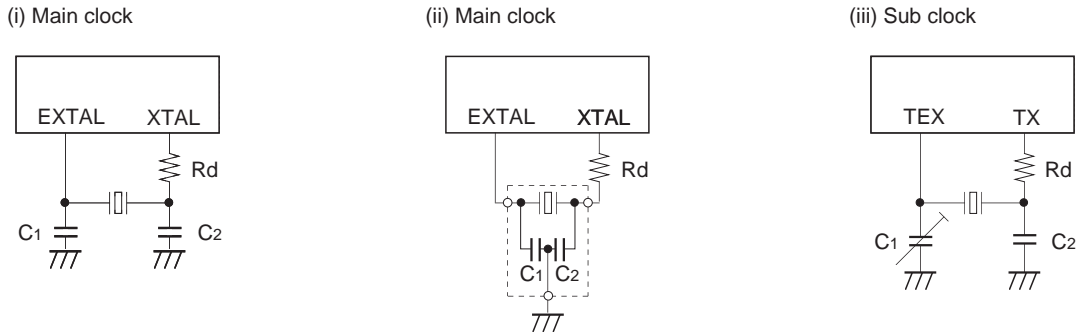


Fig. 8. $\overline{\text{RST}}$ input timing



Appendix

Fig. 9. Recommended oscillation circuit



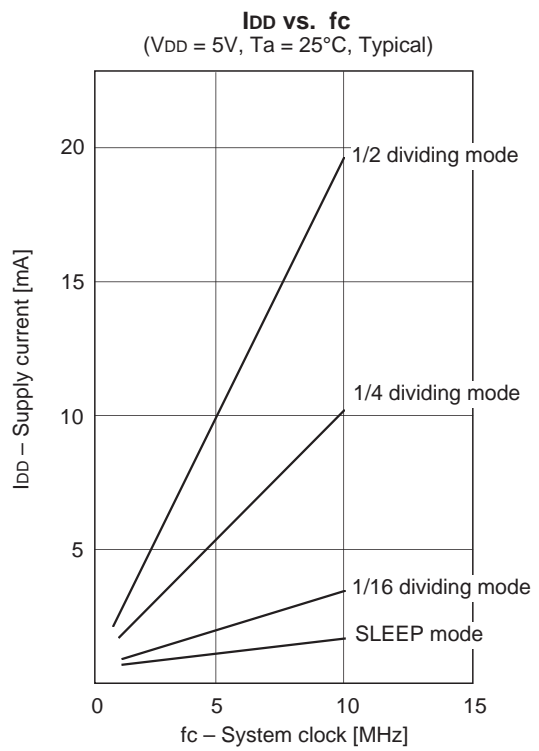
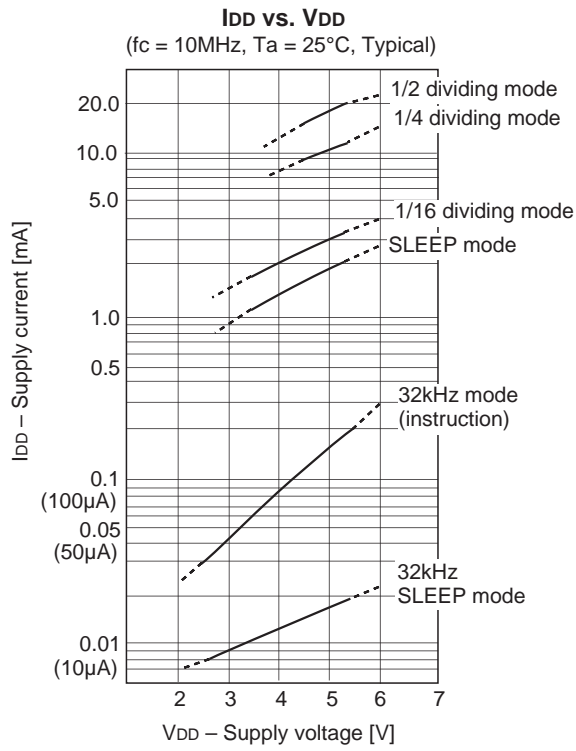
Manufacturer	Model	fc (MHz)	C ₁ (pF)	C ₂ (pF)	Rd (Ω)	Circuit example
MURATA MFG CO., LTD.	CSA4.19MG	4.19	30	30	0	(i)
	CSA8.00MTZ	8.00				
	CSA10.0MTZ	10.00				
	CST4.19MGW*	4.19				(ii)
	CST8.00MTW*	8.00				
	CST10.0MTW*	10.00				
RIVER ELETEC CO., LTD	HC-49/U03	4.19	12	12	0	(i)
		8.00				
		10.00				
KINSEKI LTD.	HC-49/U (-S)	4.19	27	27	0	
		8.00				
		10.00	20	20		
	P3	32.768kHz	50	22		1M

Models marked with an asterisk (*) have the built-in ground capacitance (C₁, C₂).

Mask option table

Option item	Product				
	Mask product				PROM version
	CXP82832	CXP82840	CXP82852	CXP82860	CXP828P60Q-1-□□□
Package	80-pin plastic QFP				80-pin plastic QFP
ROM capacitance	32K bytes	40K bytes	52K bytes	60K bytes	PROM 60K bytes
Reset pull-up resistance	Existent/Non-existent				Existent
High voltage drive pin pull-down resistor	Existent/Non-existent				Non-existent (PD7/A24 to PD0/A55) Existent (G0/A0 to A23)

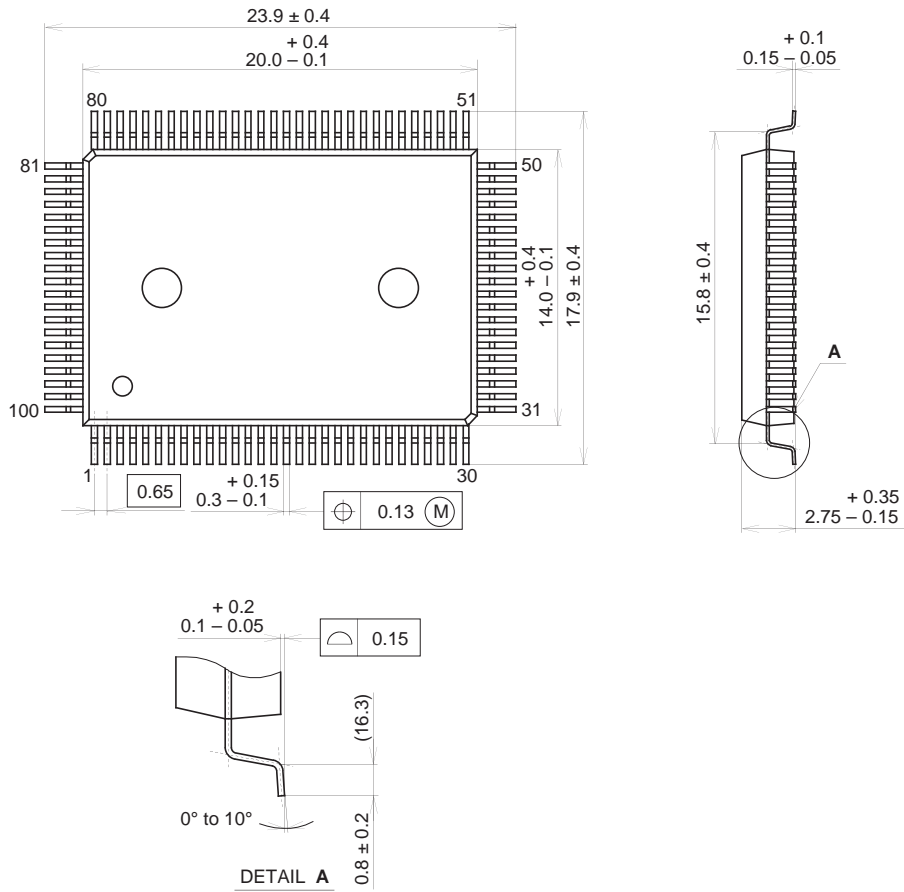
Characteristics Curve



Package Outline

Unit : mm

100PIN QFP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	QFP-100P-L01
EIAJ CODE	QFP100-P-1420
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.7g