

CMOS 8-bit Single Chip Microcomputer

Description

The CXP83508/83512/83516 and the CXP83509/83513/83517 are CMOS 8-bit single chip microcomputer integrating on a single chip an A/D converter, serial interface, timer/counter, time-base timer, sub timer/counter, LCD controller/driver and remote control reception circuit besides the basic configurations of 8-bit CPU, ROM, RAM, and I/O port.

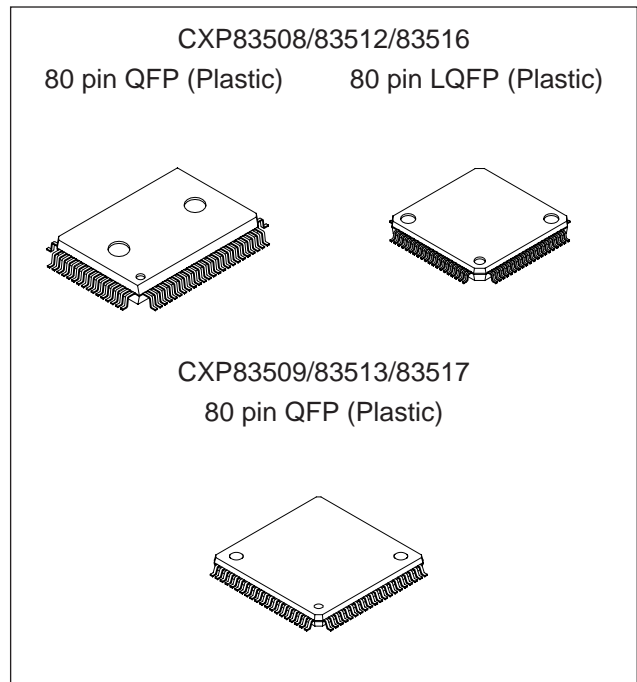
The CXP83508/83512/83516 and the CXP83509/83513/83517 also provide a sleep/stop function that enables lower power consumption.

Features

- Wide-range instruction system (213 instructions) to cover various types of data.
 - 16-bit arithmetic/multiplication and division/boolean bit operation instructions
- Minimum instruction cycle
 - 400ns at 10MHz operation (4.5 to 5.5V)
 - 1 μ s at 4MHz operation (2.7 to 5.5V)
 - 122 μ s at 32kHz operation (2.7 to 5.5V)
- Incorporated ROM capacity
 - 8K bytes (CXP83508, 83509)
 - 12K bytes (CXP83512, 83513)
 - 16K bytes (CXP83516, 83517)
- Incorporated RAM capacity
 - 608bytes (includes LCD display data area and serial interface RAM)
- Peripheral functions
 - A/D converter
 - 8-bit, 8-channel, successive approximation method (Conversion time of 12.4 μ s/10MHz)
 - Serial interface
 - Incorporated buffer RAM (Auto transfer for 1 to 32 bytes), 1 channel
 - 8-bit clock synchronized type (MSB/LSB first selectable), 1 channel
 - Timer
 - 8-bit timer, 8-bit timer/counter, 19-bit time-base timer, Sub timer/counter
 - LCD controller/driver
 - Maximum 128 segment display possible (during 1/4 duty)
 - 4 common output, 32 segment output
 - Display method static, 1/2, 1/3, 1/4 duty
 - Bias method 1/2, 1/3 bias
 - Remote control reception circuit
 - 8-bit pulse measuring counter, 6-stage FIFO
- Interruption
 - 14 factors, 14 vectors, multi-interruption possible
- Standby mode
- Package
 - 80-pin plastic QFP/LQFP
- Piggy/evaluation chip
 - CXP83600 (CXP83508, 83512, 83516)
 - CXP83601 (CXP83509, 83513, 83517)

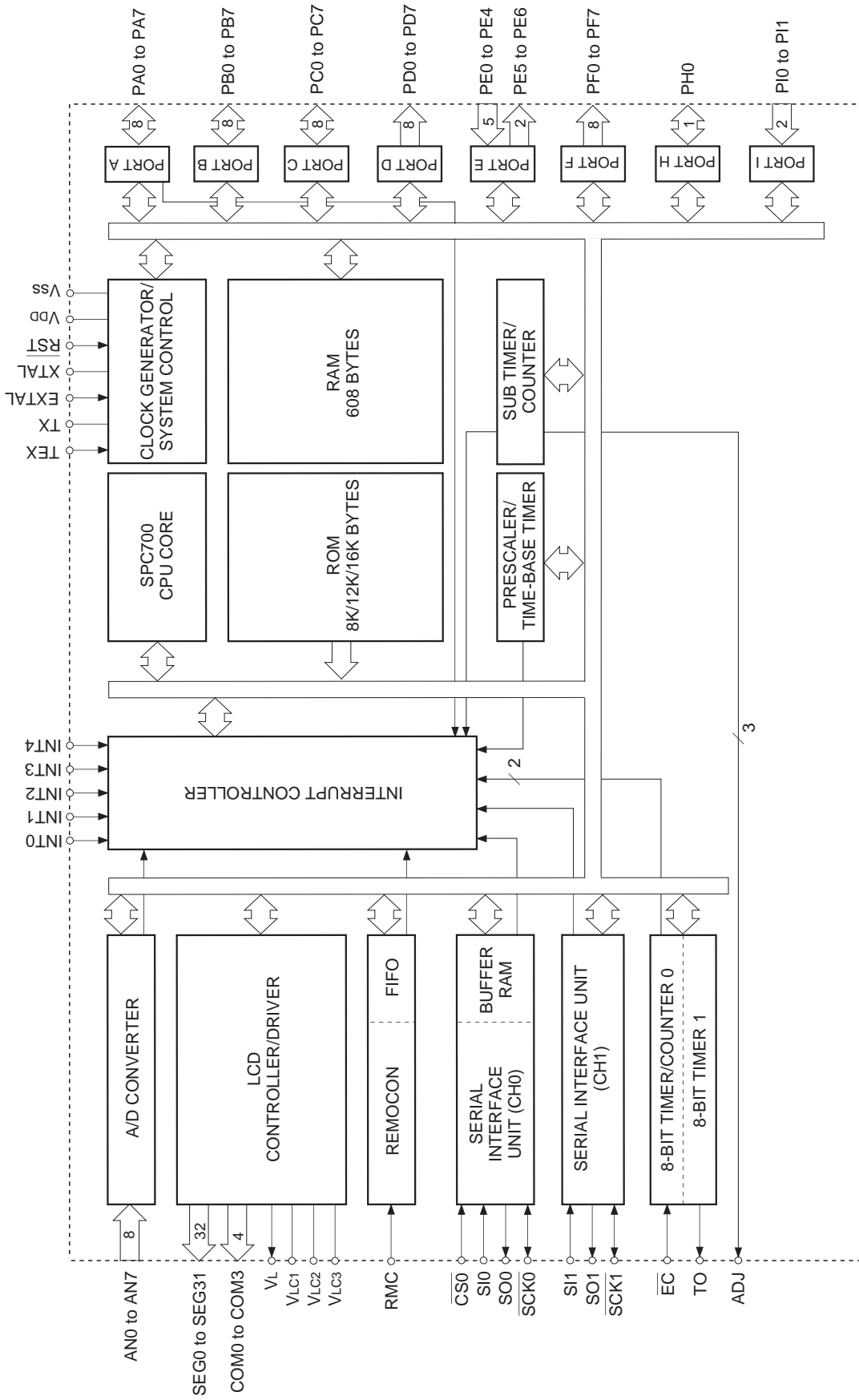
Structure

Silicon gate CMOS IC

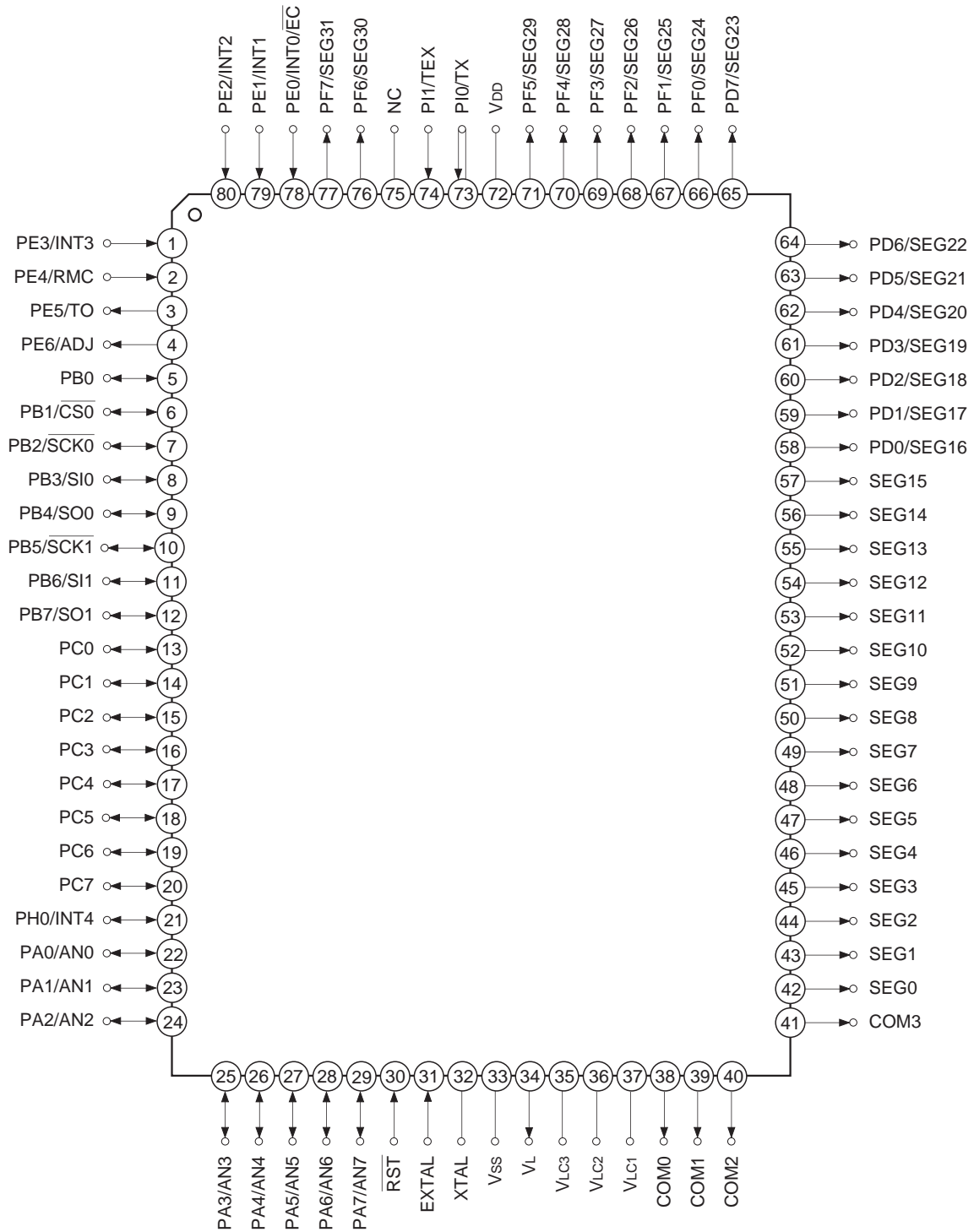


Sony reserves the right to change products and specifications without prior notice. This information does not convey any license by any implication or otherwise under any patents or other right. Application circuits shown, if any, are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits.

Block Diagram

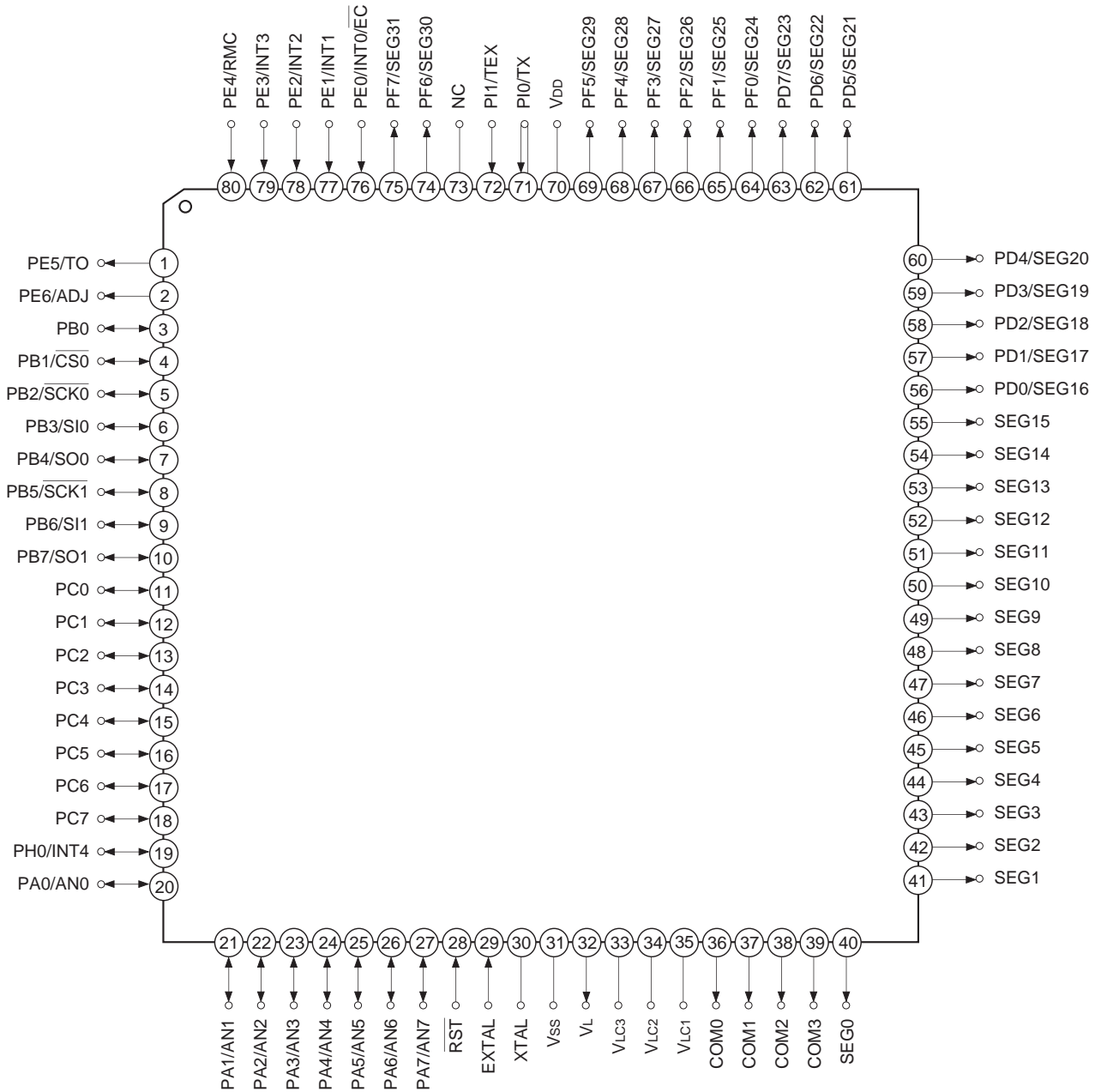


Pin Assignment (Top View) CXP83508/83512/83516 (QFP package)



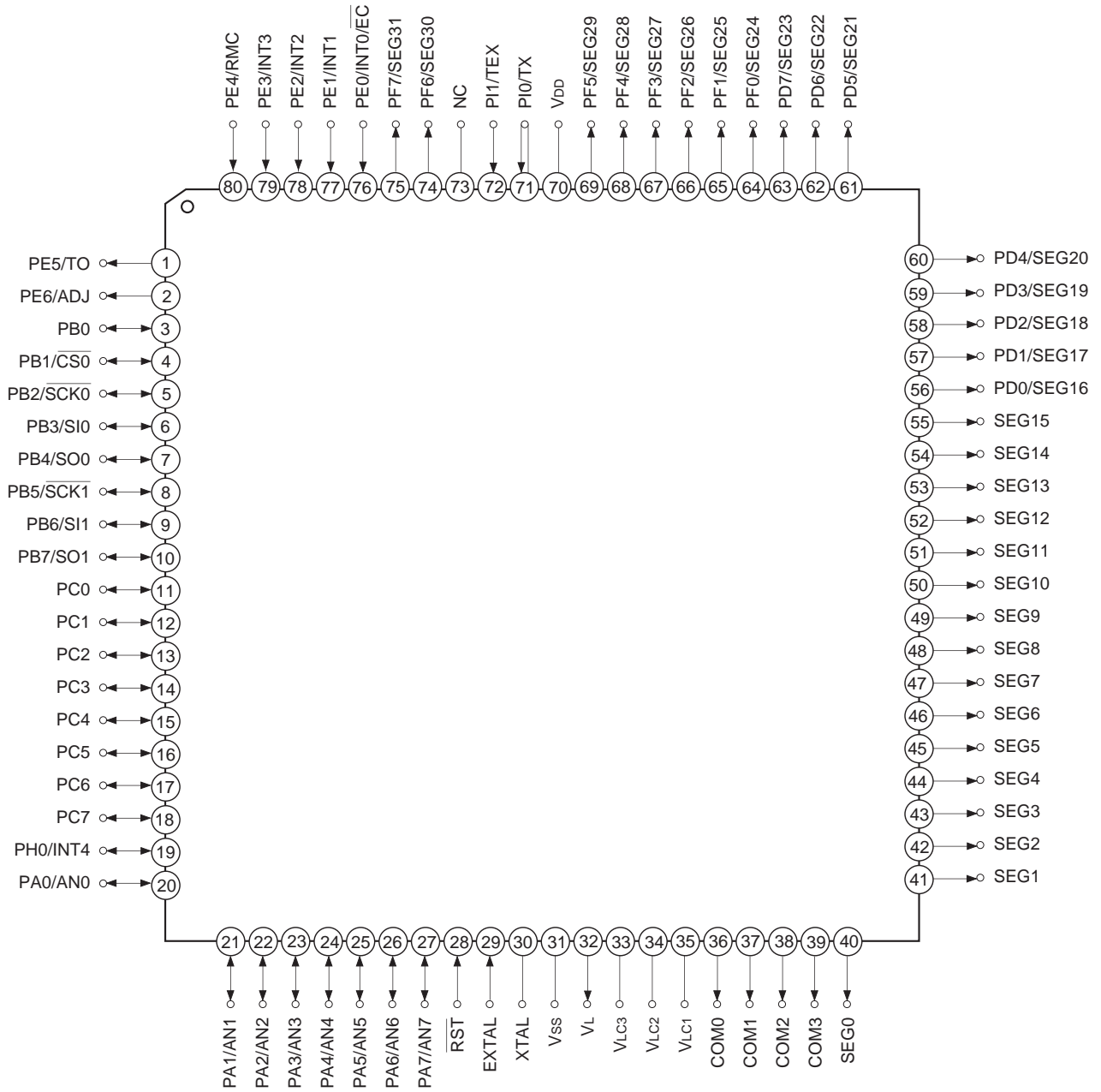
Note Do not make any connections to NC (Pin 75).

Pin Assignment (Top View) CXP83508/83512/83516 (LQFP package)



Note) Do not make any connections to NC (Pin 73).

Pin Assignment (Top View) CXP83509/83513/83517 (QFP package)



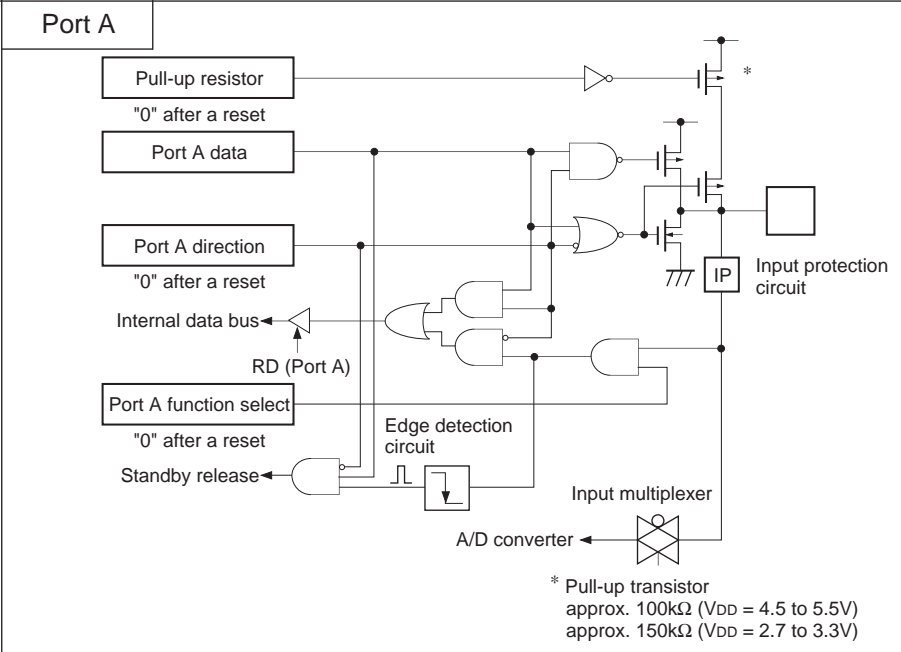
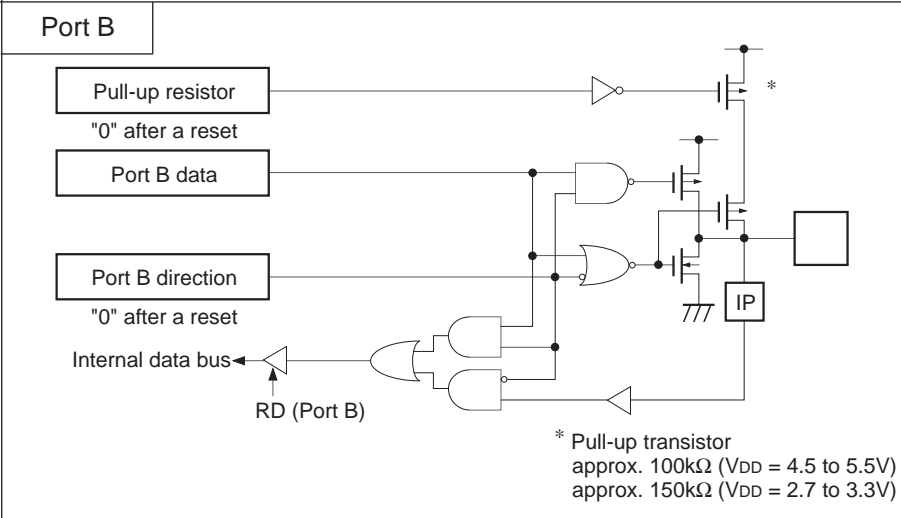
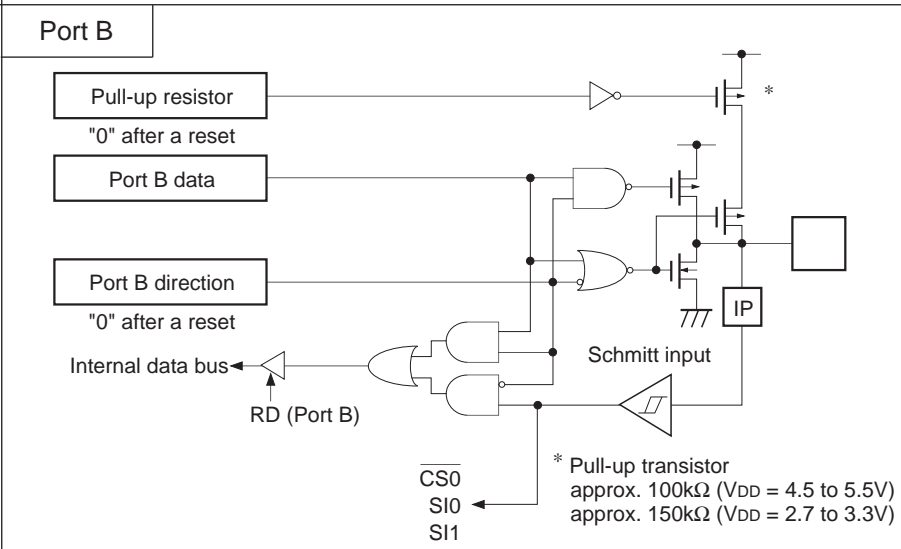
Note) Do not make any connections to NC (Pin 73).

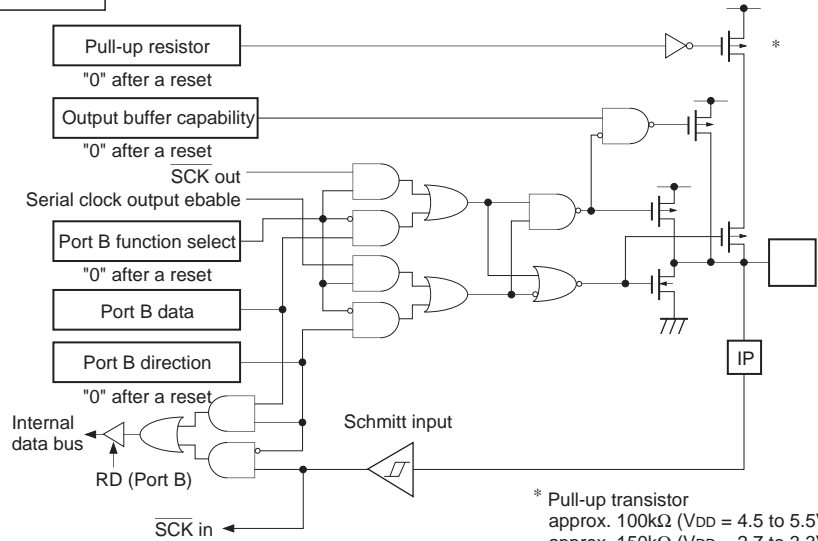
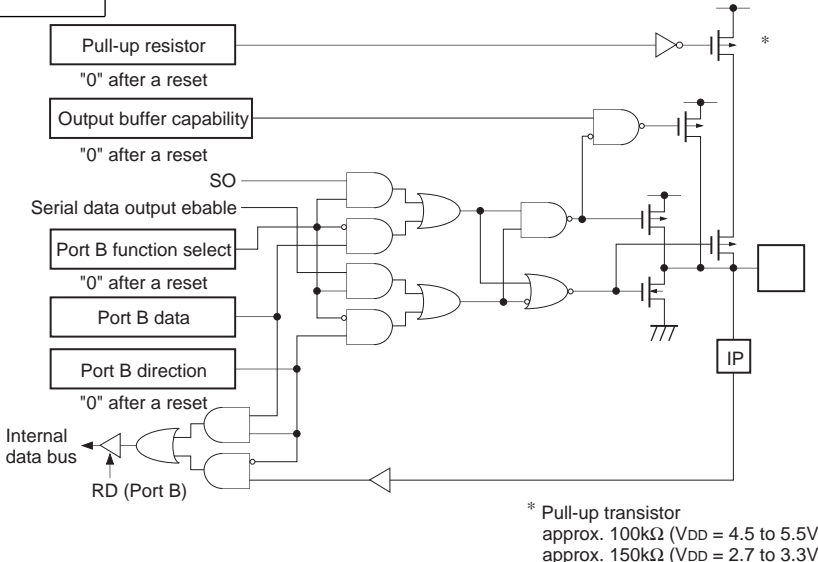
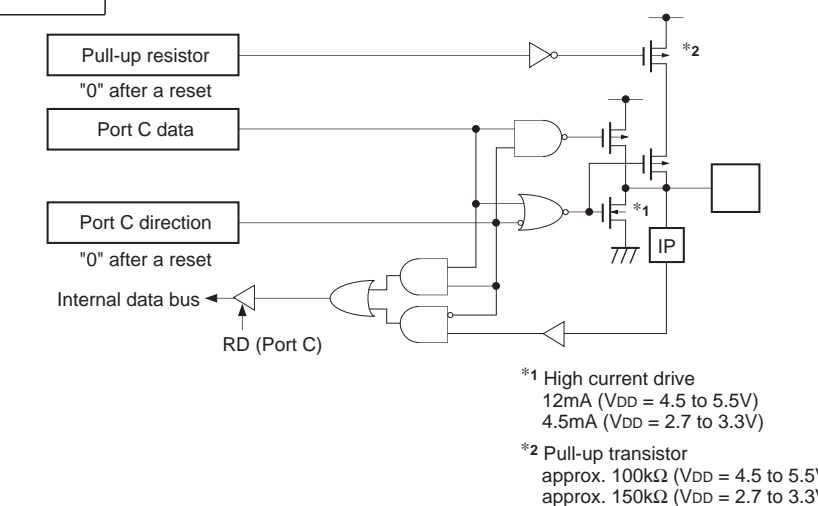
Pin Description

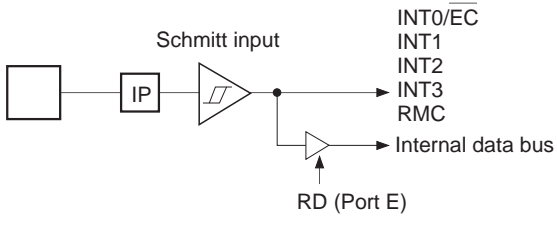
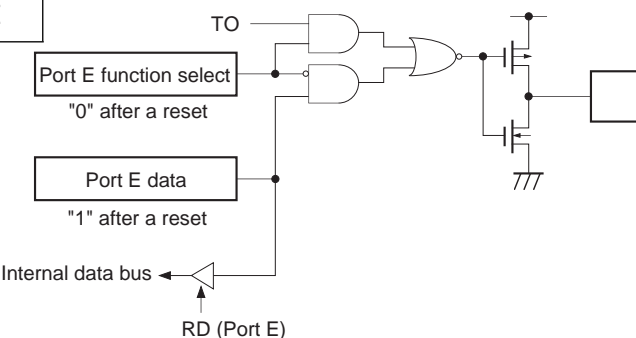
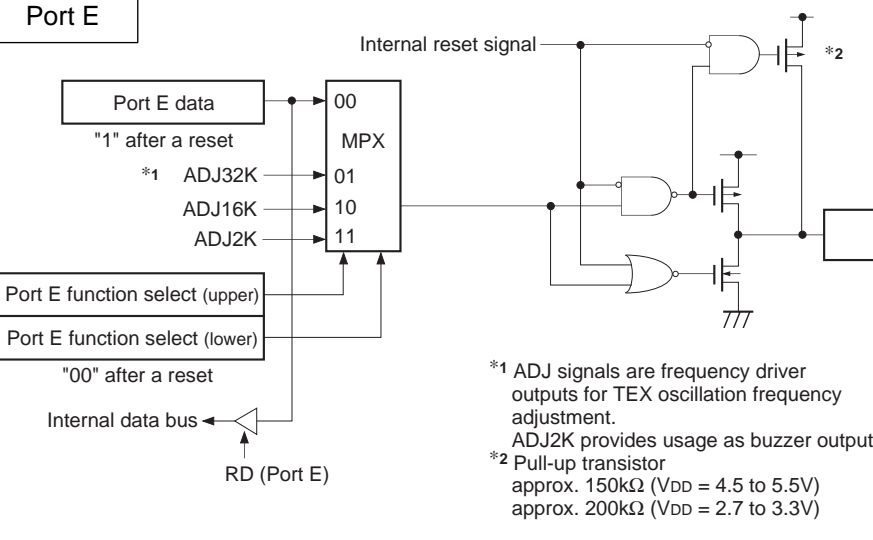
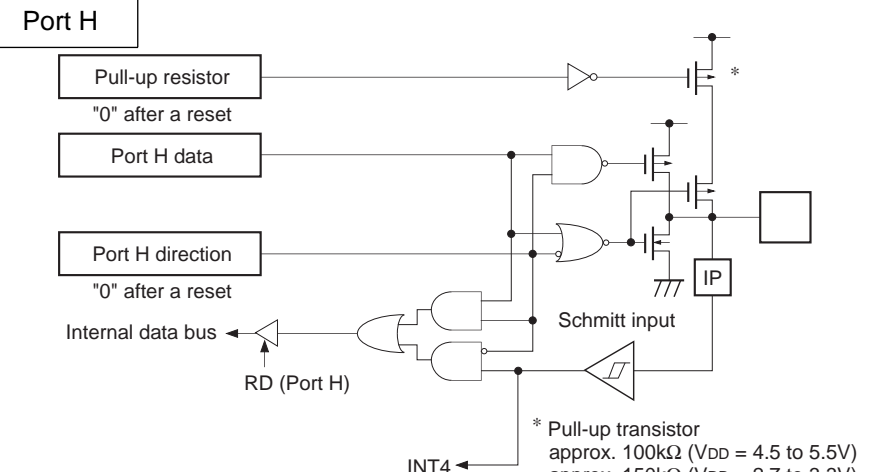
Symbol	I/O	Functions	
PA0/AN0 to PA7/AN7	I/O/Analog input	(Port A) 8-bit I/O port. I/O can be set in a bit unit. Standby release input can be set in a bit unit. Incorporation of pull-up resistor can be set through the program in a bit unit. (8 pins)	Analog inputs to A/D converter. (8 pins)
PB0	I/O	(Port B) 8-bit I/O port. I/O can be set in a bit unit. Incorporation of pull-up resistor can be set through the program in a bit unit. (8 pins)	Chip select input for serial interface (CH0).
PB1/ $\overline{CS0}$	I/O/Input		Serial clock I/O (CH0).
PB2/ $\overline{SCK0}$	I/O/I/O		Serial data input (CH0).
PB3/SI0	I/O/Input		Serial data output (CH0).
PB4/SO0	I/O/Output		Serial clock I/O (CH1).
PB5/ $\overline{SCK1}$	I/O/I/O		Serial data input (CH1).
PB6/SI1	I/O/Input		Serial data output (CH1).
PB7/SO1	I/O/Output		
PC0 to PC7	I/O	(Port C) 8-bit I/O port. I/O can be set in a bit unit. Capable of driving 12mA sink current. Incorporation of pull-up resistor can be set through the program in a bit unit. (8 pins)	
PE0/INT0/ \overline{EC}	Input/Input/Input	(Port E) 7-bit port. Lower 5 bits are for inputs; upper 2 bits are for outputs. (7 pins)	External event inputs for 8-bit timer/counter.
PE1/INT1	Input/Input		External interruption request inputs. (4 pins)
PE2/INT2	Input/Input		Remote control reception circuit input.
PE3/INT3	Input/Input		Output for 8-bit timer/counter rectangular wave.
PE4/RMC	Input/Input		Output for TEX oscillation frequency division.
PE5/TO	Output/Output		
PE6/ADJ	Output/Output		
PH0/INT4	I/O/Input	(Port H) 1-bit I/O port. Incorporation of pull-up resistor can be set through the program. (1 pin)	External interruption request input. (1 pin)
PI0/TX	Input	(Port I) 2-bit input port. (2 pins)	Crystal connectors for sub timer/counter clock oscillation. For usage as event counter, input to TEX, and leave TX open.
PI1/TEX	Input/Input		

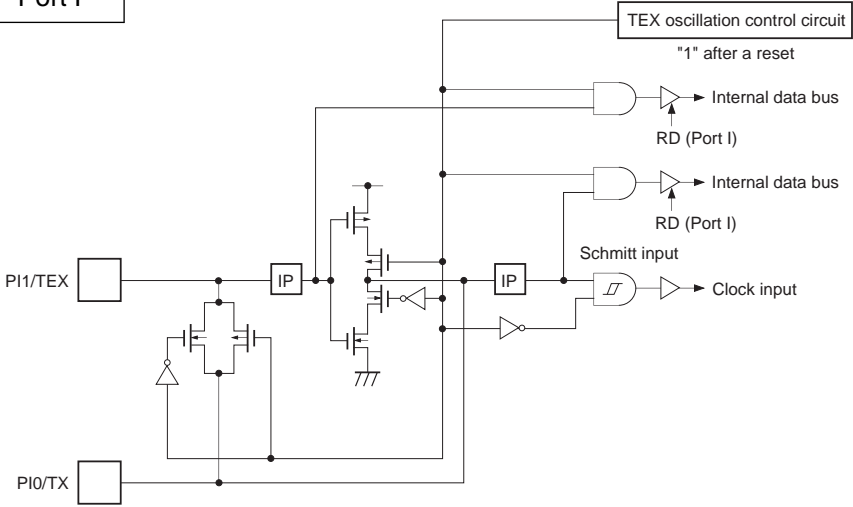
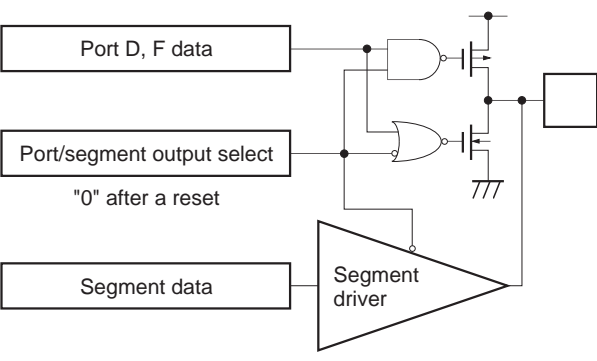
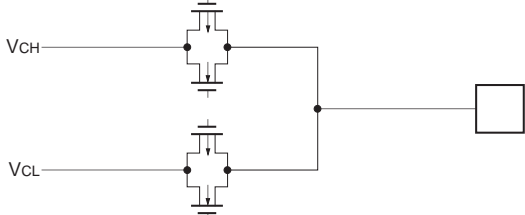
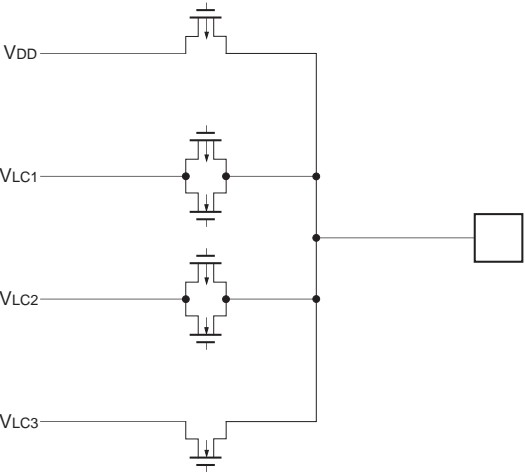
Symbol	I/O	Functions	
PD0/SEG16 to PD7/SEG23	Output/Output	(Port D) 8-bit output port. (8 pins)	LCD segment signal outputs. (16 pins)
PF0/SEG24 to PF7/SEG31	Output/Output	(Port F) 8-bit output port. (8 pins)	
SEG0 to SEG15	Output	LCD segment signal output. (16 pins)	
COM0 to COM3	Output	LCD common signal output. (4 pins)	
V _{Lc1} to V _{Lc3}		LCD bias power supply. (3 pins)	
V _L	Output	Control pin to cut off the current flowing to external LCD bias resistor during standby.	
EXTAL	Input	Crystal connectors for system clock oscillation. When the clock is supplied externally, input to EXTAL; opposite phase clock should be input to XTAL.	
XTAL			
$\overline{\text{RST}}$	Input	Low-level active system reset.	
NC		NC. Do not make any connections to NC.	
V _{DD}		Positive power supply.	
V _{SS}		GND.	

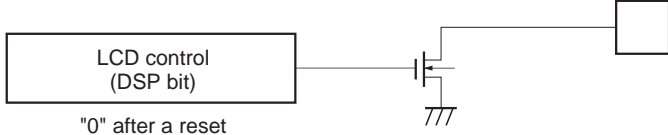
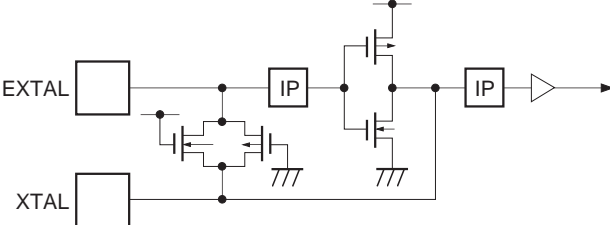
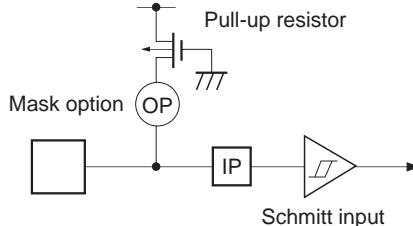
I/O Circuit Format for Pins

Pin	Circuit format	After a reset
<p>PA0/AN0 to PA7/AN7</p> <p>8 pins</p>	<p>Port A</p>  <p>* Pull-up transistor approx. 100kΩ (V_{DD} = 4.5 to 5.5V) approx. 150kΩ (V_{DD} = 2.7 to 3.3V)</p>	<p>Hi-Z</p>
<p>PB0</p> <p>1 pin</p>	<p>Port B</p>  <p>* Pull-up transistor approx. 100kΩ (V_{DD} = 4.5 to 5.5V) approx. 150kΩ (V_{DD} = 2.7 to 3.3V)</p>	<p>Hi-Z</p>
<p>PB1/$\overline{\text{CS0}}$ PB3/SI0 PB6/SI1</p> <p>3 pins</p>	<p>Port B</p>  <p>* Pull-up transistor approx. 100kΩ (V_{DD} = 4.5 to 5.5V) approx. 150kΩ (V_{DD} = 2.7 to 3.3V)</p> <p>$\overline{\text{CS0}}$ SI0 SI1</p>	<p>Hi-Z</p>

Pin	Circuit format	After a reset
<p>PB2/$\overline{\text{SCK0}}$ PB5/$\overline{\text{SCK1}}$</p> <p>2 pins</p>	<p>Port B</p>  <p>* Pull-up transistor approx. 100kΩ (V_{DD} = 4.5 to 5.5V) approx. 150kΩ (V_{DD} = 2.7 to 3.3V)</p>	<p>Hi-Z</p>
<p>PB4/SO0 PB7/SO1</p> <p>2 pins</p>	<p>Port B</p>  <p>* Pull-up transistor approx. 100kΩ (V_{DD} = 4.5 to 5.5V) approx. 150kΩ (V_{DD} = 2.7 to 3.3V)</p>	<p>Hi-Z</p>
<p>PC0 to PC7</p> <p>8 pins</p>	<p>Port C</p>  <p>*1 High current drive 12mA (V_{DD} = 4.5 to 5.5V) 4.5mA (V_{DD} = 2.7 to 3.3V)</p> <p>*2 Pull-up transistor approx. 100kΩ (V_{DD} = 4.5 to 5.5V) approx. 150kΩ (V_{DD} = 2.7 to 3.3V)</p>	<p>Hi-Z</p>

Pin	Circuit format	After a reset
<p>PE0/INT0/\overline{EC} PE1/INT1 PE2/INT2 PE3/INT3 PE4/RMC</p> <p>5 pins</p>	<p>Port E</p>  <p>INT0/\overline{EC} INT1 INT2 INT3 RMC</p> <p>Internal data bus</p> <p>RD (Port E)</p>	<p>Hi-Z</p>
<p>PE5/TO</p> <p>1 pin</p>	<p>Port E</p>  <p>TO</p> <p>Port E function select "0" after a reset</p> <p>Port E data "1" after a reset</p> <p>Internal data bus</p> <p>RD (Port E)</p>	<p>High level</p>
<p>PE6/ADJ</p> <p>1 pin</p>	<p>Port E</p>  <p>Internal reset signal</p> <p>Port E data "1" after a reset *1 ADJ32K ADJ16K ADJ2K</p> <p>MPX 00 01 10 11</p> <p>Port E function select (upper) Port E function select (lower) "00" after a reset</p> <p>Internal data bus</p> <p>RD (Port E)</p> <p>*2</p> <p>*1 ADJ signals are frequency driver outputs for TEX oscillation frequency adjustment. ADJ2K provides usage as buzzer output. *2 Pull-up transistor approx. 150kΩ ($V_{DD} = 4.5$ to $5.5V$) approx. 200kΩ ($V_{DD} = 2.7$ to $3.3V$)</p>	<p>High level High level at ON resistance of pull-up transistor during a reset.</p>
<p>PH0/INT4</p> <p>1 pin</p>	<p>Port H</p>  <p>Pull-up resistor "0" after a reset</p> <p>Port H data</p> <p>Port H direction "0" after a reset</p> <p>Internal data bus</p> <p>RD (Port H)</p> <p>Schmitt input</p> <p>INT4</p> <p>* Pull-up transistor approx. 100kΩ ($V_{DD} = 4.5$ to $5.5V$) approx. 150kΩ ($V_{DD} = 2.7$ to $3.3V$)</p>	<p>Hi-Z</p>

Pin	Circuit format		After a reset
<p>PI0/TX PI1/TEX</p> <p>2 pins</p>	<p>Port I</p>		<p>Oscillation halted port input</p>
<p>PD0/SEG16 to PD7/SEG23 PF0/SEG24 to PF7/SEG31</p> <p>16 pins</p>	<p>Port D Port F</p>		<p>Segment output (V_{DD} level)</p>
<p>SEG0 to SEG15</p> <p>16 pins</p>	<p>Segment</p>		<p>V_{DD} level</p>
<p>COM0 to COM3</p> <p>4 pins</p>	<p>Common</p>		<p>V_{DD} level</p>

Pin	Circuit format	After a reset
<p>V_L</p> <p>1 pin</p>	 <p>LCD control (DSP bit)</p> <p>"0" after a reset</p>	<p>Hi-Z</p>
<p>EXTAL</p> <p>XTAL</p> <p>2 pins</p>	 <ul style="list-style-type: none"> • Diagram shows circuit composition during oscillation. • Feedback resistor is removed during stop. XTAL becomes high level. 	<p>Oscillation</p>
<p>$\overline{\text{RST}}$</p> <p>1 pin</p>	 <p>Pull-up resistor</p> <p>Mask option</p> <p>Schmitt input</p>	<p>Low level (during a reset)</p>

Absolute Maximum Ratings

(V_{SS} = 0V)

Item	Symbol	Rating	Unit	Remarks
Supply voltage	V _{DD}	-0.3 to +7.0	V	
LCD bias voltage	V _{LC1} , V _{LC2} , V _{LC3}	-0.3 to +7.0*1	V	
Input voltage	V _{IN}	-0.3 to +7.0*1	V	
Output voltage	V _{OUT}	-0.3 to +7.0*1	V	
High level output current	I _{OH}	-5	mA	Output per pin
High level total output current	ΣI _{OH}	-50	mA	Total for all output pins
Low level output current	I _{OL}	15	mA	Value per pin, excluding high current output pins
	I _{OLC}	20	mA	Value per pin for high current output pins*2
Low level total output current	ΣI _{OL}	100	mA	Total for all output pins
Operating temperature	T _{opr}	-20 to +75	°C	
Storage temperature	T _{stg}	-55 to +150	°C	
Allowable power dissipation	P _D	600	mW	QFP-80P-L01
		380	mW	LQFP-80P-L01
		380	mW	QFP-80P-L03

*1 V_{IN} and V_{OUT} must not exceed V_{DD} + 0.3V.

*2 The high current drive transistor is the N-ch transistor of Port C (PC).

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should be conducted under the recommended operating conditions. Exceeding these conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions

(V_{SS} = 0V)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V _{DD}	4.5	5.5	V	fc = 10MHz or less Guaranteed operation range during 1/2 and 1/4 frequency dividing mode
		2.7	5.5		
		2.7	5.5		Guaranteed operation range during 1/16 frequency dividing mode or sleep mode
		2.7	5.5		Guaranteed operation range with TEX clock
		2.5	5.5		Guaranteed data hold range during stop
LCD bias voltage	V _{LC1}	V _{SS}	V _{DD}	V	LCD power supply range*4
	V _{LC2}				
	V _{LC3}				
High level input voltage	V _{IH}	0.7V _{DD}	V _{DD}	V	*1
	V _{IHS}	0.8V _{DD}	V _{DD}	V	Hysteresis input*2
	V _{IHEX}	V _{DD} - 0.4	V _{DD} + 0.3	V	EXTAL*3, TEX*5
Low level input voltage	V _{IL}	0	0.3V _{DD}	V	*1
	V _{ILS}	0	0.2V _{DD}	V	Hysteresis input*2
	V _{ILEX}	-0.3	0.4	V	EXTAL*3, TEX*5
Operating temperature	Topr	-20	+75	°C	

*1 Value for each pin of normal input ports (PA, PB0, PB4, PB7, PC and PI).

*2 Value of the following pins; $\overline{\text{RST}}$, $\overline{\text{CS0}}$, $\overline{\text{SI0}}$, $\overline{\text{SI1}}$, $\overline{\text{SCK0}}$, $\overline{\text{SCK1}}$, $\overline{\text{EC/INT0}}$, INT1, INT2, INT3, INT4 and RMC.

*3 Specifies only during external clock input.

*4 Optimal values are determined by LCD used.

*5 Specifies only during external event count input.

Electrical Characteristics

DC Characteristics (V_{DD} = 4.5 to 5.5V)

(Ta = -20 to +75°C, V_{SS} = 0V)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit	
High level output voltage	V _{OH}	SCK0*1, S00*1	V _{DD} = 4.5V, I _{OH} = -1.0mA	4.0			V	
		SCK1*1, S01*1	V _{DD} = 4.5V, I _{OH} = -2.4mA	3.5			V	
		PA, PB, PC, PD*2, PE5, PE6, PF*2, PH0, VL (V _{OL} only)	V _{DD} = 4.5V, I _{OH} = -0.5mA	4.0				V
			V _{DD} = 4.5V, I _{OH} = -1.2mA	3.5				V
Low level output voltage	V _{OL}	PA, PB, PC, PD*2, PE5, PE6, PF*2, PH0, VL (V _{OL} only)	V _{DD} = 4.5V, I _{OL} = 1.8mA			0.4	V	
			V _{DD} = 4.5V, I _{OL} = 3.6mA			0.6	V	
		PC	V _{DD} = 4.5V, I _{OL} = 12.0mA			1.5	V	
Input current	I _{IHE}	EXTAL	V _{DD} = 5.5V, V _{IH} = 5.5V	0.5		40	V	
	I _{ILE}		V _{DD} = 5.5V, V _{IL} = 0.4V	-0.5		-40	μA	
	I _{IHT}	TEX	V _{DD} = 5.5V, V _{IH} = 5.5V	0.1		10	μA	
	I _{ILT}			-0.1		-10	μA	
	I _{ILR}	RST*3	V _{DD} = 5.5V V _{IL} = 0.4V			-400	μA	
	I _{IL}	PA to PC*4, PE0 to PE4, PH*4, PI, RST*3				-45	μA	
	I _{IH}		V _{DD} = 4.5V, V _{IH} = 4.0V	-2.78			μA	
I/O leakage current	I _{Iz}		V _{DD} = 5.5V V _I = 0, 5.5V			±10	μA	
Common output impedance	R _{COM}	COM0 to COM3	V _{DD} = 5V V _{LC1} = 3.75V V _{LC2} = 2.5V V _{LC3} = 1.25V		3	5	kΩ	
Segment output impedance	R _{SEG}	SEG0 to SEG15, SEG16 to SEG31*2				5	15	kΩ
Supply current*5	I _{DD1}	V _{DD}	High-speed mode operation (1/2 frequency dividing clock) V _{DD} = 5.5V, 10MHz crystal oscillation (C ₁ = C ₂ = 15pF)		12	40	mA	
	I _{DDs1}		Sleep mode V _{DD} = 5.5V, 10MHz crystal oscillation (C ₁ = C ₂ = 15pF)		2.6	8	mA	
	I _{DDs3}		Stop mode V _{DD} = 5.5V, 10MHz and termination of TEX oscillation				10	μA

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Input capacity	C _{IN}	PA to PC, PE0 to PE4, PH, PI, EXTAL, RST	Clock 1MHz 0V for all pins excluding measured pins		10	20	pF

- *1 Specifies when Port B output buffer capability switching register (BUFB: 01F4h) selects the buffer capability to high.
- *2 Common pins of PD0/SEG16 to PD7/SEG23, PF0/SEG24 to PF7/SEG31, PD and PF is the case when the common pin is selected as port; SEG16 to SEG31 is when the common pin is selected as segment output.
- *3 $\overline{\text{RST}}$ specifies the input current when pull-up resistor has been selected; leakage current when no resistor has been selected.
- *4 Pins PA to PC, and PH0 specifies the input current when pull-up resistor has been selected; leakage current when no resistor has been selected.
- *5 When all output pins are left open.

Electrical Characteristics

DC Characteristics (V_{DD} = 2.7 to 3.3V)

(Ta = -20 to +75°C, V_{SS} = 0V)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit	
High level output voltage	V _{OH}	SCK0*1, S00*1 SCK1*1, S01*1	V _{DD} = 2.7V, I _{OH} = -0.24mA	2.5			V	
			V _{DD} = 2.7V, I _{OH} = -0.90mA	2.1			V	
		PA, PB, PC, PD*2, PE5, PE6, PF*2, PH0, VL (VOL only)	V _{DD} = 2.7V, I _{OH} = -0.12mA	2.5				V
			V _{DD} = 2.7V, I _{OH} = -0.45mA	2.1				V
Low level output voltage	V _{OL}	PC	V _{DD} = 2.7V, I _{OL} = 1.0mA			0.25	V	
			V _{DD} = 2.7V, I _{OL} = 1.4mA			0.4	V	
		V _{DD} = 2.7V, I _{OL} = 4.5mA			0.9	V		
Input current	I _{IHE}	EXTAL	V _{DD} = 3.3V, V _{IH} = 3.3V	0.3		20	V	
	I _{IIE}		V _{DD} = 3.3V, V _{IL} = 0.3V	-0.3		-20	μA	
	I _{IHT}	TEX	V _{DD} = 3.3V, V _{IH} = 3.3V	0.1		10	μA	
	I _{ILT}		V _{DD} = 3.3V V _{IL} = 0.3V	-0.1		-10	μA	
	I _{ILR}	RST*3	V _{DD} = 3.3V V _{IL} = 0.3V	-0.9		-200	μA	
	I _{IIL}	PA to PC*4, PE0 to PE4, PH*4, PI, RST*3	V _{DD} = 3.3V V _{IL} = 0.3V			-20	μA	
	I _{IH}		V _{DD} = 2.7V, V _{IH} = 2.4V	0.9			μA	
I/O leakage current	I _{Iz}		V _{DD} = 3.3V V _I = 0, 3.3V			±10	μA	
Common output impedance	R _{COM}	COM0 to COM3	V _{DD} = 3V V _{LC1} = 2.25V V _{LC2} = 1.5V V _{LC3} = 0.75V		4.5	7.5	kΩ	
Segment output impedance	R _{SEG}	SEG0 to SEG15, SEG16 to SEG31*2	V _{DD} = 3V V _{LC1} = 2.25V V _{LC2} = 1.5V V _{LC3} = 0.75V		10	30	kΩ	
Supply current*5	I _{DD1}	V _{DD}	High-speed mode operation (1/2 frequency dividing clock) V _{DD} = 3.3V, 4MHz crystal oscillation (C ₁ = C ₂ = 15pF)		2.5	8	mA	
	I _{DD2}		V _{DD} = 3.3V, TEX*6 crystal oscillation (C ₁ = C ₂ = 47pF)		30	100	μA	
	I _{DDs1}		Sleep mode V _{DD} = 3.3V, 4MHz crystal oscillation (C ₁ = C ₂ = 15pF)		0.6	2	mA	
			V _{DD} = 3.3V, TEX*6 crystal oscillation (C ₁ = C ₂ = 47pF)		16	30	μA	
	I _{DDs3}		Stop mode V _{DD} = 3.3V, 4MHz and termination of TEX oscillation				10	μA

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Input capacity	C _{IN}	PA to PC, PE0 to PE4, PH, PI, <u>EXTAL</u> , TEX, <u>RST</u>	Clock 1MHz 0V for all pins excluding measured pins		10	20	pF

- *1 Specifies when Port B output buffer capability switching register (BUFB: 01F4h) selects the buffer capability to high.
- *2 Common pins of PD0/SEG16 to PD7/SEG23, PF0/SEG24 to PF7/SEG31, PD and PF is the case when the common pin is selected as port; SEG16 to SEG31 is when the common pin is selected as segment output.
- *3 RST specifies the input current when pull-up resistor has been selected; leakage current when no resistor has been selected.
- *4 Pins PA to PC, and PH0 specifies the input current when pull-up resistor has been selected; leakage current when no resistor has been selected.
- *5 When all output pins are left open.
- *6 The value when 32.768kHz oscillator is connected to TEX.

AC Characteristics

(1) Clock timing

(Ta = -20 to +75°C, VDD = 2.7 to 5.5V, VSS = 0V)

Item	Symbol	Pin	Conditions	Min.	Typ.	Max.	Unit
System clock frequency	fc	XTAL EXTAL	Fig. 1, Fig. 2	VDD = 4.5 to 5.5V	1	10	MHz
					1	5	
System clock input pulse width	tXL, tXH	EXTAL	Fig. 1, Fig. 2	external clock drive	VDD = 4.5 to 5.5V	37.5	ns
						77.5	
System clock input rise and fall time	tCR, tCF	EXTAL	Fig. 1, Fig. 2			200	ns
Event count input clock pulse width	tEH, tEL	EC	Fig. 3				ns
				t _{sys} + 50*1			
Event count input clock rise and fall time	tER, tEF	EC	Fig. 3			20	ms
System clock frequency	fc	TEX TX	VDD = 2.7 to 5.5V Fig. 2 (32kHz clock applied condition)		32.768		kHz
Event count input clock input pulse width	tTL, tTH	TEX	Fig. 3	10			μs
Event count input clock rise and fall time	tTR, tTF	TEX	Fig. 3			20	ms

*1 t_{sys} indicates the three values below according to the upper two bits (CPU clock selection) of the clock control register (CLC: 00FEh).

t_{sys} [ns] = 2000/fc (upper two bits = "00"), 4000/fc (upper two bits = "01"), 16000/fc (upper two bits = "11").

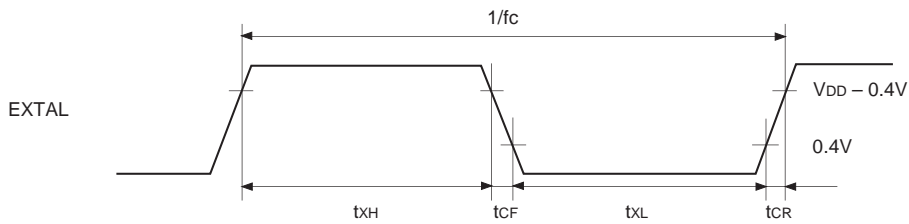


Fig. 1. Clock timing

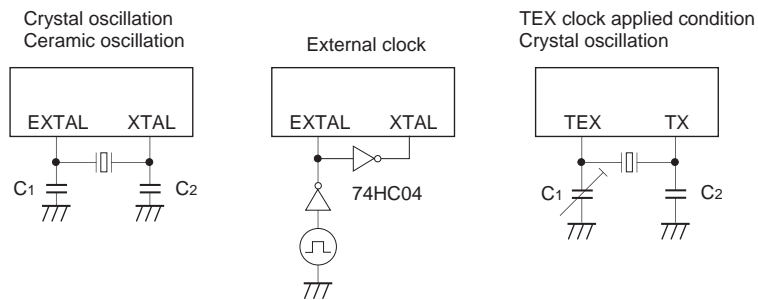


Fig. 2. Clock applied conditions

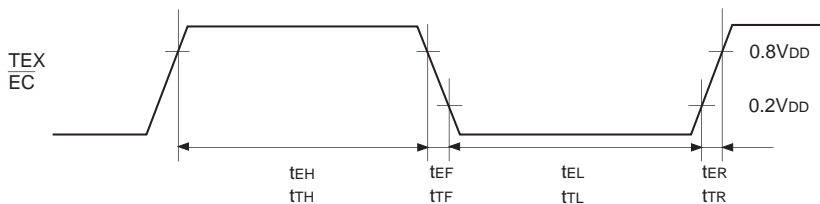


Fig. 3. Event count clock timing

(2) Serial transfer (CH0)

(Ta = -20 to +75°C, VDD = 4.5 to 5.5V, VSS = 0V)

Item	Symbol	Pin	Conditions	Min.	Max.	Unit
$\overline{CS} \downarrow \rightarrow \overline{SCK}$ delay time	t _{D\overline{CSK}}	$\overline{SCK0}$	Chip select transfer mode (\overline{SCK} = output mode)		t _{sys} + 200	ns
$\overline{CS} \uparrow \rightarrow \overline{SCK}$ float delay time	t _{D\overline{CSKF}}	$\overline{SCK0}$	Chip select transfer mode (\overline{SCK} = output mode)		t _{sys} + 200	ns
$\overline{CS} \downarrow \rightarrow SO$ delay time	t _{D\overline{CSO}}	SO0	Chip select transfer mode		t _{sys} + 200	ns
$\overline{CS} \downarrow \rightarrow SO$ float delay time	t _{D\overline{CSOF}}	SO0	Chip select transfer mode		t _{sys} + 200	ns
\overline{CS} high level width	t _{WH\overline{CS}}	$\overline{CS0}$	Chip select transfer mode	t _{sys} + 200		ns
\overline{SCK} cycle time	t _{K\overline{CY}}	$\overline{SCK0}$	Input mode	2t _{sys} + 200		ns
			Output mode	16000/fc		ns
\overline{SCK} high and low level widths	t _{KH} t _{KL}	$\overline{SCK0}$	Input mode	t _{sys} + 100		ns
			Output mode	8000/fc - 100		ns
SI input setup time (for $\overline{SCK} \uparrow$)	t _{SIK}	SI0	\overline{SCK} input mode	-t _{sys} + 100		ns
			\overline{SCK} output mode	200		ns
SI input hold time (for $\overline{SCK} \uparrow$)	t _{KSI}	SI0	\overline{SCK} input mode	2t _{sys} + 100		ns
			\overline{SCK} output mode	100		ns
$\overline{SCK} \downarrow \rightarrow SO$ delay time	t _{KSO}	SO0	\overline{SCK} input mode		2t _{sys} + 200	ns
			\overline{SCK} output mode		100	ns

Note 1) t_{sys} indicates the three values below according to the upper two bits (CPU clock selection) of the clock control register (CLC: 00FEh).

t_{sys} [ns] = 2000/fc (upper two bits = "00"), 4000/fc (upper two bits = "01"), 16000/fc (upper two bits = "11")

Note 2) \overline{CS} , \overline{SCK} , SI and SO indicates $\overline{CS0}$, $\overline{SCK0}$, SI0 and SO0, respectively.

Note 3) The load condition for the \overline{SCK} output mode, SO output delay time is 50pF + 1TTL.

Note 4) The value when Port B output buffer capability switching register (BUFB: 01F4h) selects buffer capability to normal.

Serial transfer (CH0)

(Ta = -20 to +75°C, VDD = 2.7 to 3.3V, VSS = 0V)

Item	Symbol	Pin	Conditions	Min.	Max.	Unit
$\overline{CS} \downarrow \rightarrow \overline{SCK}$ delay time	t _{DCSK}	$\overline{SCK0}$	Chip select transfer mode (\overline{SCK} = output mode)		t _{sys} + 250	ns
$\overline{CS} \uparrow \rightarrow \overline{SCK}$ float delay time	t _{DCSKF}	$\overline{SCK0}$	Chip select transfer mode (\overline{SCK} = output mode)		t _{sys} + 200	ns
$\overline{CS} \downarrow \rightarrow SO$ delay time	t _{DCSO}	SO0	Chip select transfer mode		t _{sys} + 250	ns
$\overline{CS} \downarrow \rightarrow SO$ float delay time	t _{DCSOF}	SO0	Chip select transfer mode		t _{sys} + 200	ns
\overline{CS} high level width	t _{WHCS}	$\overline{CS0}$	Chip select transfer mode	t _{sys} + 200		ns
\overline{SCK} cycle time	t _{KCY}	$\overline{SCK0}$	Input mode	2t _{sys} + 200		ns
			Output mode	16000/fc		ns
\overline{SCK} high and low level widths	t _{KH} t _{KL}	$\overline{SCK0}$	Input mode	t _{sys} + 100		ns
			Output mode	8000/fc - 150		ns
SI input setup time (for $\overline{SCK} \uparrow$)	t _{SIK}	SI0	\overline{SCK} input mode	-t _{sys} + 100		ns
			\overline{SCK} output mode	200		ns
SI input hold time (for $\overline{SCK} \uparrow$)	t _{KSI}	SI0	\overline{SCK} input mode	2t _{sys} + 100		ns
			\overline{SCK} output mode	100		ns
$\overline{SCK} \downarrow \rightarrow SO$ delay time	t _{KSO}	SO0	\overline{SCK} input mode		2t _{sys} + 250	ns
			\overline{SCK} output mode		125	ns

Note 1) t_{sys} indicates the three values below according to the upper two bits (CPU clock selection) of the clock control register (CLC: 00FEh).

t_{sys} [ns] = 2000/fc (upper two bits = "00"), 4000/fc (upper two bits = "01"), 16000/fc (upper two bits = "11")

Note 2) \overline{CS} , \overline{SCK} , SI and SO indicates $\overline{CS0}$, $\overline{SCK0}$, SI0 and SO0, respectively.

Note 3) The load condition for the \overline{SCK} output mode, SO output delay time is 50pF.

Note 4) The value when Port B output buffer capability switching register (BUFB: 01F4h) selects buffer capability to high.

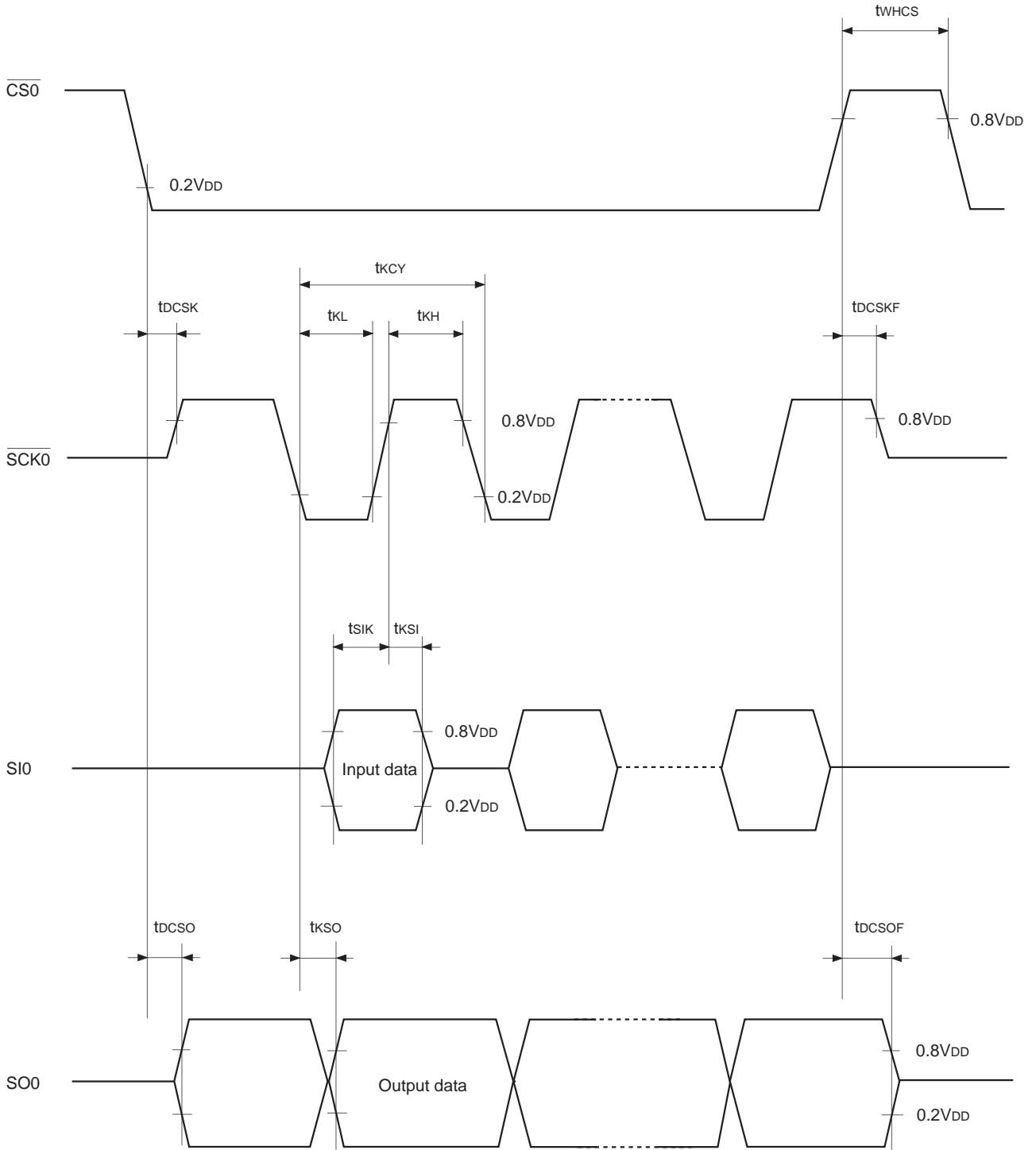


Fig. 4. Serial transfer CH0 timing

Serial Transfer (CH1)

(Ta = -20 to +75°C, VDD = 4.5 to 5.5V, VSS = 0V)

Item	Symbol	Pin	Conditions	Min.	Max.	Unit
$\overline{\text{SCK}}$ cycle time	t_{KCY}	$\overline{\text{SCK1}}$	Input mode	1000		ns
			Output mode	8000/fc		ns
$\overline{\text{SCK}}$ high and low level widths	t_{KH} t_{KL}	$\overline{\text{SCK1}}$	Input mode	400		ns
			Output mode	4000/fc - 50		ns
SI input setup time (for $\overline{\text{SCK}} \uparrow$)	t_{SIK}	SI1	$\overline{\text{SCK}}$ input mode	100		ns
			$\overline{\text{SCK}}$ output mode	200		ns
SI input hold time (for $\overline{\text{SCK}} \uparrow$)	t_{KSI}	SI1	$\overline{\text{SCK}}$ input mode	200		ns
			$\overline{\text{SCK}}$ output mode	100		ns
$\overline{\text{SCK}} \downarrow \rightarrow \text{SO}$ delay time	t_{KSO}	SO1	$\overline{\text{SCK}}$ input mode		200	ns
			$\overline{\text{SCK}}$ output mode		100	ns

- Note 1)** t_{sys} indicates the three values below according to the upper two bits (CPU clock selection) of the clock control register (CLC: 00FEh).
 t_{sys} [ns] = 2000/fc (upper two bits = "00"), 4000/fc (upper two bits = "01"), 16000/fc (upper two bits = "11")
- Note 2)** $\overline{\text{SCK}}$, SI and SO indicates $\overline{\text{SCK1}}$, SI1 and SO1, respectively.
- Note 3)** The load condition for the $\overline{\text{SCK1}}$ output mode, SO1 output delay time is 50pF + 1TTL.
- Note 4)** The value when Port B output buffer capability switching register (BUFB: 01F4h) selects buffer capability to normal.

Serial Transfer (CH1)

(Ta = -20 to +75°C, VDD = 2.7 to 3.3V, VSS = 0V)

Item	Symbol	Pin	Conditions	Min.	Max.	Unit
$\overline{\text{SCK}}$ cycle time	t_{KCY}	$\overline{\text{SCK1}}$	Input mode	1000		ns
			Output mode	8000/fc		ns
$\overline{\text{SCK}}$ high and low level widths	t_{KH} t_{KL}	$\overline{\text{SCK1}}$	Input mode	400		ns
			Output mode	4000/fc - 100		ns
SI input setup time (for $\overline{\text{SCK}} \uparrow$)	t_{SIK}	SI1	$\overline{\text{SCK}}$ input mode	100		ns
			$\overline{\text{SCK}}$ output mode	200		ns
SI input hold time (for $\overline{\text{SCK}} \uparrow$)	t_{KSI}	SI1	$\overline{\text{SCK}}$ input mode	200		ns
			$\overline{\text{SCK}}$ output mode	100		ns
$\overline{\text{SCK}} \downarrow \rightarrow \text{SO}$ delay time	t_{KSO}	SO1	$\overline{\text{SCK}}$ input mode		250	ns
			$\overline{\text{SCK}}$ output mode		125	ns

- Note 1)** t_{sys} indicates the three values below according to the upper two bits (CPU clock selection) of the clock control register (CLC: 00FEh).
 t_{sys} [ns] = 2000/fc (upper two bits = "00"), 4000/fc (upper two bits = "01"), 16000/fc (upper two bits = "11")
- Note 2)** $\overline{\text{SCK}}$, SI and SO indicates $\overline{\text{SCK1}}$, SI1 and SO1, respectively.
- Note 3)** The load condition for the $\overline{\text{SCK1}}$ output mode, SO1 output delay time is 50pF.
- Note 4)** The value when Port B output buffer capability switching register (BUFB: 01F4h) selects buffer capability to high.

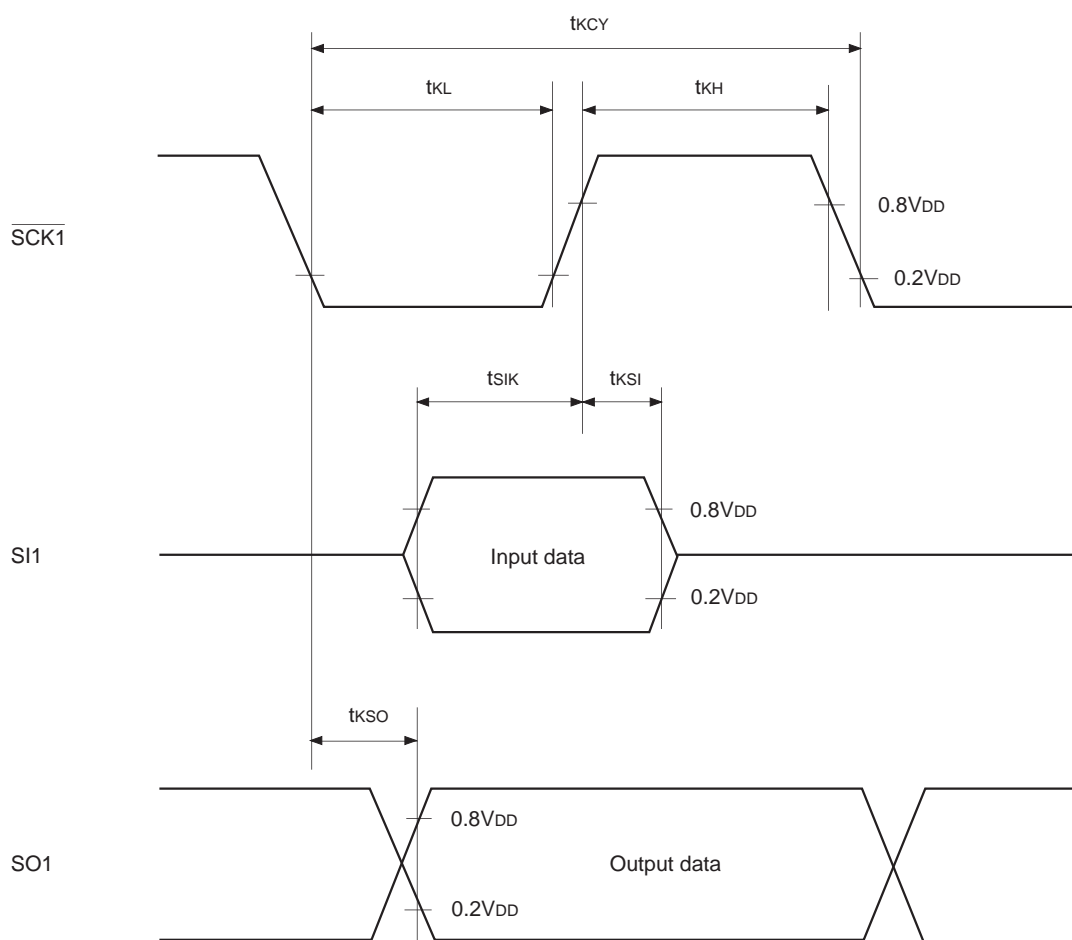


Fig. 5. Serial transfer CH1 timing

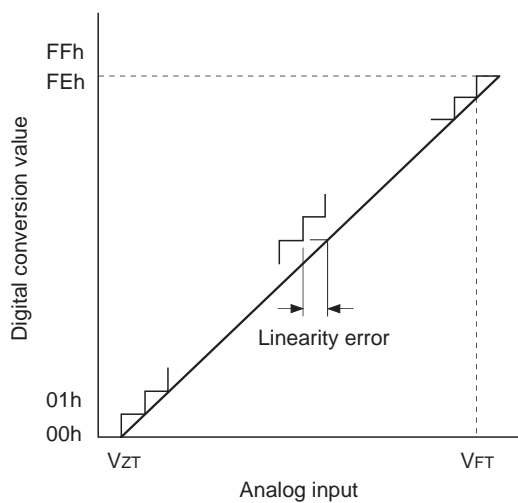
(3) A/D converter characteristics

(Ta = -20 to +75°C, VDD = 4.5 to 5.5V, VSS = 0V)

Item	Symbol	Pin	Conditions	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error						±3	LSB
Zero transition voltage	V _{ZT} *1		Ta = 25°C VDD = 5.0V VSS = 0V	-10	10	70	mV
Full-scale transition voltage	V _{FT} *2			4910	4970	5030	mV
Conversion time	t _{CONV}			31/f _{ADC} *3			µs
Sampling time	t _{SAMP}			10/f _{ADC} *3			µs
Analog input voltage	V _{IAN}	AN0 to AN7		0		VDD	V

(Ta = -20 to +75°C, VDD = 2.7 to 3.3V, VSS = 0V)

Item	Symbol	Pin	Conditions	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error						±3	LSB
Zero transition voltage	V _{ZT} *1		Ta = 25°C VDD = 2.7V VSS = 0V	-10	11	40	mV
Full-scale transition voltage	V _{FT} *2			2651	2688	2716	mV
Conversion time	t _{CONV}			31/f _{ADC} *3			µs
Sampling time	t _{SAMP}			10/f _{ADC} *3			µs
Analog input voltage	V _{IAN}	AN0 to AN7		0		VDD	V



- *1 V_{ZT}: Value at which the digital conversion value changes from 00h to 01h and vice versa.
- *2 V_{FT}: Value at which the digital conversion value changes from FEh to FFh and vice versa.
- *3 f_{ADC} = fc/4

Fig. 6. Definition of A/D converter terms

(4) Interruption, reset input

($T_a = -20$ to $+75^\circ\text{C}$, $V_{DD} = 2.7$ to 5.5V , $V_{SS} = 0\text{V}$)

Item	Symbol	Pin	Conditions	Min.	Max.	Unit
External interruption high and low level widths	t_{IH} t_{IL}	INT0 INT1 INT2 INT3 INT4		1		μs
Reset input low level width	t_{RSL}	$\overline{\text{RST}}$		$32/f_c$		μs

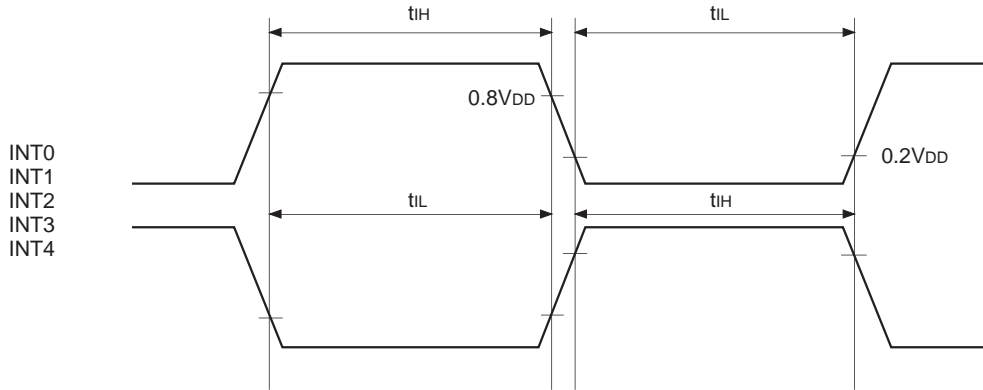


Fig. 7. Interruption input timing

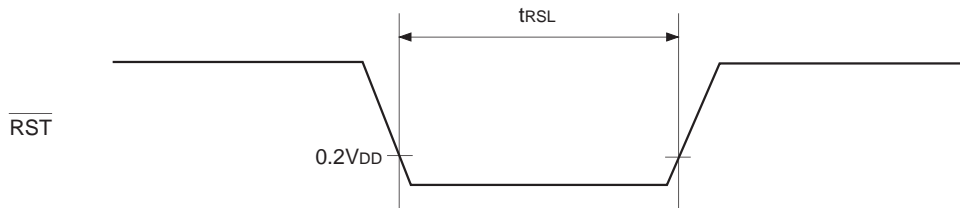


Fig. 8. $\overline{\text{RST}}$ input timing

Appendix

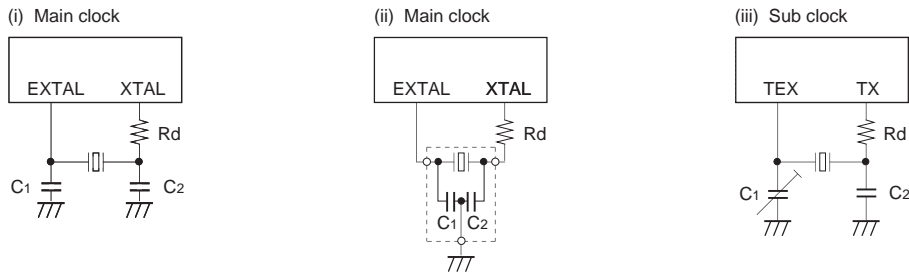


Fig. 9. SPC700 series recommended oscillation circuit

Manufacturer	Model	fc (MHz)	C1 (pF)	C2 (pF)	Rd (Ω)	Circuit example	Remarks	
MURATA MFG CO., LTD.	CSA4.19MG	4.19	100	100	0	(i)		
	CSA8.00MG	8.00	30	30	0			
	CSA10.0MT	10.00	30	30	0			
	CST4.19MGW*1	4.19	100	100	0	(ii)		
	CST8.00MTW*1	8.00	30	30	0			
	CST10.00MTW*1	10.00	30	30	0			
RIVER ELETEC CO., LTD.	HC-49/U03	4.19	22	22	1.0k	(i)		
		8.00	15	15	100			
		10.00	10	10	100			
KINSEKI LTD.	CX-5F	4.19	33	33	2.2k			CL = 12.0pF
		8.00	18	18	0			CL = 12.0pF
		10.00	15	15	0			CL = 12.0pF
TDK Corporation	FCR4.19MC5*1	4.19	30 (± 20%)	30 (± 20%)	0	(ii)		
	FCR8.0MC5*1	8.00	20 (± 20%)	20 (± 20%)				
	FCR10.0MC5*1	10.00	20 (± 20%)	20 (± 20%)				
	CCR4.19MC3*1	4.19	36 (± 20%)	36 (± 20%)				
	CCR8.0MC5*1	8.00	20 (± 20%)	20 (± 20%)				
	CCR10.0MC5*1	10.00	20 (± 20%)	20 (± 20%)				
Seiko Instruments Inc.	VTC-200 SP-T	32.768	18	18	330k	(iii)	CL = 12.5pF	
		75.00	4	4	100k		CL = 6.0pF	

*1 Those marked with an *1 signify types with built-in ground capacitance (C1, C2).

FCR***: Lead-type ceramic oscillator
 CCR***: Surface mounted-type ceramic oscillator
 CL : Load capacitor

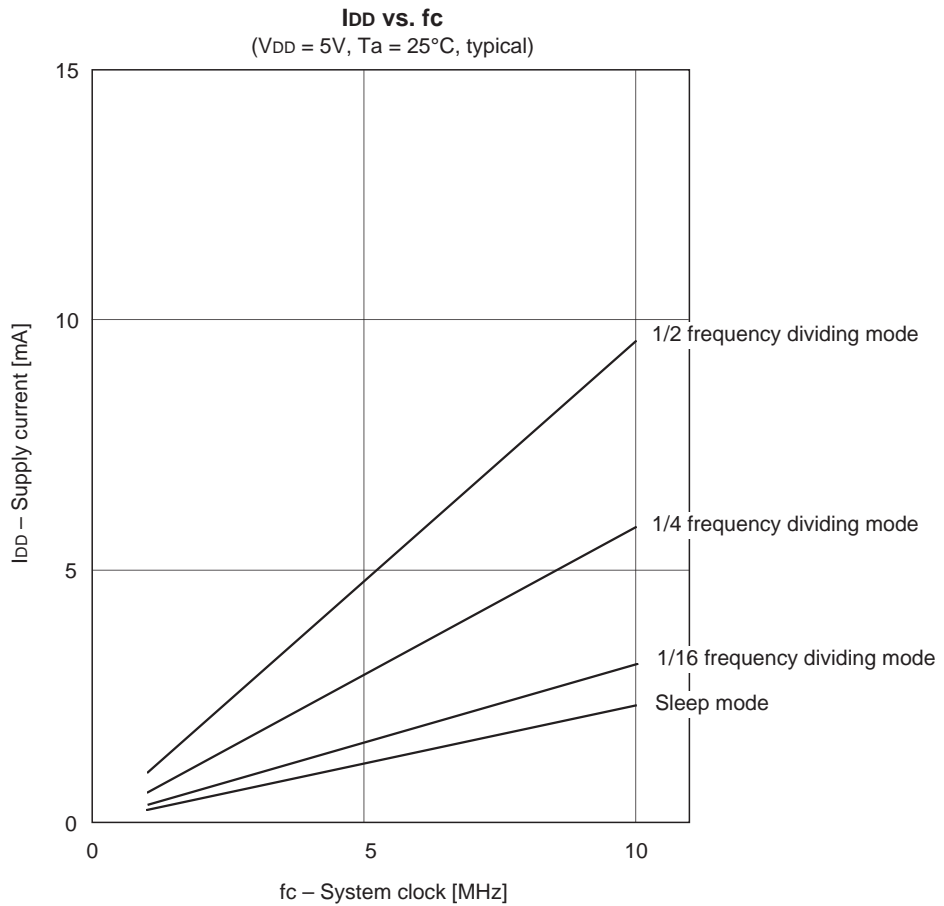
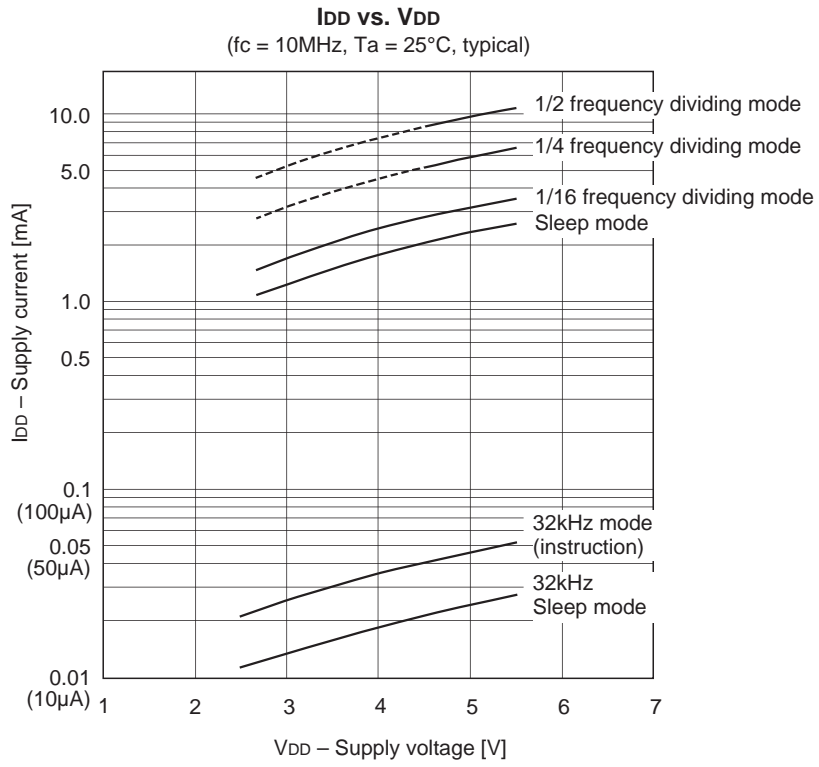
Mask Option Table

Item	Content	
Reset pin pull-up resistor	Non-existent	Existent

Package List

Product name	Package
CXP83508/83512/83516	80-pin plastic QFP/LQFP
CXP83509/83513/83517	80-pin plastic QFP (0.65mm pitch)

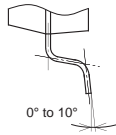
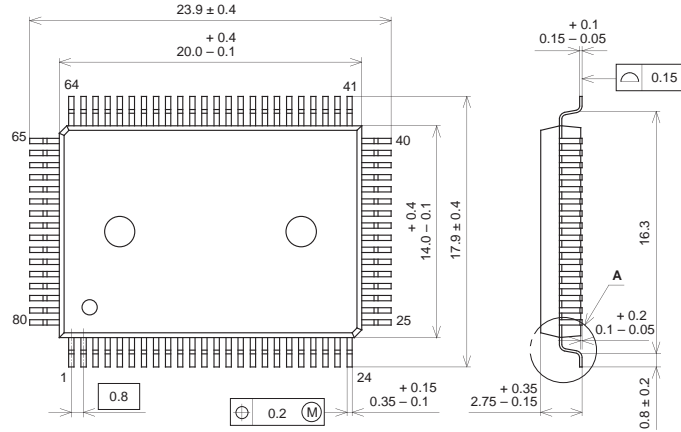
Characteristics Curve



Package Outline Unit: mm

CXP83508/83512/83516

80PIN QFP (PLASTIC)



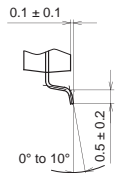
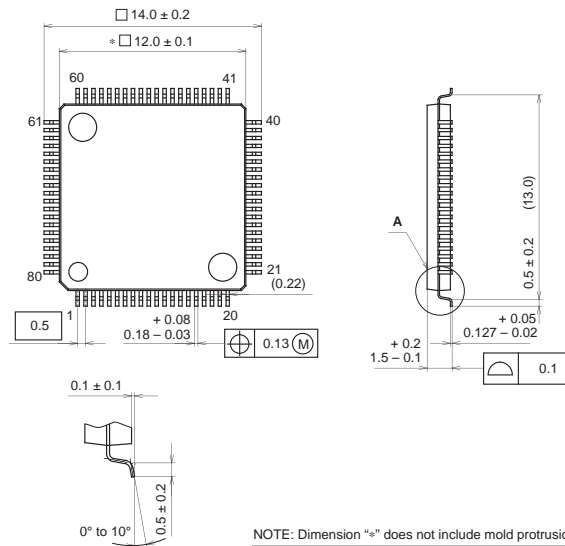
SONY CODE	QFP-80P-L01
EIAJ CODE	QFP080-P-1420
JEDEC CODE	—

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.6g

CXP83508/83512/83516

80PIN LQFP (PLASTIC)



NOTE: Dimension "*" does not include mold protrusion.

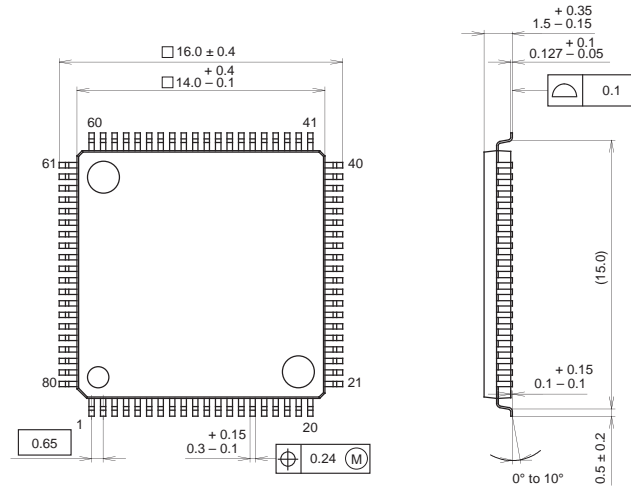
SONY CODE	LQFP-80P-L01
EIAJ CODE	LQFP080-P-1212
JEDEC CODE	—

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	0.5g

CXP83509/83513/83517

80PIN QFP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	QFP-80P-L03
EIAJ CODE	QFP080-P-1414
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.6g