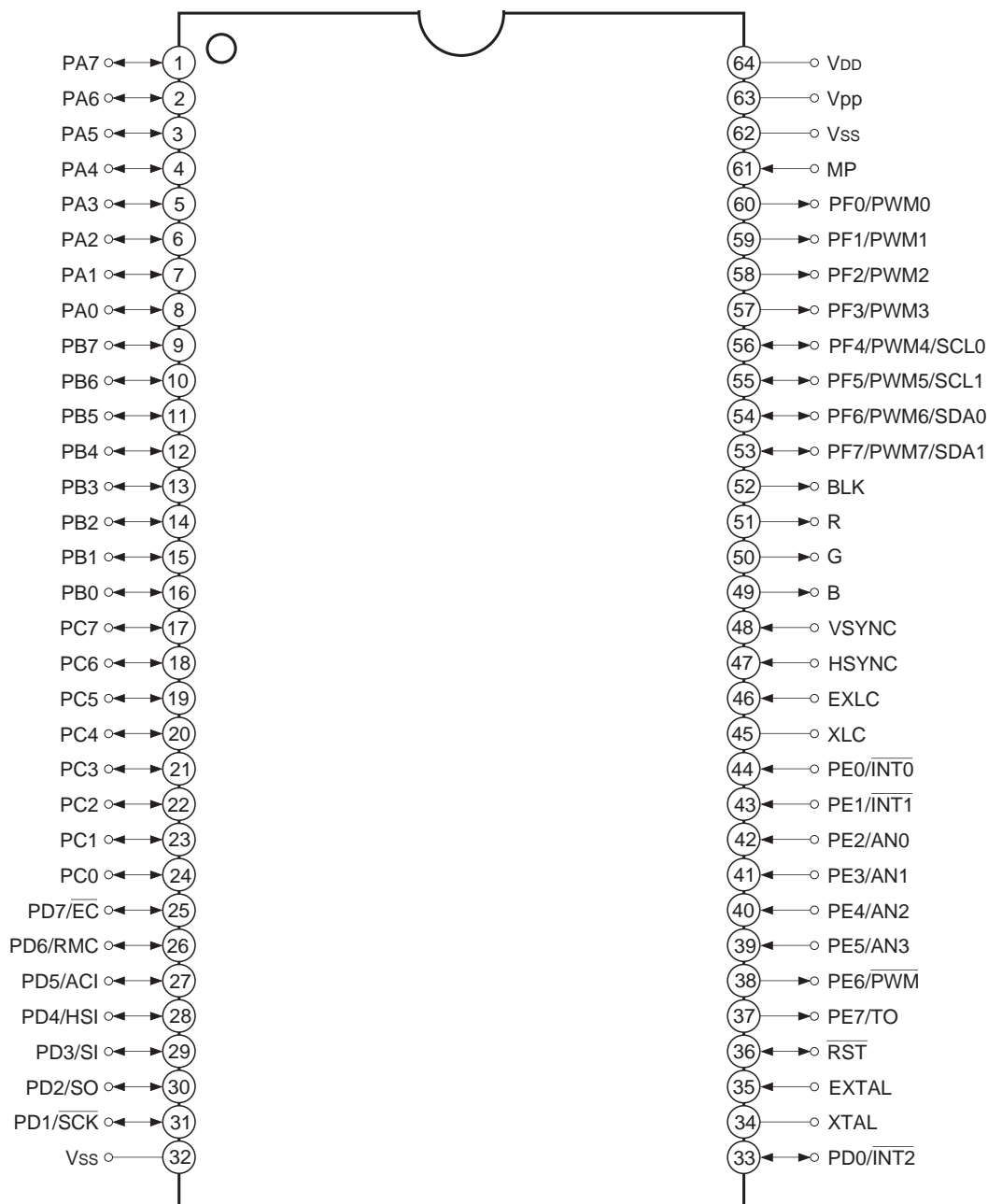


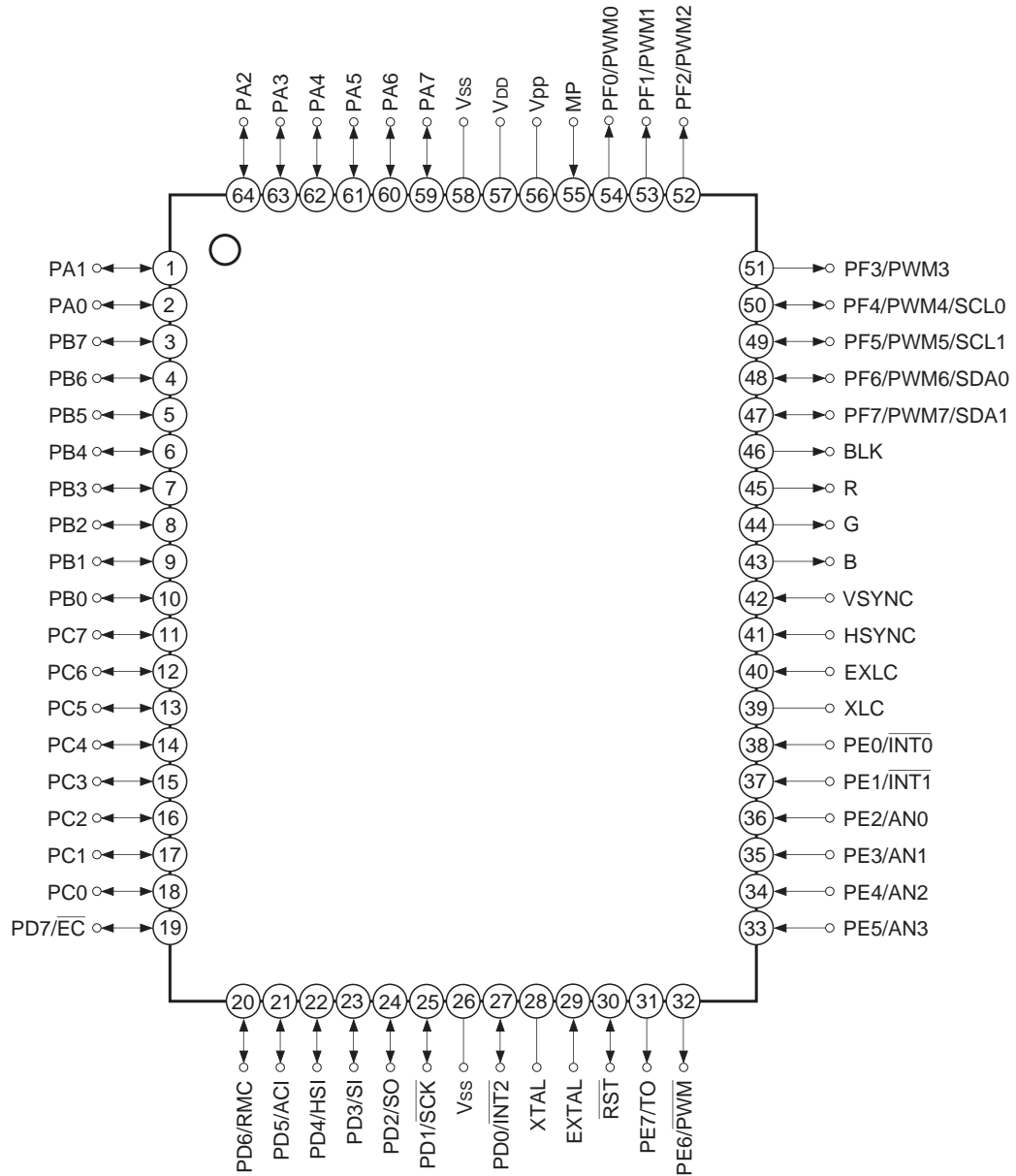
Block Diagram

Pin Assignment 1 (Top View) 64 pin SDIP Package



- Note)**
1. Vpp (Pin 63) is always connected to VDD.
 2. Vss (Pins 32 and 62) are both connected to GND.
 3. MP (Pin 61) is always connected to GND.

Pin Assignment 2 (Top View) 64 pin QFP Package



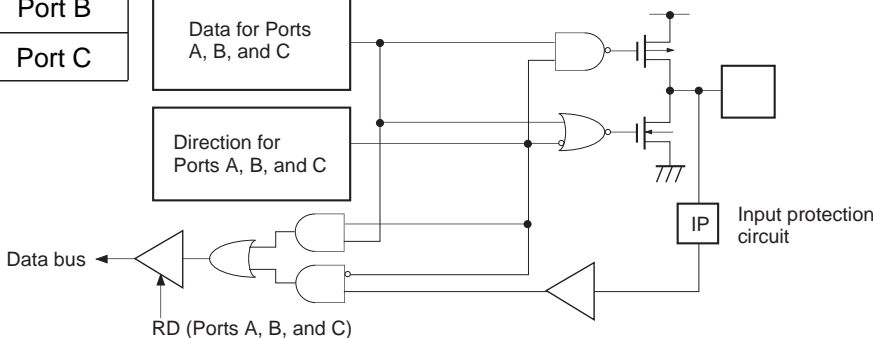
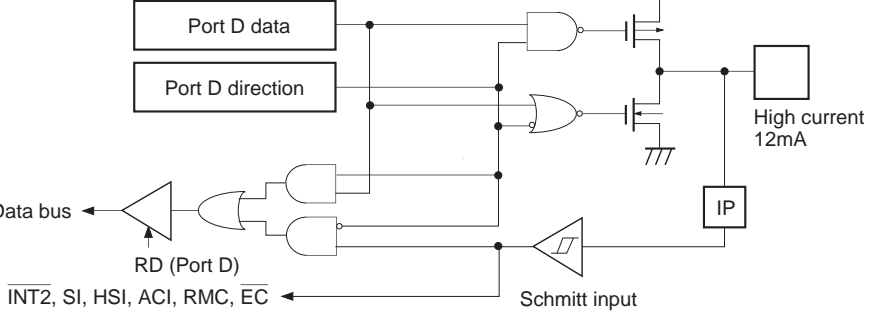
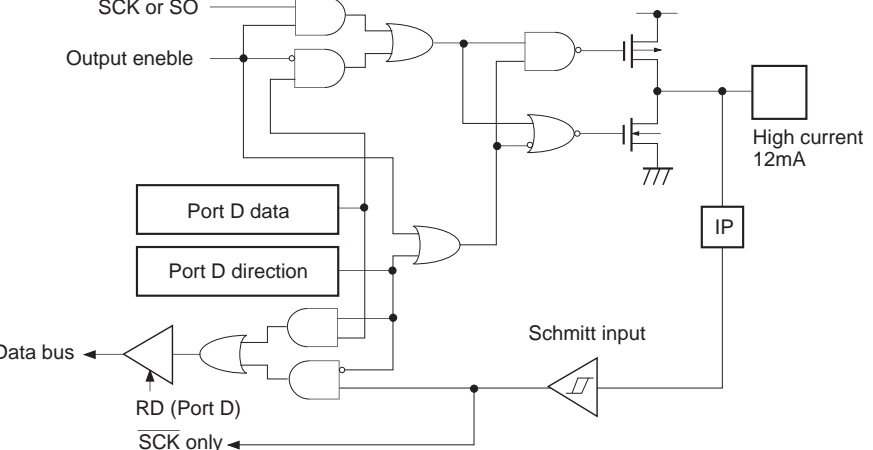
- Note)**
1. Vpp (Pin 56) is always connected to Vdd.
 2. Vss (Pins 26 and 58) are both connected GND.
 3. MP (Pin 55) is always connected to GND.

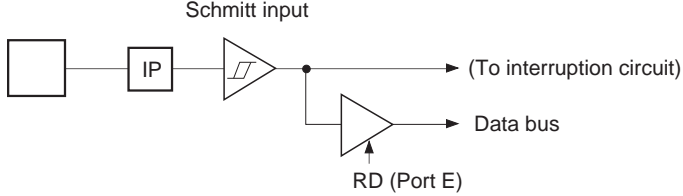
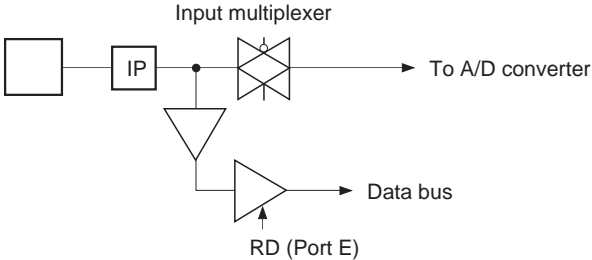
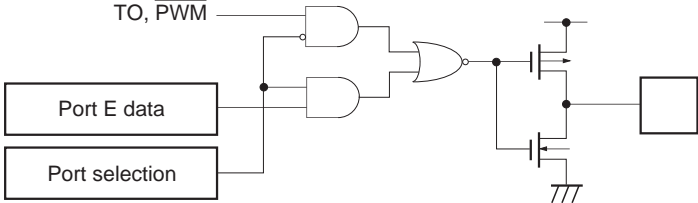
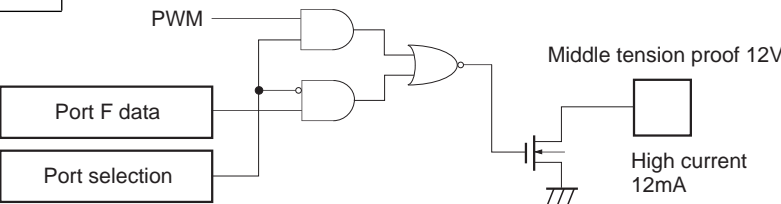
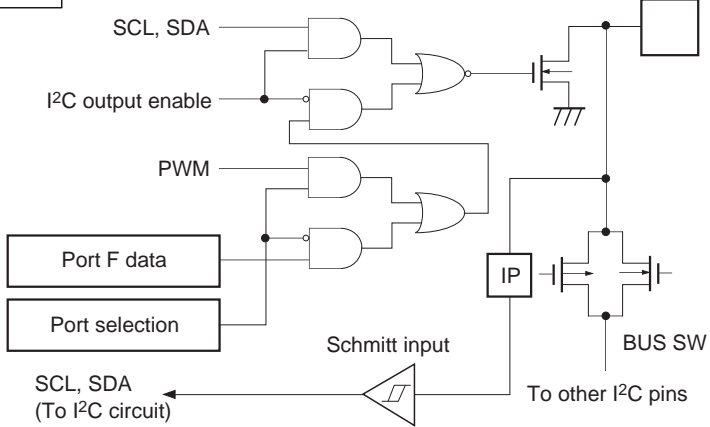
Pin Description

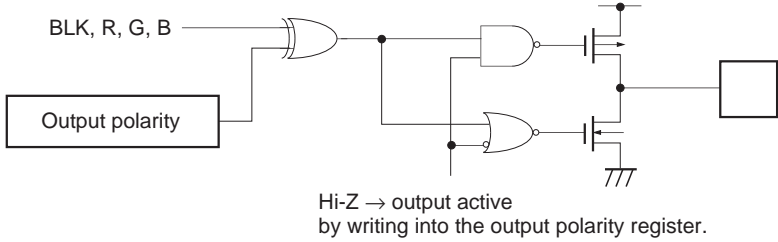
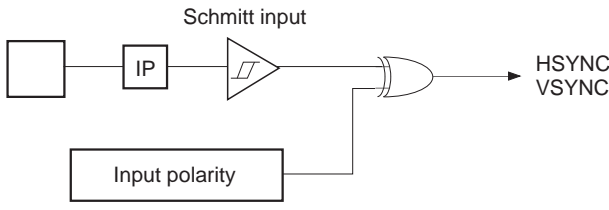
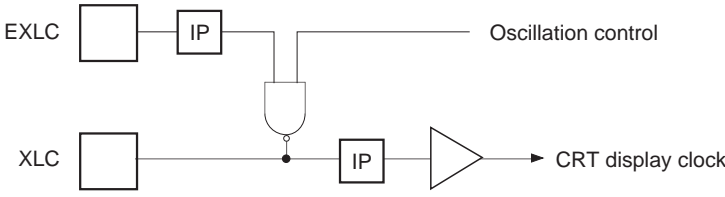
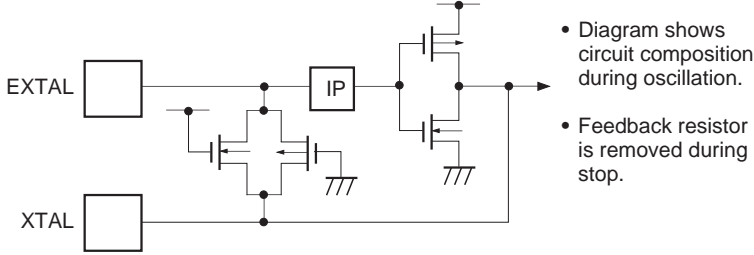
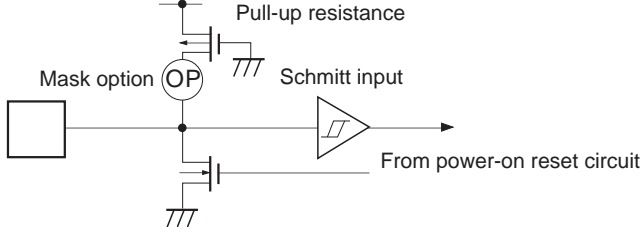
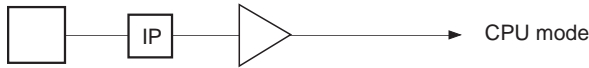
Symbol	I/O	Description	
PA0 to PA7	I/O	(Port A) 8-bit I/O port. I/O can be set in a unit of single bits. (8 pins)	
PB0 to PB7	I/O	(Port B) 8-bit I/O port. I/O can be set in a unit of single bits. (8 pins)	
PC0 to PC7	I/O	(Port C) 8-bit I/O port. I/O can be set in a unit of single bits. (8 pins)	
PD0/ $\overline{\text{INT2}}$	I/O/Input	(Port D) 8-bit I/O port. I/O can be set in a unit of single bits. Capable of driving 12mA sink current. (8 pins)	External interruption request input. Active at falling edge.
PD1/ $\overline{\text{SCK}}$	I/O/I/O		Serial clock I/O.
PD2/SO	I/O/Output		Serial data output.
PD3/SI	I/O/Input		Serial data input.
PD4/HSI	I/O/Input		HSYNC counter input.
PD5/ACI	I/O/Input		Input for power supply frequency counter.
PD6/RMC	I/O/Input		Input for remote control reception circuit.
PD7/ $\overline{\text{EC}}$	I/O/Input		External event input for timer/counter.
PE0/ $\overline{\text{INT0}}$ PE1/ $\overline{\text{INT1}}$	Input/Input	(Port E) 8-bit port. Lower 6 bits are for inputs; upper 2 bits are for outputs. (8 pins)	External interruption request inputs. Active at falling edge. (2 pins)
PE2/AN0 to PE5/AN3	Input/Input		Analog inputs for A/D converter. (4 pins)
PE6/ $\overline{\text{PWM}}$	Output/Output		14-bit PWM output. (CMOS output)
PE7/TO	Output/Output		Rectangular waveform output for Timer 1. (Duty output 50%)
PF0/PWM0 to PF3/PWM3	Output/Output	(Port F) 8-bit output port, operating as N-ch open drain output for high current (12mA). Lower 4 bits are for medium voltage drive outputs (12V), upper 4bits are for 5V drive outputs. (8 pins)	6-bit PWM outputs. (8 pins)
PF4/PWM4/ SCL0 PF5/PWM5/ SCL1	Output/Output/ I/O		Transfer clock I/Os for I ² C bus interface.
PF6/PWM6/ SDA0 PF7/PWM7/ SDA1	Output/Output/ I/O		Transfer data I/Os for I ² C data bus.
R, G, B, BLK	Output	4-bit outputs for CRT display.	
HSYNC	Input	Horizontal synchronizing signal input for CRT display.	
VSYNC	Input	Vertical synchronizing signal input for CRT display.	

Symbol	I/O	Description
EXLC	Input	Clock oscillation I/Os for CRT display. Oscillation frequency is set using the external L and C.
XLC	Output	
EXTAL	Input	Crystal connectors for system clock oscillation. When the clock is supplied externally, input to EXTAL and leave XTAL open.
XTAL	Output	
$\overline{\text{RST}}$	I/O	Low-level active, system reset. $\overline{\text{RST}}$ is an I/O, from which Low level is output when the built-in power-on reset function is activated at the rise of power on.
MP	Input	Microprocessor mode input. For this device, this pin must be grounded.
V _{DD}		Positive power supply.
V _{pp}		Positive power supply pin for on-chip PROM writing. Connect to V _{DD} for normal operation.
V _{ss}		GND. Both V _{ss} must be grounded.

Input/Output Circuit Formats for Pins

Pin	Circuit format	When reset
PA0 to PA7 PB0 to PB7 PC0 to PC7 24 pins		Hi-Z
PD0/ $\overline{\text{INT2}}$ PD3/SI PD4/HSI PD5/ACI PD6/RMC PD7/ $\overline{\text{EC}}$ 6 pins		Hi-Z
PD1/ $\overline{\text{SCK}}$ PD2/SO 2 pins		Hi-Z

Pin	Circuit format	When reset
<p>PE0/$\overline{\text{INT0}}$ PE1/$\overline{\text{INT1}}$</p> <p>2 pins</p>	<p>Port E</p> 	Hi-Z
<p>PE2/AN0 to PE5/AN3</p> <p>4 pins</p>	<p>Port E</p> 	Hi-Z
<p>PE6/$\overline{\text{PWM}}$ PE7/TO</p> <p>2 pins</p>	<p>Port E</p> 	High level
<p>PF0/$\overline{\text{PWM0}}$ to PF3/$\overline{\text{PWM3}}$</p> <p>4 pins</p>	<p>Port F</p> 	Hi-Z
<p>PF4/$\overline{\text{PWM4}}$/ SCL0 PF5/$\overline{\text{PWM5}}$/ SCL1 PF6/$\overline{\text{PWM6}}$/ SDA0 PF7/$\overline{\text{PWM7}}$/ SDA1</p> <p>4 pins</p>	<p>Port F</p> 	Hi-Z

Pin	Circuit format	When reset
<p>BLK R G B</p> <p>4 pins</p>	 <p>Hi-Z → output active by writing into the output polarity register.</p>	<p>Hi-Z</p>
<p>HSYNC VSYNC</p> <p>2 pins</p>		<p>Hi-Z</p>
<p>EXLC XLC</p> <p>2 pins</p>		<p>Oscillation terminated</p>
<p>EXTAL XTAL</p> <p>2 pins</p>	 <ul style="list-style-type: none"> • Diagram shows circuit composition during oscillation. • Feedback resistor is removed during stop. 	<p>Oscillation</p>
<p>$\overline{\text{RST}}$</p> <p>1 pin</p>		<p>Low level</p>
<p>MP</p> <p>1 pin</p>		<p>Hi-Z</p>

Absolute Maximum Ratings

(V_{SS} = 0V reference)

Item	Symbol	Rating	Unit	Remarks
Supply voltage	V _{DD}	-0.3 to +7.0	V	
	V _{pp}	-0.3 to +13.0	V	Incorporated PROM
Input voltage	V _{IN}	-0.3 to +7.0* ¹	V	
Output voltage	V _{OUT}	-0.3 to +7.0* ¹	V	
Medium voltage drive output voltage	V _{OUTP}	-0.3 to +15.0	V	Pins PF0 to PF3
High level output current	I _{OH}	-5	mA	
High level total output current	∑I _{OH}	-50	mA	Total for all output pins
Low level output current	I _{OL}	15	mA	Excludes high current outputs
	I _{OLC}	20	mA	High current outputs* ²
Low level total output current	∑I _{OL}	130	mA	Total for all output pins
Operating temperature	T _{opr}	-10 to +75	°C	
Storage temperature	T _{stg}	-55 to +150	°C	
Allowable power dissipation	P _D	1000	mW	SDIP
		600	mW	QFP

*¹ V_{IN} and V_{OUT} must not exceed V_{DD} + 0.3V.

*² The high current operation transistor are the N-ch transistors of the PD and PF0 to PF3 ports.

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should be conducted under the recommended operating conditions.

Exceeding these conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions

(V_{SS} = 0V reference)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V _{DD}	4.5	5.5	V	Guaranteed operation range
		3.5	5.5	V	Low-speed mode guaranteed operation range* ¹
		2.5	5.5	V	Guaranteed data hold range during stop
	V _{pp}	V _{pp} = V _{DD}		V	* ⁵
High level input voltage	V _{IH}	0.7V _{DD}	V _{DD}	V	Includes I ² C Schmitt input* ²
	V _{IHS}	0.8V _{DD}	V _{DD}	V	CMOS Schmitt input* ³
	V _{IHEX}	V _{DD} - 0.4	V _{DD} + 0.3	V	EXTAL* ⁴
Low level input voltage	V _{IL}	0	0.3V _{DD}	V	Includes I ² C Schmitt input* ²
	V _{ILS}	0	0.2V _{DD}	V	CMOS Schmitt input* ³
	V _{ILEX}	-0.3	0.4	V	EXTAL* ⁴
Operating temperature	T _{opr}	-10	+75	°C	

*¹ Specifies only for 1/16 frequency demultiplication mode and sleep mode.

*² Value for each pin of normal input ports (PA, PB, PC, PE2 to PE5), PF4 to PF7, and MP.

*³ Value of the following pins: PD0/ $\overline{\text{INT2}}$, PD1/ $\overline{\text{SCK}}$, PD2, PD3/SI, PD4/HSI, PD5/ACI, PD6/RMC, PD7/ $\overline{\text{EC}}$, PE0/ $\overline{\text{INT0}}$, PE1/ $\overline{\text{INT1}}$, HSYNC, VSYNC, $\overline{\text{RST}}$.

*⁴ Specifies only during external clock input.

*⁵ V_{pp} and V_{DD} should be set to the same voltage.

Electrical Characteristics

DC Characteristics

(Ta = -10 to +75°C, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output current	V _{OH}	PA to PD, PE6, PE7, R, G, B, BLK	V _{DD} = 4.5V, I _{OH} = -0.5mA	4.0			V
			V _{DD} = 4.5V, I _{OH} = -1.2mA	3.5			V
Low level output current	V _{OL}	PA to PD, PE6, PE7, R, G, B, BLK, PF0 to PF3, RST	V _{DD} = 4.5V, I _{OL} = 1.8mA			0.4	V
			V _{DD} = 4.5V, I _{OL} = 3.6mA			0.6	V
		PD, PF0 to PF3	V _{DD} = 4.5V, I _{OL} = 12.0mA			1.5	V
		PF4 to PF7 (SCL0, SCL1, SDA0, SDA1)	V _{DD} = 4.5V, I _{OL} = 3.0mA			0.4	V
			V _{DD} = 4.5V, I _{OL} = 4.0mA			0.6	V
Input current	I _{IHE}	EXTAL	V _{DD} = 5.5V, V _{IH} = 5.5V	0.5		40	μA
	I _{IHL}		V _{DD} = 5.5V, V _{IL} = 0.4V	-0.5		-40	μA
	I _{ILR}		RST	V _{DD} = 5.5V, V _{IL} = 0.4V	-1.5		-400
I/O leakage current	I _{Iz}	PA to PE, HSYNC, VSYNC, R, G, B, BLK, MP	V _{DD} = 5.5V V _I = 0, 5.5V			±10	μA
Open drain output leakage current (N-ch Tr in off state)	I _{ILOH}	PF0 to PF3	V _{DD} = 5.5V, V _{OH} = 12.0V			50	μA
		PF4 to PF7	V _{DD} = 5.5V, V _{OH} = 5.5V			10	μA
Impedance connected to I ² C bus switch (output Tr in off state)	R _{BS}	SCL0: SCL1 SDA0: SDA1	V _{DD} = 4.5V V _{SCL0} = V _{SCL1} = 2.25V V _{SDA0} = V _{SDA1} = 2.25V			120	Ω
Power supply current	I _{DD}	V _{DD} *1	Operation mode*1 (1/2 frequency demultiplier clock) 4MHz crystal oscillation (C ₁ = C ₂ = 22pF) All outputs open		10	25	mA
	I _{DDSL}				0.7	3	mA
	I _{DDST}				—	—	—
Input capacity	C _{IN}	Pins other than V _{DD} and V _{SS}	Clock 1MHz 0V for no-measured pins		10	20	pF

*1 Rating applies only if OSD oscillator is halted.

*2 This device does not enter in the stop mode.

AC Characteristics

(1) Clock timing

($T_a = -10$ to $+75^\circ\text{C}$, $V_{DD} = 4.5$ to 5.5V , $V_{SS} = 0\text{V}$ reference)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
System clock frequency	f_c	XTAL EXTAL	Fig. 1, Fig. 2	3.5	4.5	MHz
System clock input pulse width	t_{XL} , t_{XH}	EXTAL	Fig. 1, Fig. 2 External clock drive	100		ns
System clock input rise time, fall time	t_{CR} , t_{CF}	EXTAL	Fig. 1, Fig. 2 External clock drive		200	ns
Event counter input clock pulse width	t_{EH} , t_{EL}	\overline{EC}	Fig. 3	$t_{sys} + 50^{*1}$		ns
Event counter input clock rise time, fall time	t_{ER} , t_{EF}	\overline{EC}	Fig. 3		20	ms

*1 t_{sys} indicates the three values below according to the upper two bits (CPU clock selection) of the clock control register (address: 00FEH).

t_{sys} [ns] = $2000/f_c$ (upper two bits = "00"), $4000/f_c$ (upper two bits = "01"), $16000/f_c$ (upper two bits = "11")

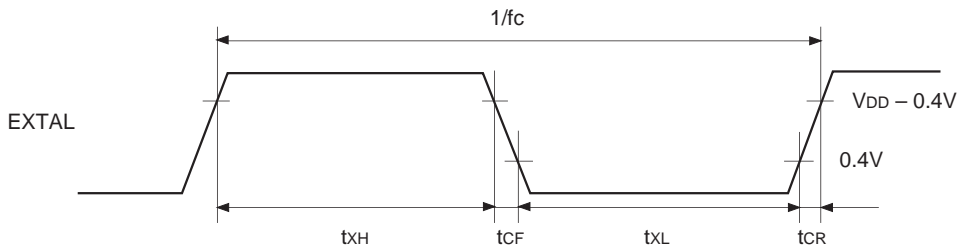


Fig. 1. Clock timing

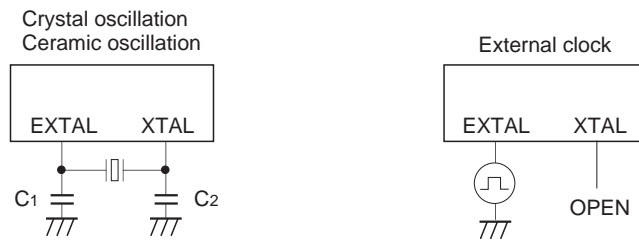


Fig. 2. Clock applied condition

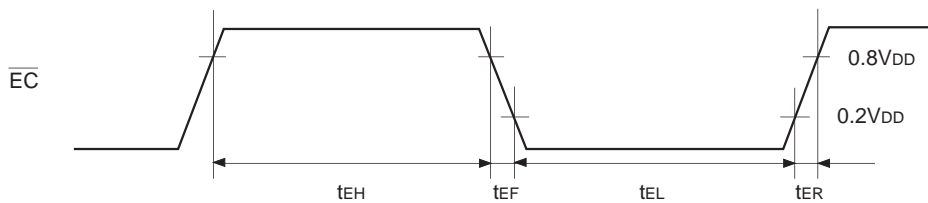


Fig. 3. Event count clock timing

(2) Serial transfer

($T_a = -10$ to $+75^\circ\text{C}$, $V_{DD} = 4.5$ to 5.5V , $V_{SS} = 0\text{V}$ reference)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
$\overline{\text{SCK}}$ cycle time	t_{KCY}	$\overline{\text{SCK}}$	Input mode	1000		ns
			Output mode	8000/fc		ns
$\overline{\text{SCK}}$ High and Low level widths	t_{KH}	$\overline{\text{SCK}}$	$\overline{\text{SCK}}$ input mode	400		ns
	t_{KL}		$\overline{\text{SCK}}$ output mode	4000/fc – 50		ns
SI input setup time (for $\overline{\text{SCK}} \uparrow$)	t_{SIK}	SI	$\overline{\text{SCK}}$ input mode	100		ns
			$\overline{\text{SCK}}$ output mode	200		ns
SI input hold time (for $\overline{\text{SCK}} \uparrow$)	t_{KSI}	SI	$\overline{\text{SCK}}$ input mode	200		ns
			$\overline{\text{SCK}}$ output mode	100		ns
$\overline{\text{SCK}} \downarrow \rightarrow \text{SO}$ delay time	t_{KSO}	SO	$\overline{\text{SCK}}$ input mode		200	ns
			$\overline{\text{SCK}}$ output mode		100	ns

Note) The load condition for the $\overline{\text{SCK}}$ output mode, SO output delay time is $50\text{pF} + 1\text{TTL}$.

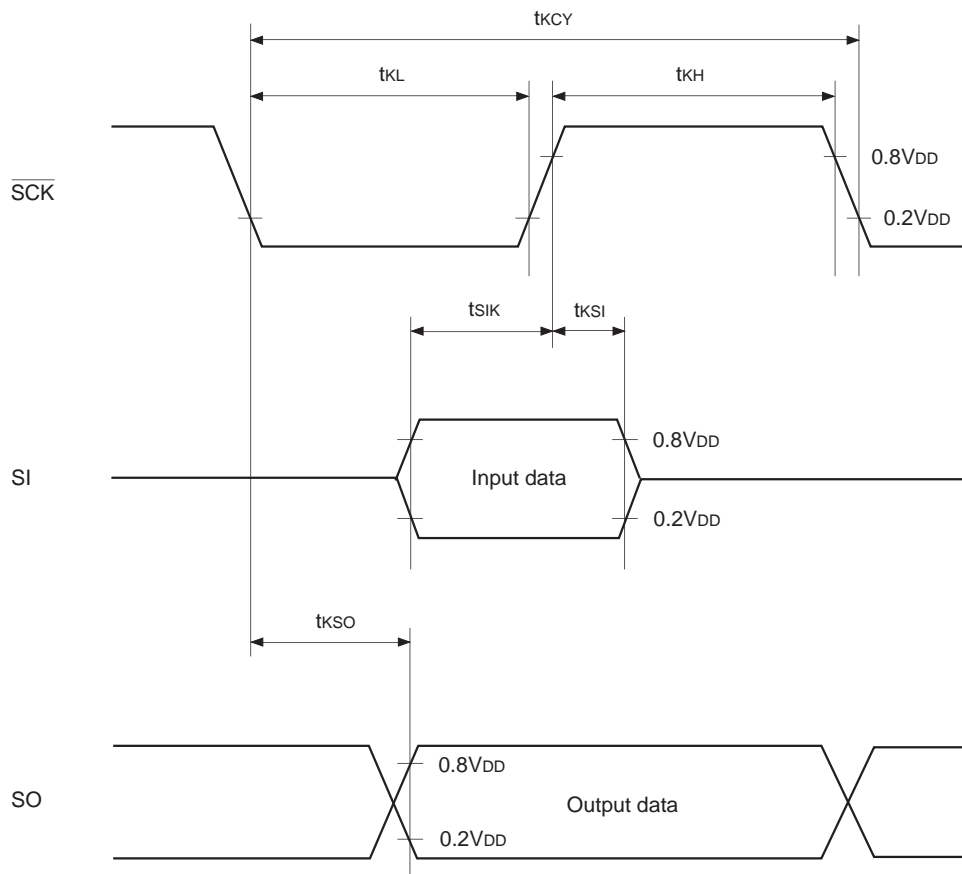


Fig. 4. Serial transfer timing

(3) Interruption, reset input

($T_a = -10$ to $+75^\circ\text{C}$, $V_{DD} = 4.5$ to 5.5V , $V_{SS} = 0\text{V}$ reference)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
External interruption High and Low level widths	t_{IH} t_{IL}	$\overline{\text{INT0}}$ to $\overline{\text{INT2}}$		1		μs
Reset input Low level width	t_{RSL}	$\overline{\text{RST}}$		$8/f_c$		μs

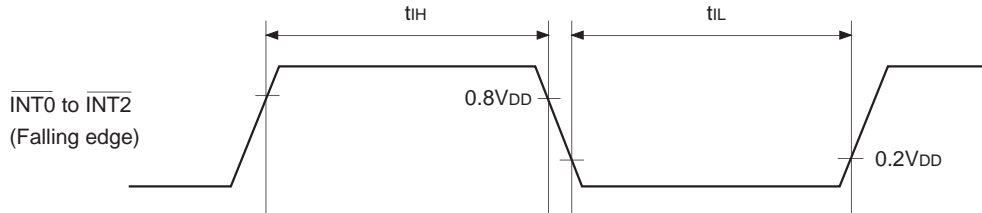


Fig. 5. Interruption input timing

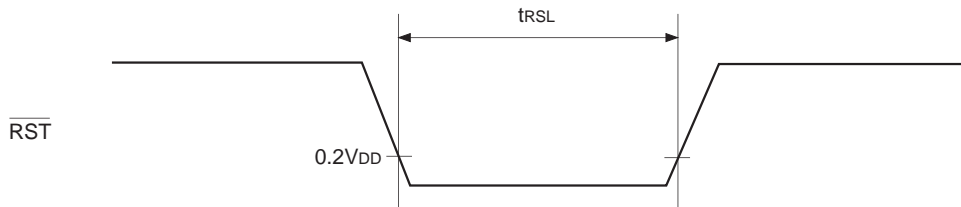


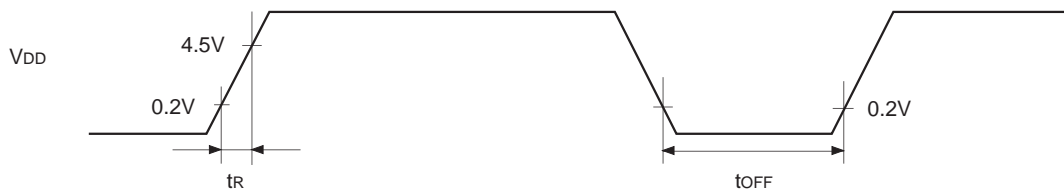
Fig. 6. $\overline{\text{RST}}$ input timing

(4) Power-on reset

Power-on reset

($T_a = -10$ to $+75^\circ\text{C}$, $V_{DD} = 4.5$ to 5.5V , $V_{SS} = 0\text{V}$ reference)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
Power supply rise time	t_R	V_{DD}	Power-on reset	0.05	50	ms
Power supply cut-off time	t_{OFF}		Repetitive power-on reset	1		ms



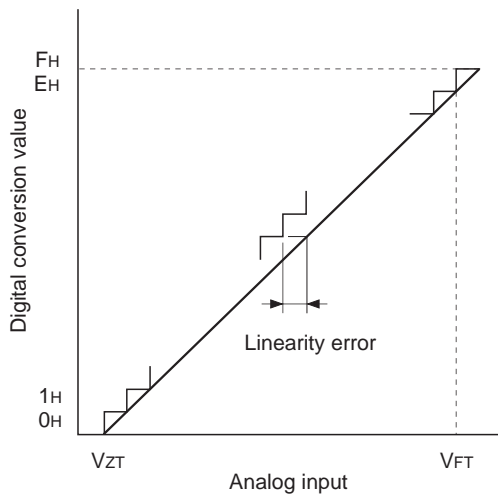
The power supply should be raised smoothly.

Fig. 7. Power-on reset

(5) A/D converter characteristics

($T_a = -10$ to $+75^\circ\text{C}$, $V_{DD} = 4.5$ to 5.5V , $V_{SS} = 0\text{V}$ reference)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Resolution						4	Bits
Linearity error			$T_a = 25^\circ\text{C}$ $V_{DD} = 5.0\text{V}$ $V_{SS} = 0\text{V}$			± 1	LSB
Zero transition voltage	V_{ZT}^{*1}			-10	160	320	mV
Full-scale transition voltage	V_{FT}^{*2}			4370	4530	4690	mV
Conversion time	t_{CONV}			$160/f_c$			μs
Sampling time	t_{SAMP}			$12/f_c$			μs
Analog input voltage	V_{IAN}	AN0 to AN3		0		V_{DD}	V



- *1 V_{ZT} : Value at which the digital conversion value changes from 0H to 1H and vice versa.
- *2 V_{FT} : Value at which the digital conversion value changes from EH to FH and vice versa.

Fig. 8. Definition of A/D converter terms

Note) The 4-bit conversion specifies values based on the upper 5 bits of the A/D data register (ADD: Address 00F5H), compensated into 4-bit data. A program example is shown below:

(A/D converter program example)

```

MOV    A, ADD    ; ACC ← conversion data
LSR    A         ; Shift to the right (4 times)
LSR    A         ;
LSR    A         ;
LSR    A         ;
ADC    A, #00H   ; Addition with carry (data increment if AD3 = 1)
CMP    A, #10H   ;
BNE    ADC_SKIP ;
MOV    A, #0FH   ;
    
```

ADC_SKIP:

(6) I²C bus timing

(Ta = -10 to +75°C, V_{DD} = 4.5 to 5.5V, V_{SS} = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
SCL clock frequency	f _{SCL}	SCL		0	100	kHz
Bus free time prior to transfer start	t _{BUF}	SDA, SCL		4.7		μs
Transfer start hold time	t _{HD; STA}	SDA, SCL		4.0		μs
Clock Low level width	t _{LOW}	SCL		4.7		μs
Clock High level width	t _{HIGH}	SCL		4.0		μs
Setup time during repetitive transfer	t _{SU; STA}	SDA, SCL		4.7		μs
Data hold time	t _{HD; DAT}	SDA, SCL		0*1		μs
Data setup time	t _{SU; DAT}	SDA, SCL		250		ns
SDA, SCL rise time	t _R	SDA, SCL			1	μs
SDA, SCL fall time	t _F	SDA, SCL			300	ns
Transfer end setup time	t _{SU; STO}	SDA, SCL		4.7		μs

*1 The data hold time does not take into consideration SCL rise time (300ns max.). Ensure that the data hold time exceeds 300ns.

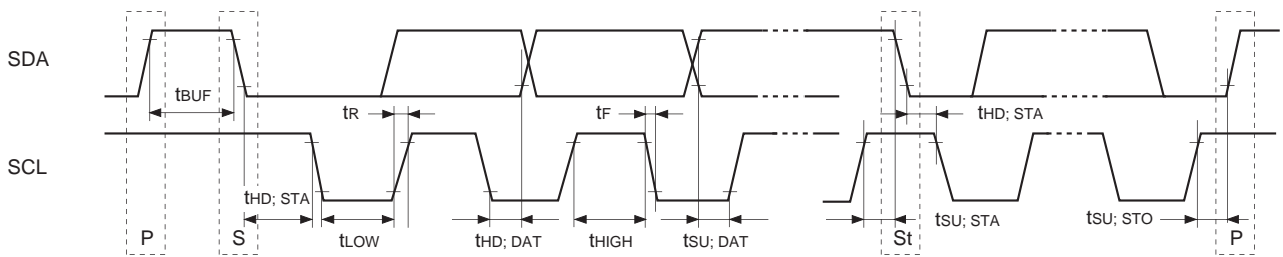


Fig. 9. I²C bus transfer timing

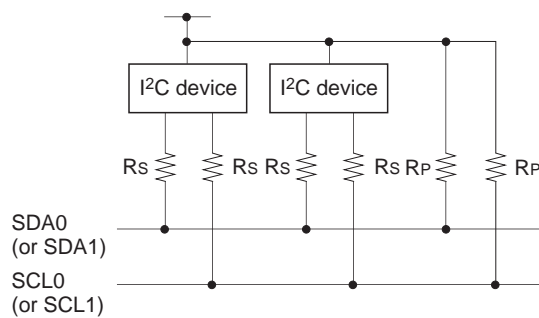


Fig. 10. Recommended circuit example for I²C device

- Pull-up resistors must be connected to SDA0 (or SDA1) and SCL0 (or SCL1).
- Serial resistance (R_s = 300Ω and under) of SDA0 (or SDA1) and SCL0 (or SCL1) reduces spike noise caused by CRT flashover.

(7) OSD (On-Screen Display) timing

($T_a = -10$ to $+75^\circ\text{C}$, $V_{DD} = 4.5$ to 5.5V , $V_{SS} = 0\text{V}$ reference)

Item	Symbol	Pins	Condition	Min.	Max.	Unit
OSD clock frequency	f_{osc}	EXLC XLC	Fig. 12	4	13	MHz
HSYNC pulse width	t_{HWD}	HSYNC	Fig. 11	1.2		μs
HSYNC after-edge rise time/fall time	t_{HCG}	HSYNC	Fig. 11		200	ns
VSYNC after-edge rise time/fall time	t_{VCG}	VSYNC	Fig. 11		1.0	μs

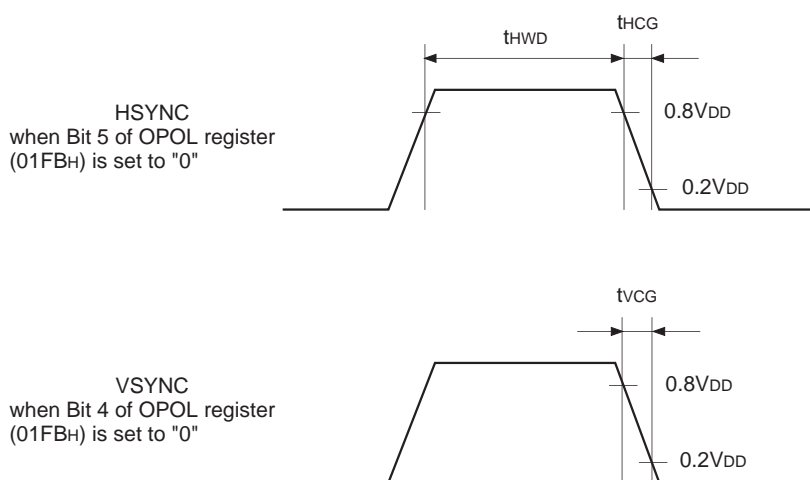


Fig. 11. OSC timing

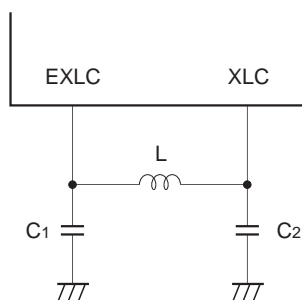


Fig. 12. LC oscillation circuit example

Supplement



Fig. 13. Recommended Oscillation circuit

Manufacturer	Model	fc (MHz)	C1 (pF)	C2 (pF)	Rd (Ω)	Circuit example
MURATA MFG CO., LTD.	CSA4.00MG	4.00	30	30	0	(i)
	CSA4.19MG	4.19				
	CST4.00MGW*	4.00				(ii)
	CST4.19MGW*	4.19				
RIVER ELETEC CORPORATION	HC-49/U03	4.00	10	10	0	(i)
		4.19				
KINSEKI LTD.	HC-49/U (-S)	4.00	18	18	0	
		4.19				

* Indicates types with on-chip grounding capacitance (C1 and C2).

Product List

Option item	Mask	CXP852P32AS-1-□□□	CXP852P32AQ-1-□□□
Package	64-pin plastic SDIP/QFP	64-pin plastic SDIP	64-pin plastic QFP
PROM capacitance	12K/16K bytes (CXP85112B/85116B) 20K/24K/28K/32K bytes (CXP85220A/85224A /85228A/85232A)	PROM 32K bytes	PROM 32K bytes
Reset pin pull-up resistor	Existent/Non-existent	Existent	Existent
Power-on reset circuit	Existent/Non-existent	Existent	Existent
Font data	User specified	User specified (PROM)*1	User specified (PROM)*1

*1 The font data for the one-time PROM version is operated in the same way as the program writing.

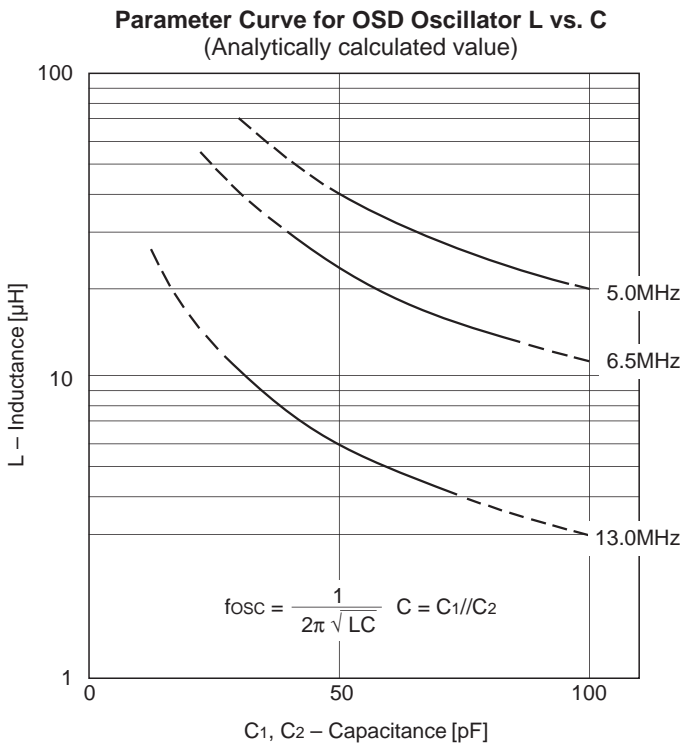
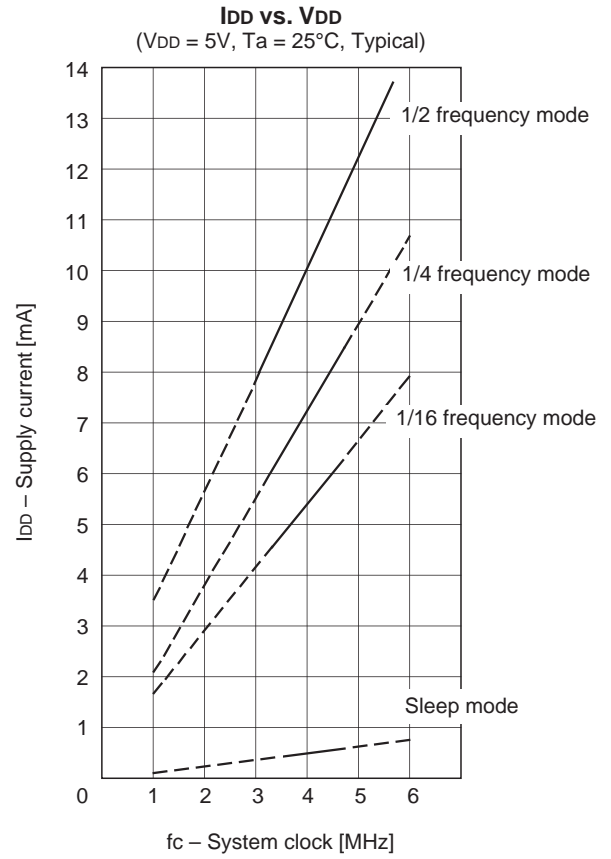
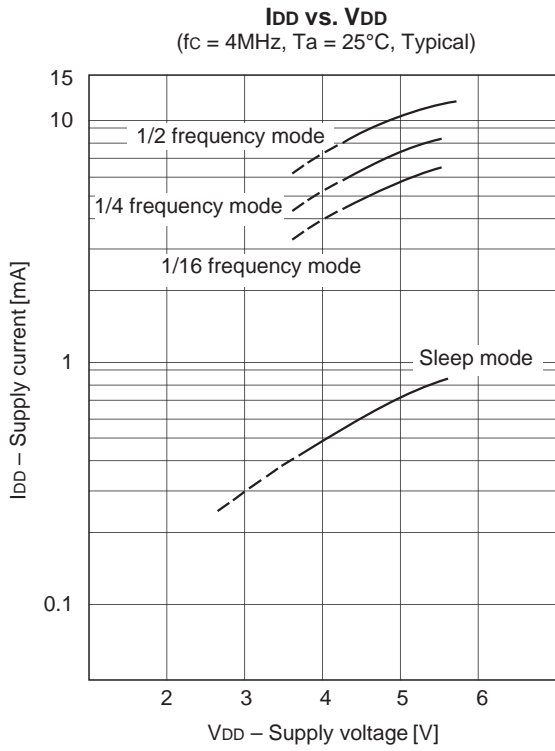
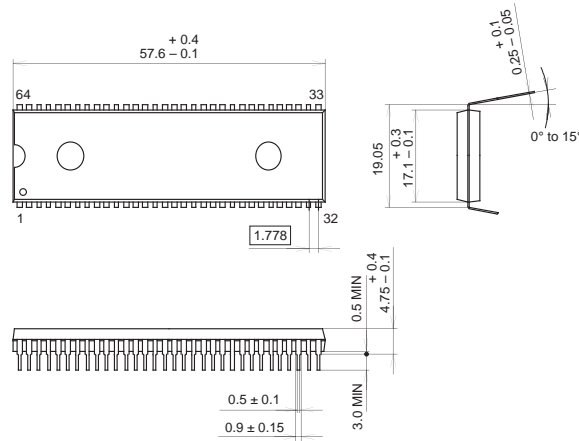


Fig. 14. Characteristics curves

Package Outline

Unit: mm

64PIN SDIP (PLASTIC)

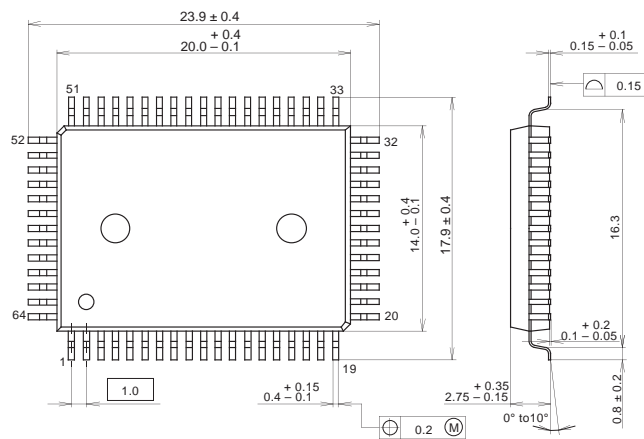


PACKAGE STRUCTURE

SONY CODE	SDIP-64P-01
EIAJ CODE	SDIP064-P-0750
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	8.6g

64PIN QFP(PLASTIC)



PACKAGE STRUCTURE

SONY CODE	QFP-64P-L01
EIAJ CODE	QFP064-P-1420
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.5g