SONY

CXP873P60

CMOS 8-bit Single Chip Microcomputer

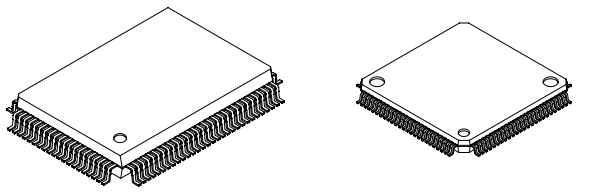
Description

The CXP873P60 is a CMOS 8-bit micro-computer which consists of A/D converter, serial interface, timer/counter, time base timer, vector interruption, high precision timing pattern generation circuit, PWM generator, PWM for tuner, VISS/VASS circuit, 32kHz timer/event counter, remote control receiving circuit, general purpose prescaler, HSYNC counter, VCR vertical sync separation circuit and the measurement circuit which measure signals of capstan FG and drum FG/PG and other servo systems, as well as basic configurations like 8-bit CPU, PROM, RAM and I/O port. They are integrated into a single chip.

Also the CXP873P60 provides sleep/stop function which enables to lower power consumption and ultra-low speed instruction mode in 32kHz operation.

Incorporating a one-time PROM, the CXP873P60 has an equivalent function to the CXP87360, and is suitable for evaluation in system development and for the production of small amounts.

100 pin QFP (PIastic) 100 pin LQFP (PIastic)



Structure

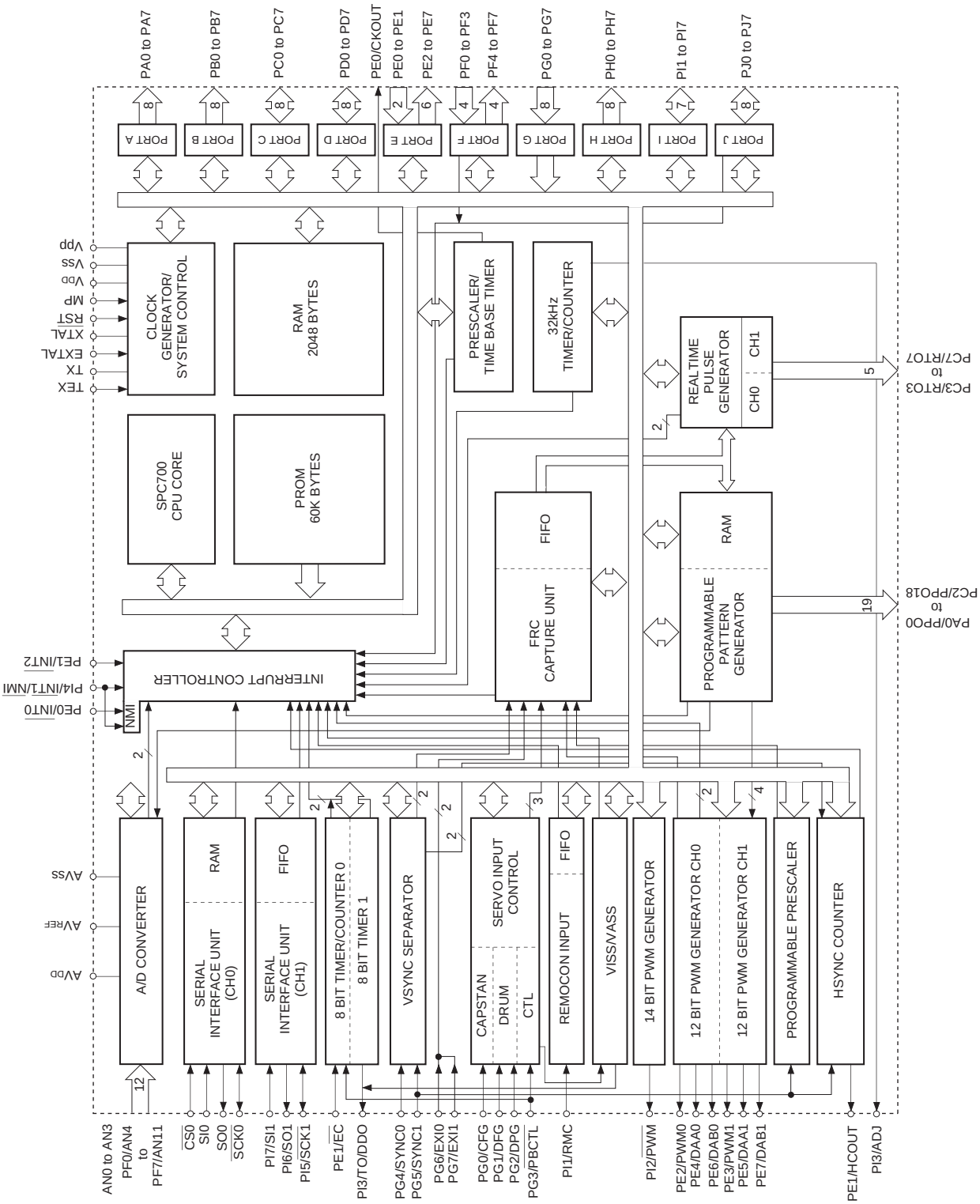
Silicon gate CMOS IC

Features

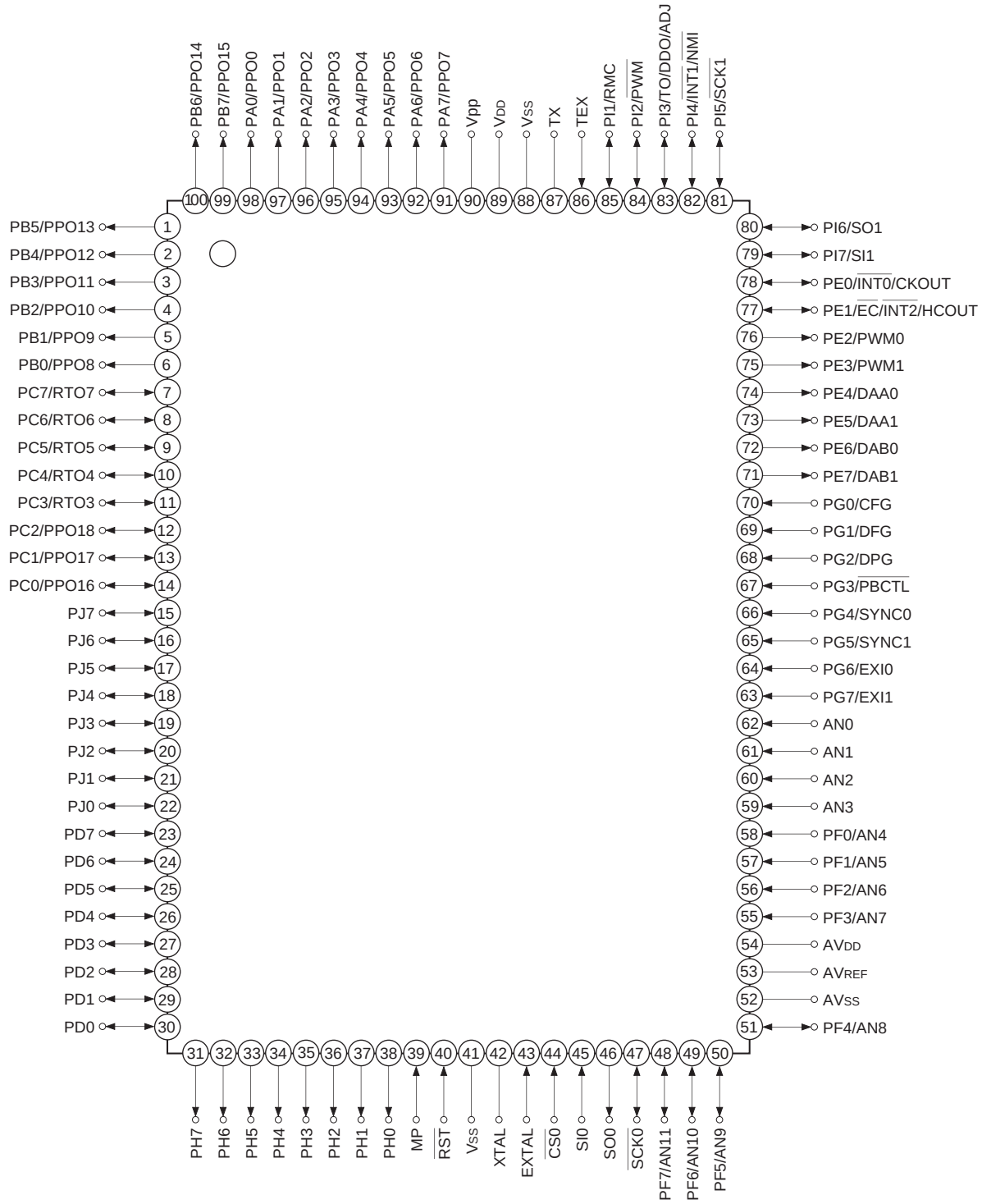
- A wide instruction set (213 instructions) which cover various types of data
  — 16-bit arithmetic/multiplication and division/boolean bit operation instructions
- Minimum instruction cycle 250ns at 16MHz operation (4.5V to 5.5V)
  333ns at 12MHz operation (3.0V to 5.5V)
  122µs at 32kHz operation
- Incorporated PROM capacity 60K bytes
- Incorporated RAM capacity 2048 bytes
- Peripheral functions
  - — A/D converter: 8-bit, 12-channel, successive approximation system (Conversion time 20.0µs/16MHz)
  - — Serial interface: Incorporated buffer RAM (1 to 32 bytes auto transfer) 1-channel; Incorporated 8-bit and 8-stage FIFO for data (1 to 8 bytes auto transfer) 1-channel
  - — Timer: 8-bit timer, 8-bit timer/counter, 19-bit time base timer, 32kHz timer/counter
  - — High precision timing pattern generator: PPG 19-pin 32-stage programmable; RTG 5-pin 2-channel
  - — PWM/DA gate output: PWM 12-bit, 2-channel (Repetitive frequency 62kHz/16MHz); DA gate pulse output 13-bit, 4-channel
  - — Servo input control: Capstan FG, Drum FG/PG, CTL input
  - — VSYNC separator
  - — FRC capture unit: Incorporated 26-bit and 8-stage FIFO
  - — PWM output: 14-bit, 1-channel
  - — VISS/VASS circuit: Pulse duty auto detection circuit
  - — Remote control receiving circuit: 8-bit pulse measurement counter with on-chip, 6-stage FIFO
  - — General purpose prescaler: 7-bit (SYNC1 input frequency divided, FRC capture possible)
  - — HSYNC counter: 12-bit event counter (Counts SYNC1 input.)
- Interruption: 21 factors, 15 vectors, multi-interruption possible
- Standby mode: SLEEP/STOP
- Package: 100-pin plastic QFP/LQFP

E95106-ST

Block Diagram



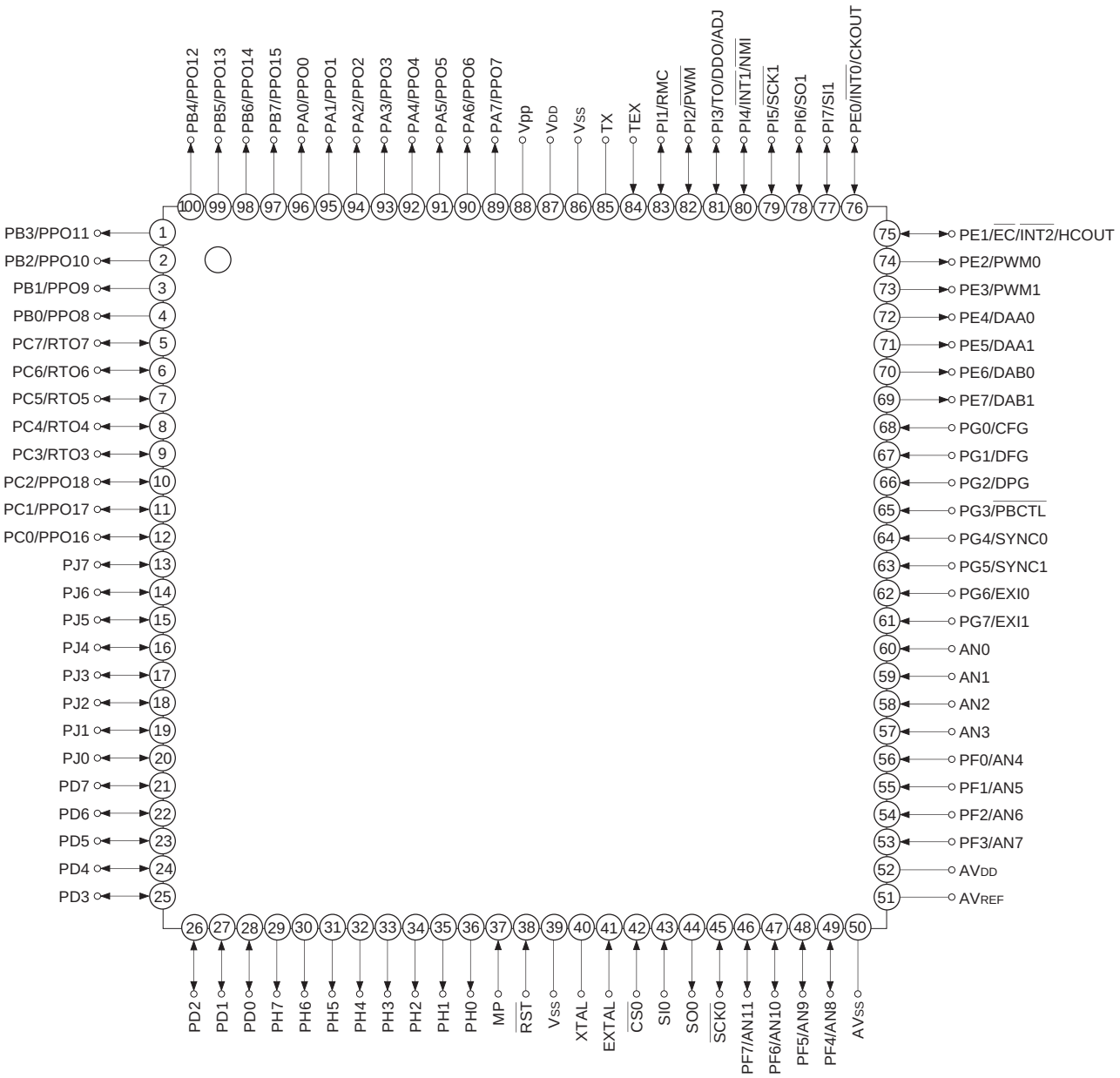
Pin Configuration 1 (Top View) 100-pin QFP package



Note) 1. Vpp (Pin 90) is always connected to V_{DD}.

2. Vss (Pins 41 and 88) are both connected to GND.

Pin Configuration 2 (Top View) 100-pin LQFP package



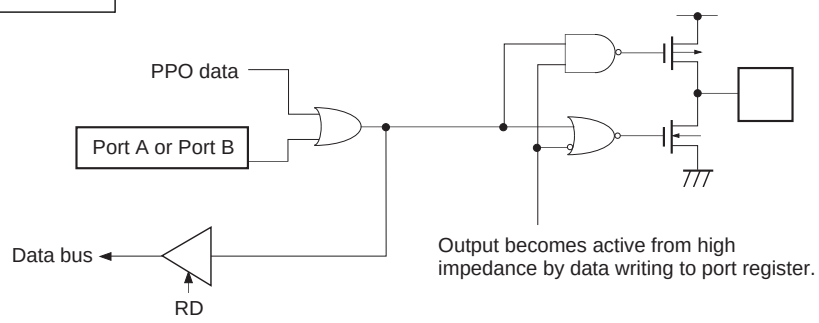
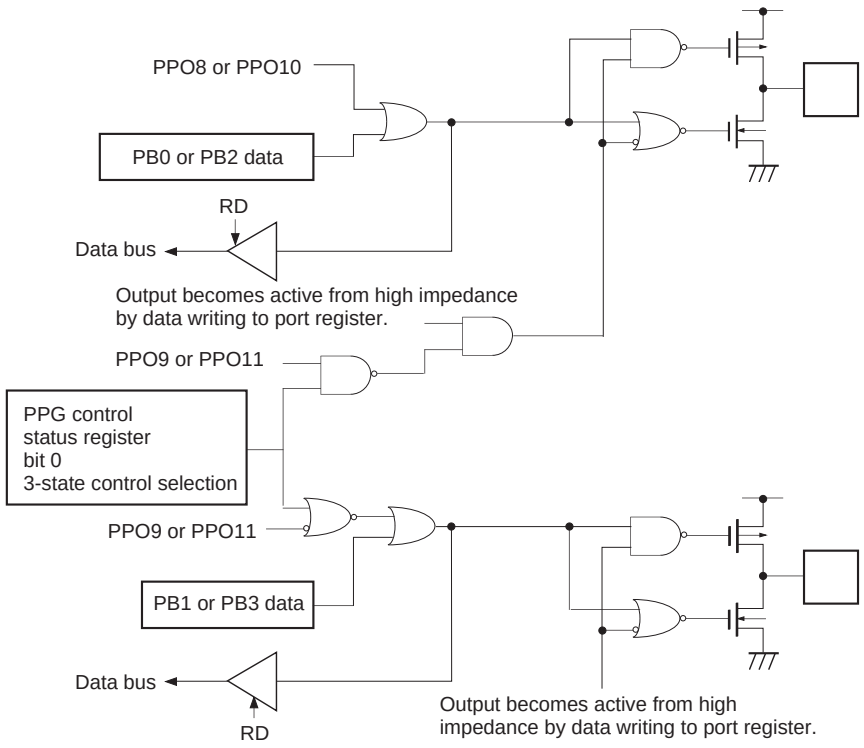
Note) 1. Vpp (Pin 88) is always connected to V_{DD}.
2. Vss (Pins 39 and 86) are both connected to GND.

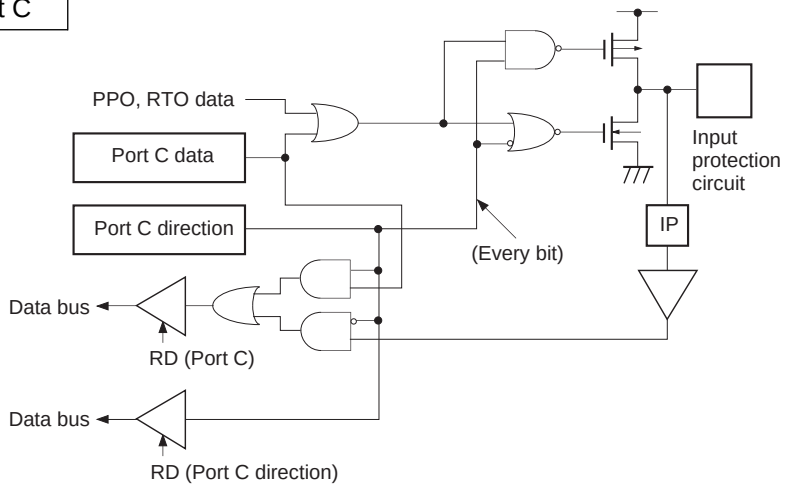
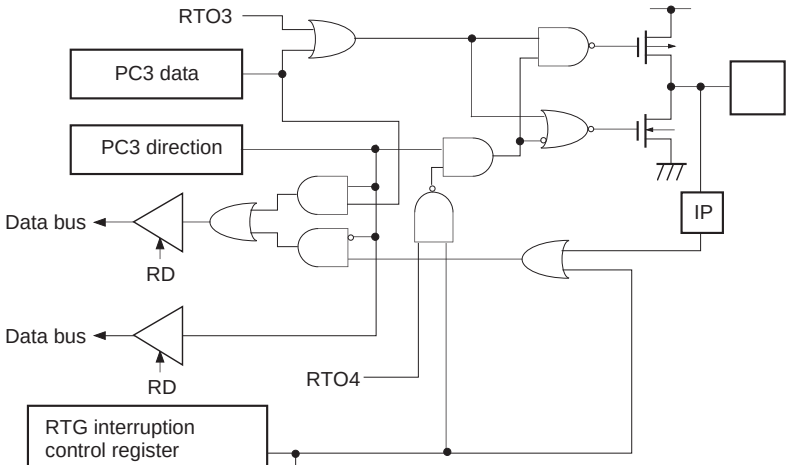
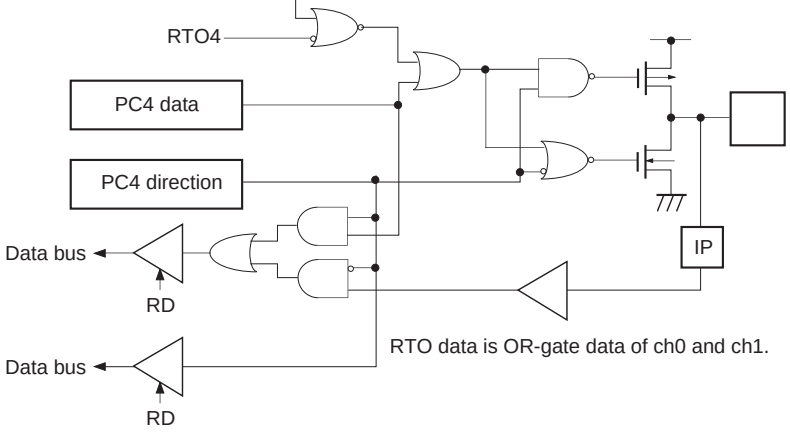
Pin Description

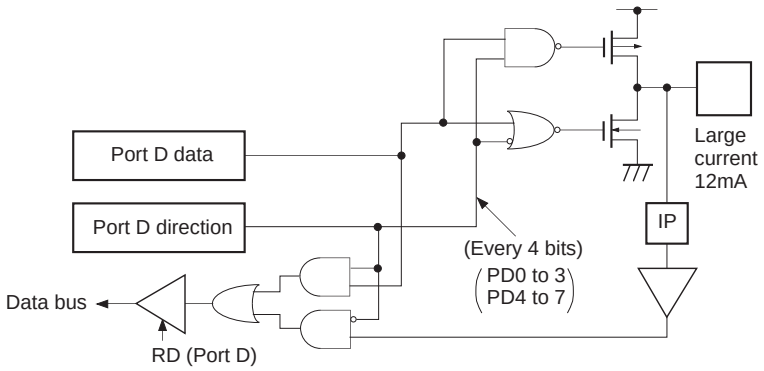
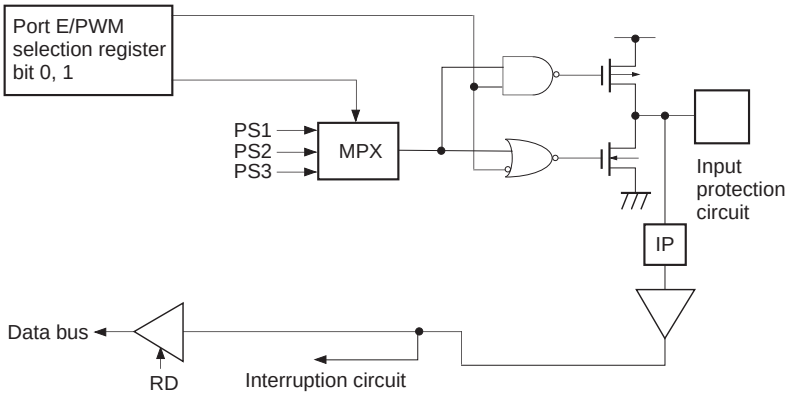
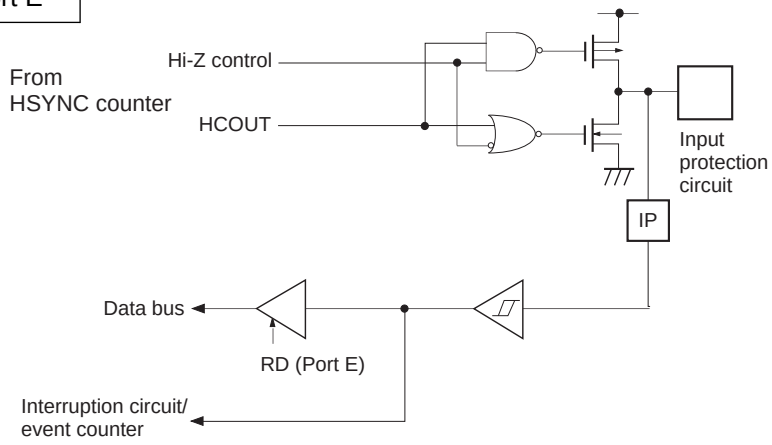
<table>
<tr><th>Symbol</th><th>I/O</th><th colspan="4">Description</th></tr>
<tr><td>PA0/PPO0
to
PA7/PPO7</td><td>Output/
Real time
output</td><td colspan="2">(Port A)
8-bit output port. Data is gated with PPO contents by OR-gate and they are output.
(8 pins)</td><td rowspan="2">Programmable pattern generator (PPG) output.
Functions as high precision real time pulse output port.
(19 pins)
PB0 and PB2 can be 3-state controlled with PPG.</td></tr>
<tr><td>PB0/PPO8
to
PB7/PPO15</td><td>Output/
Real time
output</td><td colspan="2">(Port B)
8-bit output port. Data is gated with PPO contents by OR-gate and they are output.
(8 pins)</td></tr>
<tr><td>PC0/PPO16
to
PC2/PPO18</td><td>I/O/
Real time
output</td><td colspan="2" rowspan="2">(Port C)
8-bit I/O port, enables to specify I/O by bit unit.
Data is gated with PPO or RTO contents by OR-gate and they are output.
(8 pins)</td><td rowspan="2">Real time pulse generator (RTG) output.
Functions as high precision real time pulse output port. (5 pins)</td></tr>
<tr><td>PC3/RTO3
to
PC7/RTO7</td><td>I/O/
Real time
output</td></tr>
<tr><td>PD0 to PD7</td><td>I/O</td><td colspan="4">(Port D)
8-bit I/O port. Enable to specify I/O by 4-bit unit.
Enables to drive 12mA sink current.
(8 pins)</td></tr>
<tr><td>PE0/$\overline{\text{INT0}}$/
CKOUT</td><td>Input/Input/Output</td><td rowspan="8">(Port E)
8-bit port.
Lower 2 bits are input pins and upper 6 bits are output pins.
(8 pins)</td><td colspan="3">Input pin to request external interruption.
Active when falling edge.
PC3 can be 3-state controlled with RTG.
System clock frequency division output.</td></tr>
<tr><td>PE1/$\overline{\text{EC}}$/$\overline{\text{INT2}}$/
HCOUT</td><td>Input/Input/Input/
Output</td><td>External event input pin for timer/counter.</td><td>Input pin to request external interruption.
Active when falling edge.</td><td>Coinsidence signal output of HSYNC counter.</td></tr>
<tr><td>PE2/PWM0</td><td>Output/Output</td><td colspan="3" rowspan="2">PWM output pins.
(2 pins)</td></tr>
<tr><td>PE3/PWM1</td><td>Output/Output</td></tr>
<tr><td>PE4/DAA0</td><td>Output/Output</td><td colspan="3" rowspan="4">DA gate pulse output pins.
(4 pins)</td></tr>
<tr><td>PE5/DAA1</td><td>Output/Output</td></tr>
<tr><td>PE6/DAB0</td><td>Output/Output</td></tr>
<tr><td>PE7/DAB1</td><td>Output/Output</td></tr>
<tr><td>AN0 to AN3</td><td>Input</td><td colspan="4">Analog input pins to A/D converter. (12 pins)</td></tr>
<tr><td>PF0/AN4
to
PF3/AN7</td><td>Input/Input</td><td colspan="4" rowspan="2">(Port F)
Lower 4 bits are input port and upper 4 bits are output port.
Lower 4 bits also serve as standby release input pin.
(8 pins)</td></tr>
<tr><td>PF4/AN8
to
PF7/AN11</td><td>Output/Input</td></tr>
<tr><td>$\overline{\text{SCK0}}$</td><td>I/O</td><td colspan="4">Serial clock (CH0) I/O pin.</td></tr>
<tr><td>SO0</td><td>Ouput</td><td colspan="4">Serial data (CH0) output pin.</td></tr>
<tr><td>SI0</td><td>Input</td><td colspan="4">Serial data (CH0) input pin.</td></tr>
<tr><td>$\overline{\text{CS0}}$</td><td>Input</td><td colspan="4">Serial chip select (CH0) input pin.</td></tr>
</table>

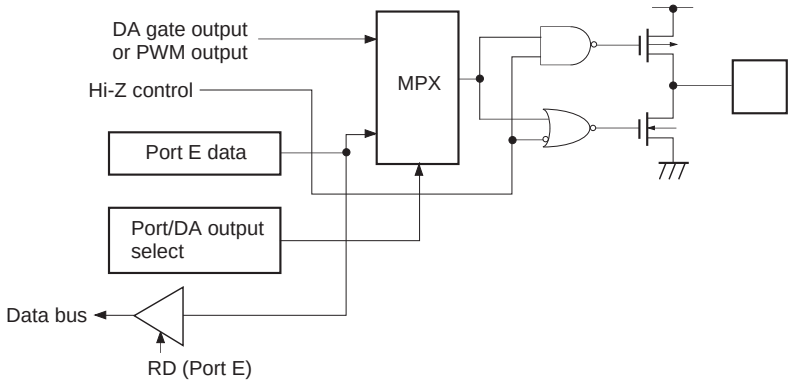
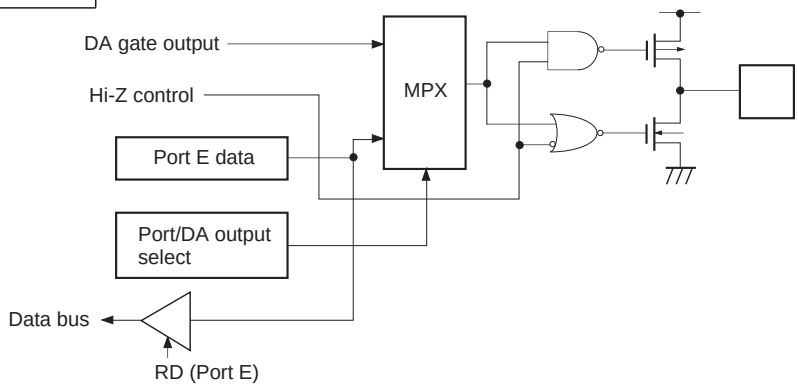
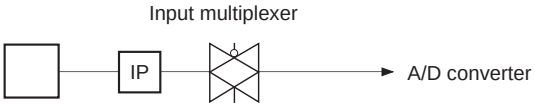
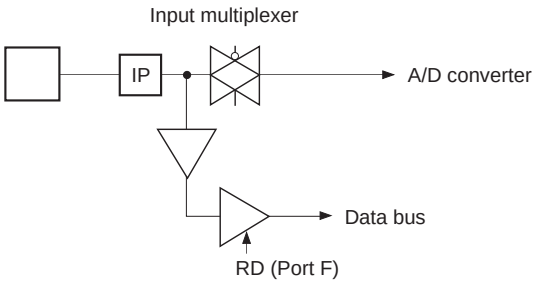
Symbol	I/O	Description	
PG0/CFG	Input/Input	(Port G) 8-bit input port. (8 pins)	Capstan FG input pin.
PG1/DFG	Input/Input		Drum FG input pin.
PG2/DPG	Input/Input		Drum PG input pin.
PG3/$\overline{\text{PBCTL}}$	Input/Input		Playback CTL pulse input pin. External event input pin of timer/counter.
PG4/SYNC0	Input/Input		Composite sync signal input pin.
PG5/SYNC1	Input/Input		
PG6/EXI0	Input/Input		External input pin to FRC capture unit.
PG7/EXI1	Input/Input		
PH0 to PH7	Output	(Port H) 8-bit output port ; Medium withstand voltage (12V) and high current (12mA), N-ch open drain output. (8 pins)	
PI1/RMC	I/O/Input	(Port I) 7-bit I/O port. I/O port can be specified by bit unit. (7 pins)	Remote control receiving circuit input pin.
PI2/$\overline{\text{PWM}}$	I/O/Output		14-bit PWM output pin.
PI3/TO/ DDO/ADJ	I/O/Output/ Output/Output		Timer/counter, CTL duty detection, 32kHz oscillation adjustment output pin.
PI4/$\overline{\text{INT1}}$/ $\overline{\text{NMI}}$	I/O/Input/Input		Input pin to request external interruption and non-maskable interruption. Active when falling edge.
PI5/$\overline{\text{SCK1}}$	I/O/I/O		Serial clock (CH1) I/O pin.
PI6/SO1	I/O/Output		Serial data (CH1) output pin.
PI7/SI1	I/O/Input		Serial data (CH1) input pin.
PJ0 to PJ7	I/O	(Port J) 8-bit I/O port. Function as standby release input can be specified by bit unit. I/O can be specified by bit unit.	
EXTAL	Input	Connecting pin of crystal oscillator for system clock. When supplying the external clock, input the external clock to EXTAL pin and input opposite phase clock to XTAL pin.	
XTAL	Output		
TEX	Input	Connecting pin of crystal oscillator for 32kHz timer clock. When used as event counter, input to TEX pin and leave TX pin open. (Feedback resistor is not removed.)	
TX	Output		
$\overline{\text{RST}}$	Input	System reset pin of active "L" level.	
MP	Input	Microprocessor mode input pin. Always connect to GND.	
AV_{DD}		Positive power supply pin of A/D converter.	
AV_{REF}	Input	Reference voltage input pin of A/D converter.	
AVss		GND pin of A/D converter.	
V_{DD}		Positive power supply pin.	
Vpp		Positive power supply pin for incorporated PROM writing. In normal operation, connect to V_{DD}.	
Vss		GND pin. Connect both Vss pins to GND.	

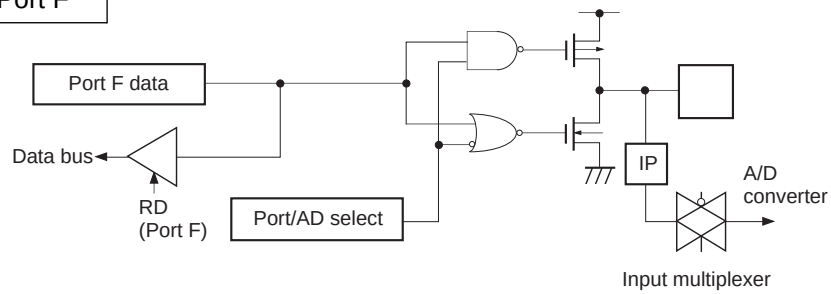
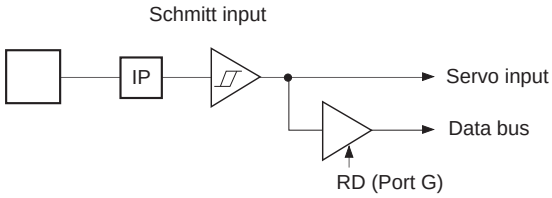
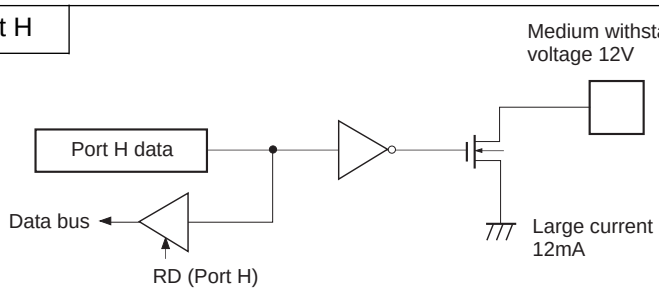
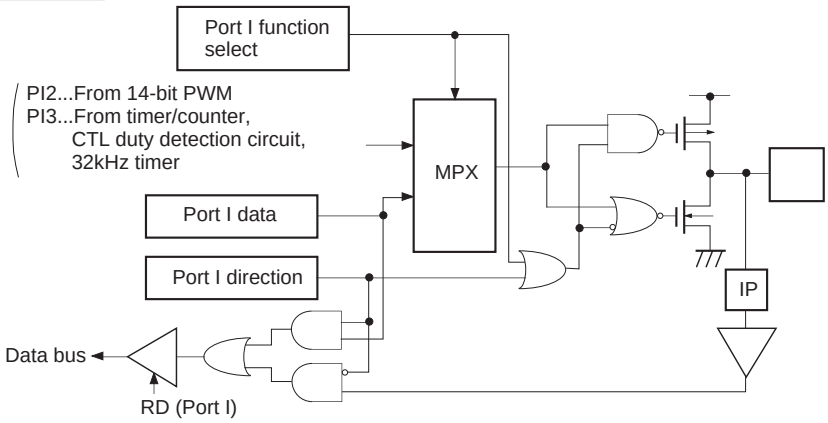
Input/Output Circuit Formats for Pins

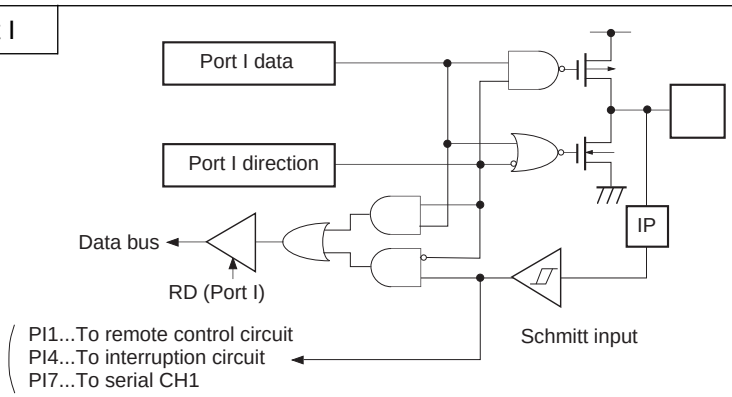
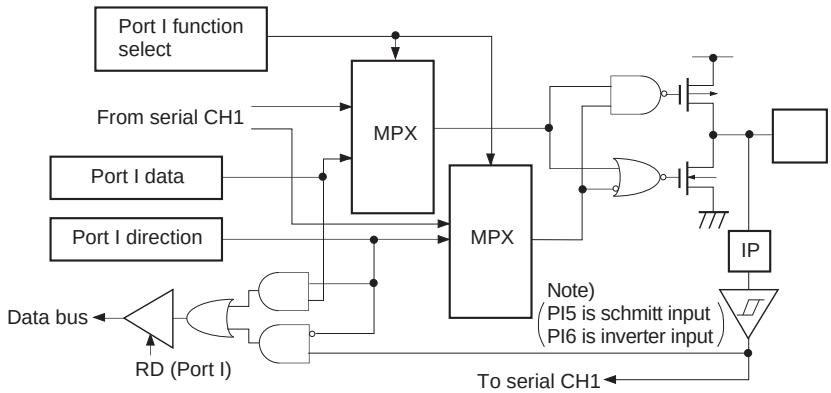
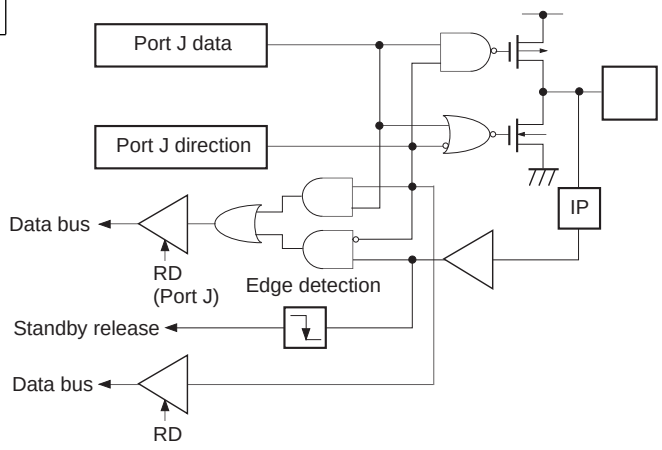
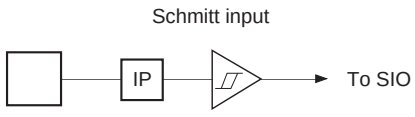
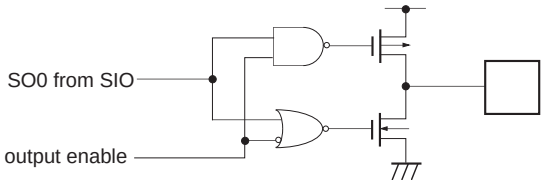
Pin	Circuit format	When reset
PA0 /PPO0 to PA7/PPO7 PB4/PPO12 to PB7/PPO15 12 pins	Port A Port B 	Hi-Z
PB0 /PPO8 PB2/PPO10 2 pins		Hi-Z
PB1/PPO9 PB3/PPO11 2 pins		Hi-Z

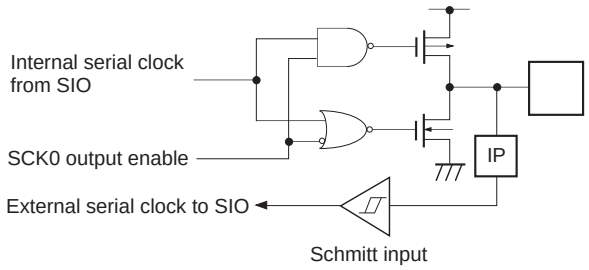
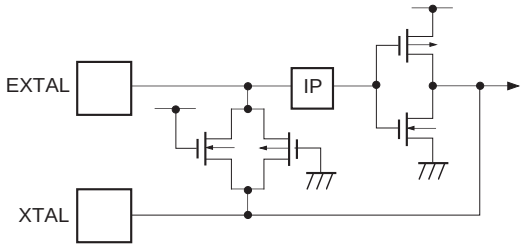
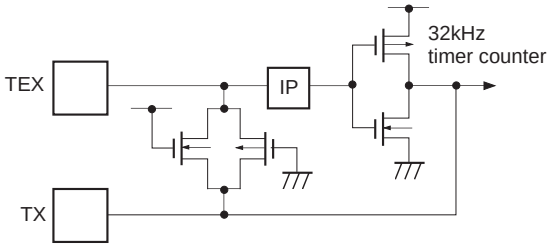
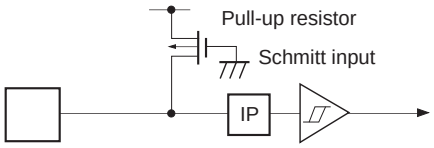
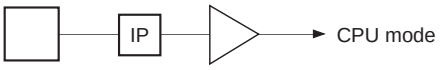
Pin	Circuit format	When reset
PC0/PPO16 to PC2/PPO18 PC5/RTO5 to PC7/RTO7 6 pins	Port C 	Hi-Z
PC3/RTO3 1 pin		Hi-Z
PC4/RTO4 1 pin		Hi-Z

Pin	Circuit format	When reset
PD0 to PD7 8 pins	Port D 	Hi-Z
PE0/$\overline{\text{INT0}}$/ CKOUT 1 pin	Port E 	Hi-Z
PE1/$\overline{\text{EC}}$/$\overline{\text{INT2}}$ 1 pin	Port E 	Hi-Z

Pin	Circuit format	When reset
PE2/PWM0 PE3/PWM1 PE4/DAA0 PE5/DAA1 4 pins	Port E 	Hi-Z
PE6/DAB0 PE7/DAB1 2 pins	Port E 	H level
AN0 to AN3 4 pins		Hi-Z
PF0/AN4 to PF3/AN7 4 pins	Port F 	Hi-Z

Pin	Circuit format	When reset
PF4/AN8 to PF7/AN11 4 pins	Port F  	Hi-Z
PG0/CFG PG1/DFG PG2/DPG PG3/$\overline{\text{PBCTL}}$ PG4/SYNC0 PG5/SYNC1 PG6/EXI0 PG7/EXI1 8 pins	Port G  Note) For PG4 and PG5 input format, there are CMOS schmitt input and TTL schmitt input with product.	Hi-Z
PH0 to PH7 8 pins	Port H  	Hi-Z
PI2/$\overline{\text{PWM}}$ PI3/TO/ DDO/ADJ 2 pins	Port I  	Hi-Z

Pin	Circuit format	When reset
PI1/RMC PI4/INT1/NMI PI7/SI1 3 pins	Port I 	Hi-Z
PI5/SCK1 PI6/SO1 2 pins	Port I 	Hi-Z
PJ0 to PJ7 8 pins	Port J 	Hi-Z
CS0 SI0 2 pins		Hi-Z
SO0 1 pin		Hi-Z

Pin	Circuit format	When reset
$\overline{\text{SCK0}}$ 1 pin		Hi-Z
EXTAL XTAL 2 pins	 • Shows the circuit composition during oscillation. • Feedback resistor is removed during stop.	Oscillation
TEX TX 2 pins	 • Shows the circuit composition during oscillation. • Feedback resistor is removed during 32kHz oscillation circuit stop by software. At this time TEX pin outputs “L” level and TX pin outputs “H” level.	Oscillation
$\overline{\text{RST}}$ 1 pin		L level
MP 1 pin		Hi-Z

Absolute Maximum Ratings (Vss=0V)

Item	Symbol	Rating	Unit	Remarks
Supply voltage	V_{DD}	–0.3 to +7.0	V	
	Vpp	–0.3 to +13	V	PROM version only
	AV_{DD}	AVss to +7.0*1	V	
	AV_{SS}	–0.3 to +0.3	V	
Input voltage	V_{IN}	–0.3 to +7.0*2	V	
Output voltage	V_{OUT}	–0.3 to +7.0*2	V	
Medium withstand output voltage	V_{OUTP}	–0.3 to +15.0	V	PH pin
High level output current	I_{OH}	–5	mA	
High level total output current	$\sum I_{OH}$	–50	mA	Total of output pins
Low level output current	I_{OL}	15	mA	Other than large current output pins: per pin
	I_{OLC}	20	mA	Large current port pin*3: per pin
Low level total output current	$\sum I_{OL}$	130	mA	Total of output pins
Operating temperature	Topr	–10 to +75	°C	
Storage temperature	Tstg	–55 to +150	°C	
Allowable power dissipation	P_D	600	mW	QFP package type
		380		LQFP package type

*1) AV_{DD} and V_{DD} should be set to a same voltage.

*2) V_{IN} and V_{OUT} should not exceed V_{DD}+0.3V.

*3) The large current operation transistors are the N-CH transistors of the PD and PH ports.

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should better take place under the recommended operating conditions. Exceeding those conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions (Vss=0V)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V_{DD}	3.0	5.5	V	Guaranteed range during high speed mode (1/2 dividing clock) operation
		2.7	5.5	V	Guaranteed range during low speed mode (1/16 dividing clock) operation
		2.7	5.5	V	Guaranteed operation range by TEX clock
		2.0	5.5	V	Guaranteed data hold operation range during STOP
Analog power supply	AV_{DD}	3.0	5.5	V	*1
High level input voltage	V_{IH}	$0.7V_{DD}$	V_{DD}	V	*2
	V_{IHS}	$0.8V_{DD}$	V_{DD}	V	CMOS schmitt input*3 and PE0/$\overline{INT0}$ pin
			5.5	V	CMOS schmitt input*7
	V_{IHTS}	2.2	5.5	V	TTL schmitt input*4
	V_{IHEX}	V_{DD}–0.4	V_{DD}+0.3	V	EXTAL pin*5, *8 and TEX pin*6, *8
		V_{DD}–0.2	V_{DD}+0.2	V	EXTAL pin*5, *9 and TEX pin*6, *9
Low level input voltage	V_{IL}	0	$0.3V_{DD}$	V	*2, *8
		0	$0.2V_{DD}$	V	*2, *9
	V_{ILS}	0	$0.2V_{DD}$	V	CMOS schmitt input*3 and PE0/$\overline{INT0}$ pin
	V_{ILTS}	0	0.8	V	TTL schmitt input*4
	V_{ILEX}	–0.3	0.4	V	EXTAL pin*5, *8 and TEX pin*6, *8
		–0.3	0.2	V	EXTAL pin*5, *9 and TEX pin*6, *9
Operating temperature	Topr	–10	+75	°C	

*1) AV_{DD} and V_{DD} should be set to a same voltage.

*2) Normal input port (each pin of PC, PD, PF0 to PF3, PG, PI and PJ), MP pin.

*3) Each pin of $\overline{SCK0}$, $\overline{RST}$, PE1/$\overline{EC}$/$\overline{INT2}$, PI1/RMC, PI4/$\overline{INT1}$/$\overline{NMI}$, PI5/$\overline{SCK1}$ and PI7/SI1.

*4) Each pin of PG4 and PG5 (When TTL schmitt input is selected for the product)

*5) It specifies only when the external clock is input.

*6) It specifies only when the external event count clock is input.

*7) Each pin of $\overline{CS0}$, SI0, and PG (For PG4 and PG5, when CMOS schmitt input is selected for the product.)

*8) In case of 4.5 to 5.5V supply voltage (V_{DD}).

*9) In case of 3.0 to 3.6V supply voltage (V_{DD}).

Electrical Characteristics

DC Characteristics (V_{DD} = 4.5 to 5.5V) (Ta=–10 to +75°C, Vss=0V)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output voltage	V_{OH}	PA to PD, PE2 to PE7, PF4 to PF7, PH (V_{OL} only) PI1 to PI7 PJ, SO0, $\overline{SCK0}$	V_{DD}=4.5V, I_{OH}=–0.5mA	4.0			V
			V_{DD}=4.5V, I_{OH}=–1.2mA	3.5			V
Low level output voltage	V_{OL}		V_{DD}=4.5V, I_{OL}=1.8mA			0.4	V
			V_{DD}=4.5V, I_{OL}=3.6mA			0.6	V
		PD, PH	V_{DD}=4.5V, I_{OL}=12.0mA			1.5	V
Input current	I_{IHE}	EXTAL	V_{DD}=5.5V, V_{IH}=5.5V	0.5		40	µA
	I_{ILE}		V_{DD}=5.5V, V_{IL}=0.4V	–0.5		–40	µA
	I_{IHT}	TEX	V_{DD}=5.5V, V_{IH}=5.5V	0.1		10	µA
	I_{ILT}		V_{DD}=5.5V, V_{IL}=0.4V	–0.1		–10	µA
	I_{ILR}	$\overline{RST}$		–1.5		–400	µA
I/O leakage current	I_{IZ}	PA to PG, PI, PJ, MP AN0 to AN3, $\overline{CS0}$, SI0, SO0 $\overline{SCK0}$	V_{DD}=5.5V, V_I=0, 5.5V			±10	µA
Open drain output leakage current (N-CH Tr OFF in state)	I_{LOH}	PH	V_{DD}=5.5V V_{OH}=12V			50	µA
Supply current*1	I_{DD1}	V_{DD}	16MHz crystal oscillation (C_1=C_2=15pF) V_{DD}=5V±0.5V*2		28	50	mA
	I_{DDS1}		SLEEP mode V_{DD}=5V±0.5V		1.7	8	mA
	I_{DD2}		32kHz crystal oscillation (C_1=C_2=47pF) V_{DD}=3V±0.3V		0.7	2	mA
	I_{DDS2}		SLEEP mode V_{DD}=3V±0.3V		8	35	µA
	I_{DDS3}		STOP mode (EXTAL and TEX pins oscillation stop) V_{DD}=5V±0.5V			30	µA
Input capacity	C_{IN}	Other than V_{DD}, Vss, AV_{DD}, and AVss	Clock 1MHz 0V other than the measured pins		10	20	pF

*1) When entire output pins are open.

*2) When setting upper 2 bits (CPU clock selection) of clock control register CLC (address: 00FE$_H$) to "00" and operating in high speed mode (1/2 dividing clock).

DC Characteristics (V_{DD}=3.0 to 3.6V) (Ta=–10 to +75°C, Vss=0V)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output voltage	V_{OH}	PA to PD, PE2 to PE7, PF4 to PF7, PH (V_{OL} only) PI1 to PI7 PJ, SO0, $\overline{SCK0}$	V_{DD}=3.0V, I_{OH}=–0.15mA	2.7			V
			V_{DD}=3.0V, I_{OH}=0.5mA	2.3			V
Low level output voltage	V_{OL}		V_{DD}=3.0V, I_{OL}=1.2mA			0.3	V
			V_{DD}=3.0V, I_{OL}=1.6mA			0.5	V
		PD, PH	V_{DD}=3.0V, I_{OL}=5mA			1.0	V
Input current	I_{IHE}	EXTAL	V_{DD}=3.6V, V_{IH}=3.6V	0.3		20	µA
	I_{ILE}		V_{DD}=3.6V, V_{IL}=0.3V	–0.3		–20	µA
	I_{IHT}	TEX	V_{DD}=3.6V, V_{IH}=3.6V	0.1		10	µA
	I_{ILT}		V_{DD}=3.6V, V_{IL}=0.3V	–0.1		–10	µA
	I_{ILR}	$\overline{RST}$		–0.9		–200	µA
I/O leakage current	I_{IZ}	PA to PG, PI, PJ, MP AN0 to AN3, $\overline{CS0}$, SI0, SO0 $\overline{SCK0}$	V_{DD}=3.6V, V_I=0, 3.6V			±10	µA
Open drain output leakage current	I_{LOH}	PH	V_{DD}=3.6V, V_{OH}=12V			50	µA
Supply current*1	I_{DD1}	V_{DD}	12MHz crystal oscillation (C_1=C_2=15pF) V_{DD}=3.3V±0.3V*2		12	30	mA
	I_{DDS1}		SLEEP mode V_{DD}=3.3V±0.3V		0.8	2.5	mA
	I_{DDS3}		STOP mode (EXTAL and TEX pins oscillation stop) V_{DD}=3.3V±0.3V			30	µA
Input capacity	C_{IN}	Other than V_{DD}, Vss, AV_{DD}, and AVss	Clock 1MHz 0V other than the measured pins		10	20	pF

*1) When entire output pins are open.

*2) When setting upper 2 bits (CPU clock selection) of clock control register CLC (address: 00FE$_H$) to "00" and operating in high speed mode (1/2 dividing clock).

AC Characteristics

(1) Clock timing

(Ta=–10 to +75°C, V_{DD}=3.0 to 5.5V, Vss=0V)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
System clock frequency	f_C	XTAL EXTAL	Fig. 1, V_{DD} = 4.5 to 5.5V	1	16	MHz
			Fig. 2	1	12	
System clock input pulse width	t_{XL}, t_{XH}	XTAL EXTAL	Fig. 1, V_{DD} = 4.5 to 5.5V	28		ns
			Fig. 2 (External clock drive)	37.5		
System clock input rise and fall times	t_{CR}, t_{CF}	XTAL EXTAL	Fig. 1, Fig. 2 (External clock drive)		200	ns
Event count clock input pulse width	t_{EH}, t_{EL}	$\overline{EC}$	Fig. 3	tsys x 4*		ns
Event count clock input rise and fall times	t_{ER}, t_{EF}	$\overline{EC}$	Fig. 3		20	ns
System clock frequency	f_C	TEX TX	Fig. 2 V_{DD}=2.7 to 5.5V (32kHz clock applied condition)	32.768		kHz
Event count clock input pulse width	t_{TL}, t_{TH}	TEX	Fig. 3	10		µs
Event count clock input rise and fall times	t_{TR}, t_{TF}	TEX	Fig. 3		20	ms

* tsys indicates three values according to the contents of the clock control register (address; 00FE$_H$) upper 2 bits (CPU clock selection).
tsys [ns]=2000/fc (Upper 2 bits="00"), 4000/fc (Upper 2 bits="01"), 16000/fc (Upper 2 bits="11")

Fig. 1. Clock timing

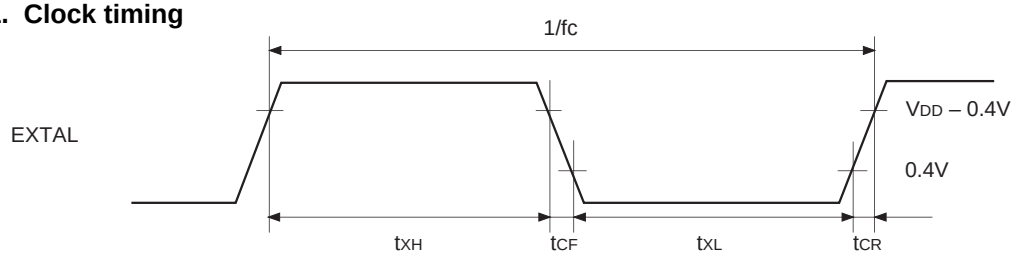


Fig. 2. Clock applied condition

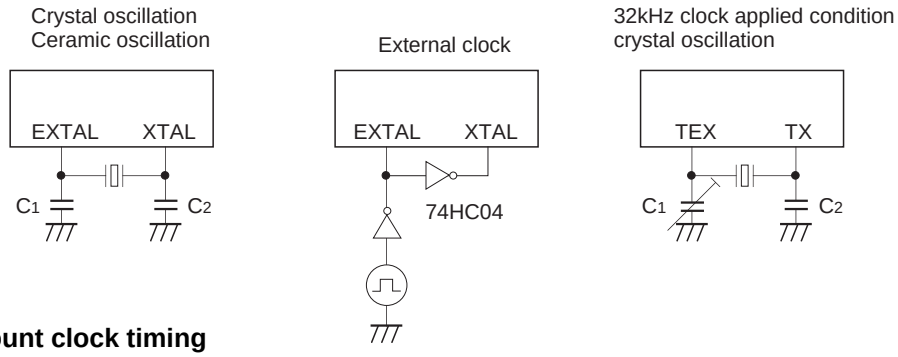
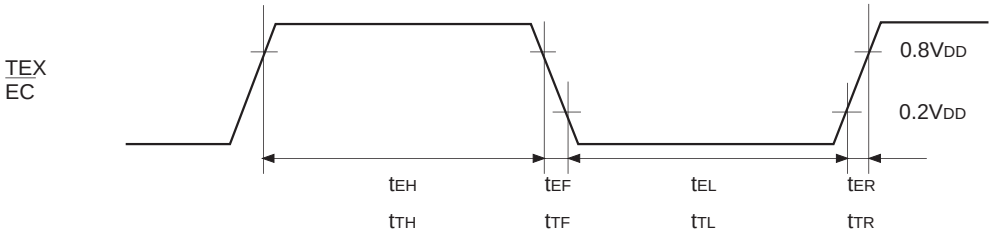


Fig. 3. Event count clock timing



(2) Serial transfer (CH0) (Ta=–10 to +75°C, V_{DD}=4.5 to 5.5V, Vss=0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{CS}\downarrow\rightarrow\overline{SCK}$ delay time	t_{DCSK}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK}$=output mode)		tsys+200	ns
$\overline{CS}\uparrow\rightarrow\overline{SCK}$ floating delay time	t_{DCSKF}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK}$=output mode)		tsys+200	ns
$\overline{CS}\downarrow\rightarrow$ SO delay time	t_{DCSO}	SO0	Chip select transfer mode		tsys+200	ns
$\overline{CS}\downarrow\rightarrow$ SO floating delay time	t_{DCSOF}	SO0	Chip select transfer mode		tsys+200	ns
$\overline{CS}$ high level width	t_{WHCS}	$\overline{CS0}$	Chip select transfer mode	tsys+200		ns
$\overline{SCK}$ cycle time	t_{KCY}	$\overline{SCK0}$	Input mode	2tsys+200		ns
			Output mode	8000/fc		ns
$\overline{SCK}$ high and low level widths	t_{KH} t_{KL}	$\overline{SCK0}$	Input mode	tsys+100		ns
			Output mode	8000/fc–100		ns
SI input setup time (against $\overline{SCK}\uparrow$)	t_{SIK}	SI0	$\overline{SCK}$ input mode	–tsys+100		ns
			$\overline{SCK}$ output mode	200		ns
SI input hold time (against $\overline{SCK}\uparrow$)	t_{KSI}	SI0	$\overline{SCK}$ input mode	2tsys+100		ns
			$\overline{SCK}$ output mode	100		ns
$\overline{SCK}\downarrow\rightarrow$ SO delay time	t_{KSO}	SO0	$\overline{SCK}$ input mode		2tsys+200	ns
			$\overline{SCK}$ output mode		100	ns

Note 1) tsys indicates three values according to the contents of the clock control register (address; 00FE$_H$) upper 2 bits (CPU clock selection).
tsys [ns]=2000/fc (Upper 2 bits="00"), 4000/fc (Upper 2 bits="01"), 16000/fc (Upper 2 bits="11")

Note 2) $\overline{CS}$, $\overline{SCK}$, SI and SO means each pin of $\overline{CS}\rightarrow\overline{CS0}$, $\overline{SCK}\rightarrow$ SCK0, SI $\rightarrow$ SI0, and SO $\rightarrow$ SO0 respectively.

Note 3) The load of $\overline{SCK}$ output mode and SO output delay time is 50pF+1TTL.

Serial transfer (CH0) (Ta=–10 to +75°C, V_{DD}=3.0 to 3.6V, Vss=0V)

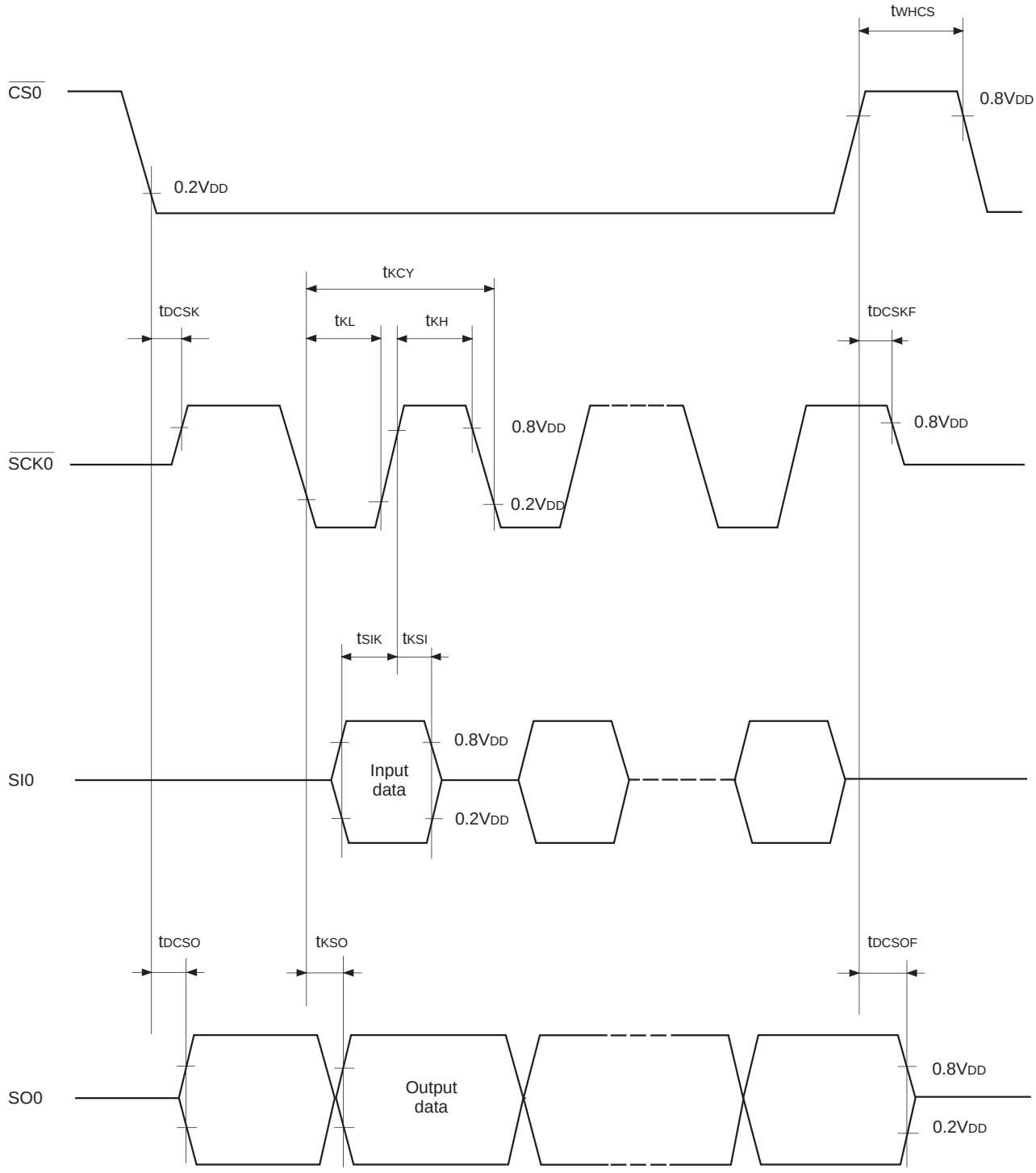
Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{CS}\downarrow\rightarrow\overline{SCK}$ delay time	t_{DCSK}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK}$=output mode)		tsys+250	ns
$\overline{CS}\uparrow\rightarrow\overline{SCK}$ floating delay time	t_{DCSKF}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK}$=output mode)		tsys+200	ns
$\overline{CS}\downarrow\rightarrow$ SO delay time	t_{DCSO}	SO0	Chip select transfer mode		tsys+250	ns
$\overline{CS}\downarrow\rightarrow$ SO floating delay time	t_{DCSOF}	SO0	Chip select transfer mode		tsys+200	ns
$\overline{CS}$ high level width	t_{WHCS}	$\overline{CS0}$	Chip select transfer mode	tsys+200		ns
$\overline{SCK}$ cycle time	t_{KCY}	$\overline{SCK0}$	Input mode	2tsys+200		ns
			Output mode	8000/fc		ns
$\overline{SCK}$ high and low level widths	t_{KH} t_{KL}	$\overline{SCK0}$	Input mode	tsys+100		ns
			Output mode	8000/fc–150		ns
SI input setup time (against $\overline{SCK}\uparrow$)	t_{SIK}	SI0	$\overline{SCK}$ input mode	–tsys+100		ns
			$\overline{SCK}$ output mode	200		ns
SI input hold time (against $\overline{SCK}\uparrow$)	t_{KSI}	SI0	$\overline{SCK}$ input mode	2tsys+100		ns
			$\overline{SCK}$ output mode	100		ns
$\overline{SCK}\downarrow\rightarrow$ SO delay time	t_{KSO}	SO0	$\overline{SCK}$ input mode		2tsys+250	ns
			$\overline{SCK}$ output mode		125	ns

Note 1) tsys indicates three values according to the contents of the clock control register (address; 00FE$_H$) upper 2 bits (CPU clock selection).
tsys [ns]=2000/fc (Upper 2 bits="00"), 4000/fc (Upper 2 bits="01"), 16000/fc (Upper 2 bits="11")

Note 2) $\overline{CS}$, $\overline{SCK}$, SI and SO means each pin of $\overline{CS}\rightarrow\overline{CS0}$, $\overline{SCK}\rightarrow$ SCK0, SI → SI0, and SO → SO0 respectively.

Note 3) The load of $\overline{SCK}$ output mode and SO output delay time is 50pF.

Fig. 4. Serial transfer timing (CH0)



Serial transfer (CH1) (SIO mode) (Ta=–10 to +75°C, V_{DD}=4.5 to 5.5V, Vss=0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{SCK1}$ cycle time	t_{KCY}	$\overline{SCK1}$	Input mode	2tsys+200		ns
			Output mode	16000/fc		ns
$\overline{SCK1}$ high and low level widths	t_{KH} t_{KL}	$\overline{SCK1}$	Input mode	tsys+100		ns
			Output mode	8000/fc–100		ns
SI1 input setup time (against $\overline{SCK1}$ ↑)	t_{SIK}	SI1	$\overline{SCK1}$ input mode	100		ns
			$\overline{SCK1}$ output mode	200		ns
SI1 input hold time (against $\overline{SCK1}$ ↑)	t_{KSI}	SI1	$\overline{SCK1}$ input mode	tsys+200		ns
			$\overline{SCK1}$ output mode	100		ns
SCK1 ↓ → SO1 delay time	t_{KSO}	SO1	$\overline{SCK1}$ input mode		tsys+200	ns
			$\overline{SCK1}$ output mode		100	ns

Note 1) tsys indicates three values according to the contents of the clock control register (address; 00FE$_H$) upper 2 bits (CPU clock selection).
tsys [ns]=2000/fc (Upper 2 bits="00"), 4000/fc (Upper 2 bits="01"), 16000/fc (Upper 2 bits="11")

Note 2) The load of $\overline{SCK1}$ output mode and SO1 output delay time is 50pF+1TTL.

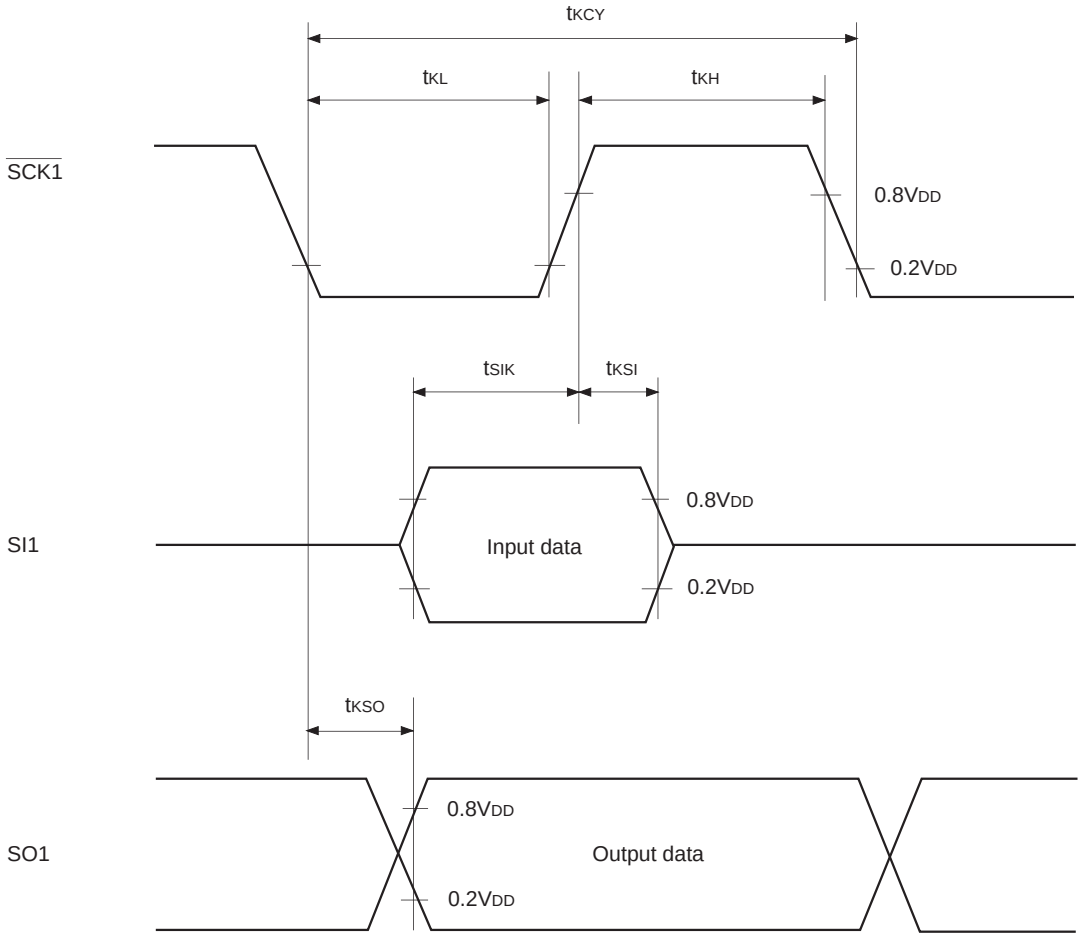
Serial transfer (CH1) (SIO mode) (Ta=–10 to +75°C, V_{DD}=3.0 to 3.6V, Vss=0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{SCK1}$ cycle time	t_{KCY}	$\overline{SCK1}$	Input mode	2tsys+200		ns
			Output mode	16000/fc		ns
$\overline{SCK1}$ high and low level widths	t_{KH} t_{KL}	$\overline{SCK1}$	Input mode	tsys+100		ns
			Output mode	8000/fc–150		ns
SI1 input setup time (against $\overline{SCK1}$ ↑)	t_{SIK}	SI1	$\overline{SCK1}$ input mode	100		ns
			$\overline{SCK1}$ output mode	200		ns
SI1 input hold time (against $\overline{SCK1}$ ↑)	t_{KSI}	SI1	$\overline{SCK1}$ input mode	tsys+200		ns
			$\overline{SCK1}$ output mode	100		ns
SCK1 ↓ → SO1 delay time	t_{KSO}	SO1	$\overline{SCK1}$ input mode		tsys+250	ns
			$\overline{SCK1}$ output mode		125	ns

Note 1) tsys indicates three values according to the contents of the clock control register (address; 00FE$_H$) upper 2 bits (CPU clock selection).
tsys [ns]=2000/fc (Upper 2 bits="00"), 4000/fc (Upper 2 bits="01"), 16000/fc (Upper 2 bits="11")

Note 2) The load of $\overline{SCK1}$ output mode and SO1 output delay time is 50pF.

Fig. 5. Serial transfer CH1 timing (SIO mode)



Serial transfer (CH1) (Special mode) (Ta=–10 to +75°C, V_{DD}=4.5 to 5.5V, Vss=0V)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
SO1 cycle time	t_{LCY}	SO1 SI1	Note 1)		104		µs
SI1 data setup time	t_{LSU}	SI1		2			µs
SI1 data hold time	t_{LHD}	SI1		2			µs

Note 1) t_{LCY} specifies only serial mode register (CH1) (SIOM1: Address 01FA$_H$) lower 2 bits (SO1 clock selection) has been set at 104µs.

Note 2) The load of SO1 pin is 50pF+1TTL.

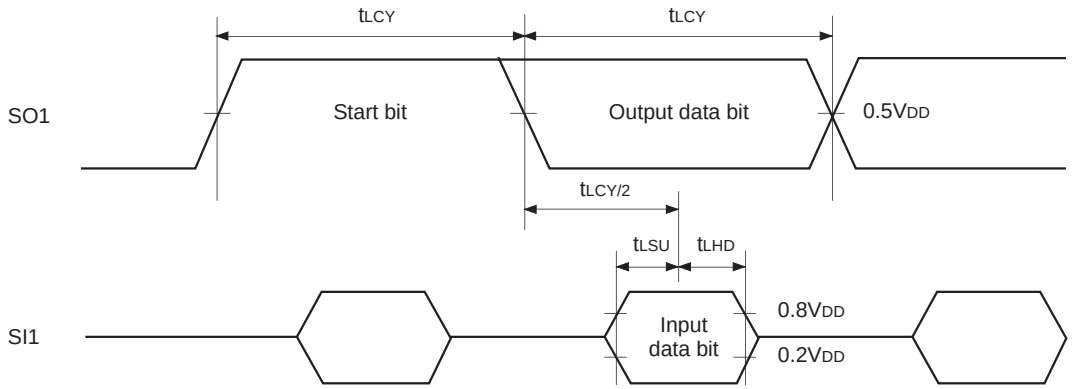
Serial transfer (CH1) (Special mode) (Ta=–10 to +75°C, V_{DD}=3.0 to 3.6V, Vss=0V)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
SO1 cycle time	t_{LCY}	SO1 SI1	Note 1)		104		µs
SI1 data setup time	t_{LSU}	SI1		2			µs
SI1 data hold time	t_{LHD}	SI1		2			µs

Note 1) t_{LCY} specifies only serial mode register (CH1) (SIOM1: Address 01FA$_H$) lower 2 bits (SO1 clock selection) has been set at 104µs.

Note 2) The load of SO1 pin is 50pF.

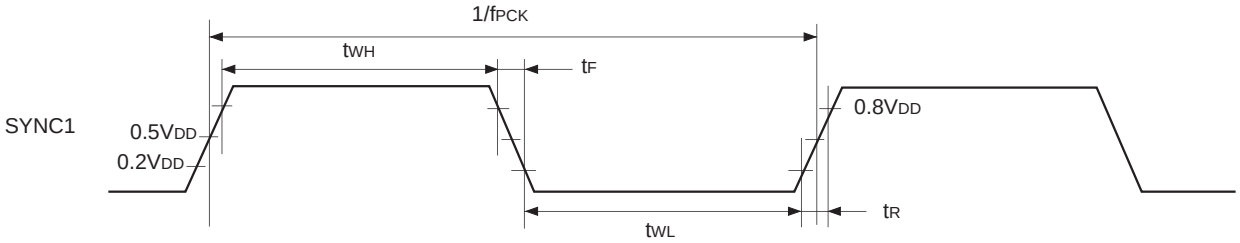
Fig. 6. Serial transfer CH1 timing (Special mode)



(3) General purpose prescaler (Ta=–10 to +75°C, V_{DD}=4.5 to 5.5V, Vss=0V)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
External clock input frequency	f_{PCK}	SYNC1				12	MHz
External clock input pulse width	t_{WH}, t_{WL}	SYNC1		33			ns
External clock input rise and fall times	t_R, t_F	SYNC1				200	ns

Fig. 7. General purpose prescaler timing



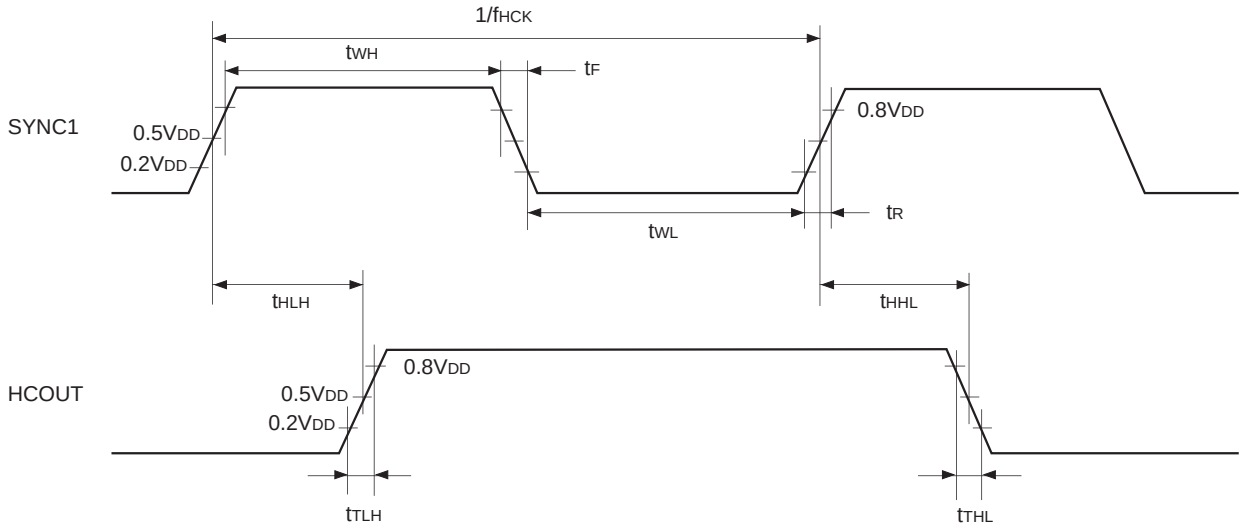
(4) HSYNC counter (Ta=–10 to +75°C, V_{DD}=3.0 to 5.5V, Vss=0V)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
External clock input frequency	f_{HCK}	SYNC1				12	MHz
External clock input pulse width	t_{WH}, t_{WL}	SYNC1		33			ns
External clock input rise and fall times	t_R, t_F	SYNC1				200	ns
HCOUT output delay time (against SYNC1 ↑)	t_{HLH}, t_{HHL}	HCOUT	External clock input SYNC1 t_R=t_F=6ns		tsys+130	tsys+220	ns
HCOUT output rise and fall times	t_{TLH}	HCOUT	External clock input SYNC1 t_R=t_F=6ns		24	50	ns
	t_{THL}				12	25	ns

Note1) tsys indicates three values according to the contents of the clock control register (address; 00FE$_H$) upper 2 bits (CPU clock selection).
tsys [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11").

Note2) The load of HCOUT pin is 50pF.

Fig. 8. HSYNC counter timing



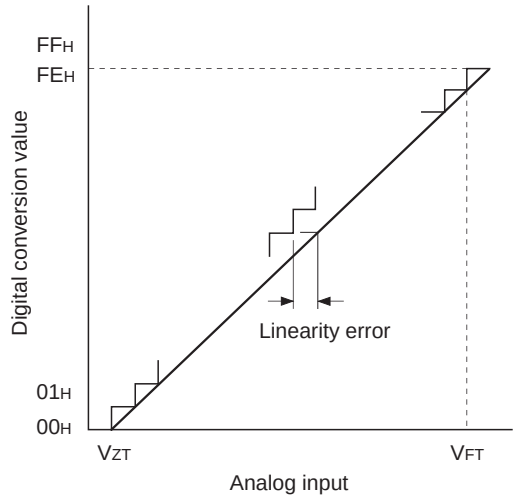
(5) A/D converter characteristics (Ta=–10 to +75°C, V_{DD}=AV_{DD}=4.5 to 5.5V, AV_{REF}=4.0 to AV_{DD}, V_{SS}=AV_{SS}=0V)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			Ta=25°C V_{DD}=AV_{DD}=AV_{REF}=5.0V V_{SS}=AV_{SS}=0V			±1	LSB
Absolute error						±2	LSB
Conversion time	t_{CONV}			160/f_{ADC}*			µs
Sampling time	t_{SAMP}			12/f_{ADC}*			µs
Reference input voltage	V_{REF}	AV_{REF}	V_{DD}=AV_{DD}=4.5 to 5.5V	AV_{DD}–0.5		AV_{DD}	V
Analog input voltage	V_{IAN}	AN0 to AN11		0			V
AV_{REF} current	I_{REF}	AV_{REF}	Operating mode		0.6	1.0	mA
	I_{REFS}		SLEEP mode STOP mode 32kHz operating mode			10	µA

(Ta=–10 to +75°C, V_{DD}=AV_{DD}=3.0 to 3.6V, AV_{REF}=2.7 to AV_{DD}, V_{SS}=AV_{SS}=0V)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			Ta=25°C V_{DD}=AV_{DD}=AV_{REF}=5.0V V_{SS}=AV_{SS}=0V			±1	LSB
Absolute error						±2	LSB
Conversion time	t_{CONV}			160/f_{ADC}*			µs
Sampling time	t_{SAMP}			12/f_{ADC}*			µs
Reference input voltage	V_{REF}	AV_{REF}	V_{DD}=AV_{DD}=3.0 to 3.6V	AV_{DD}–0.3		AV_{DD}	V
Analog input voltage	V_{IAN}	AN0 to AN11		0			V
AV_{REF} current	I_{REF}	AV_{REF}	Operating mode		0.4	0.7	mA
	I_{REFS}		SLEEP mode STOP mode 32kHz operating mode			10	µA

Fig. 9. Definitions of A/D converter terms



* The value of f_{ADC} is as follows by selecting ADC operation clock (MSC: Address 01FFH bit 0).
When PS2 is selected, f_{ADC}=fc/2
When PS1 is selected, f_{ADC}=fc

(6) Interruption, reset input (Ta=–10 to +75°C, V_{DD}=3.0 to 5.5V, Vss=0V)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
External interruption high and low level widths	t_{IH} t_{IL}	$\overline{INT0}$ $\overline{INT1}$ $\overline{INT2}$ $\overline{NMI}$ PJ0 to PJ7		1		µs
Reset input low level width	t_{RSL}	$\overline{RST}$		32/fc		µs

Fig. 10. Interruption input timing

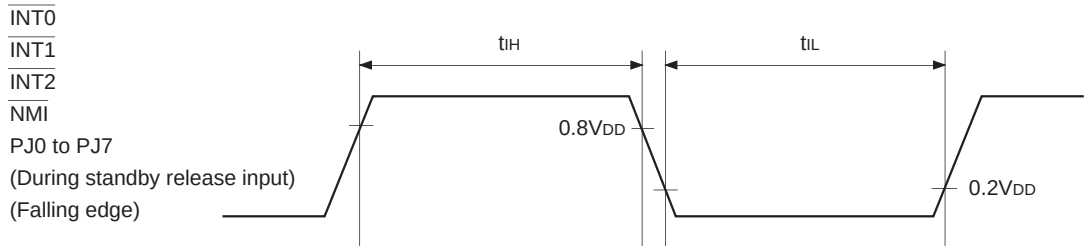
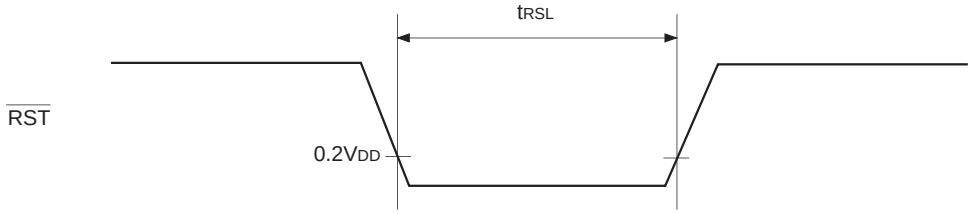


Fig. 11. Reset input timing

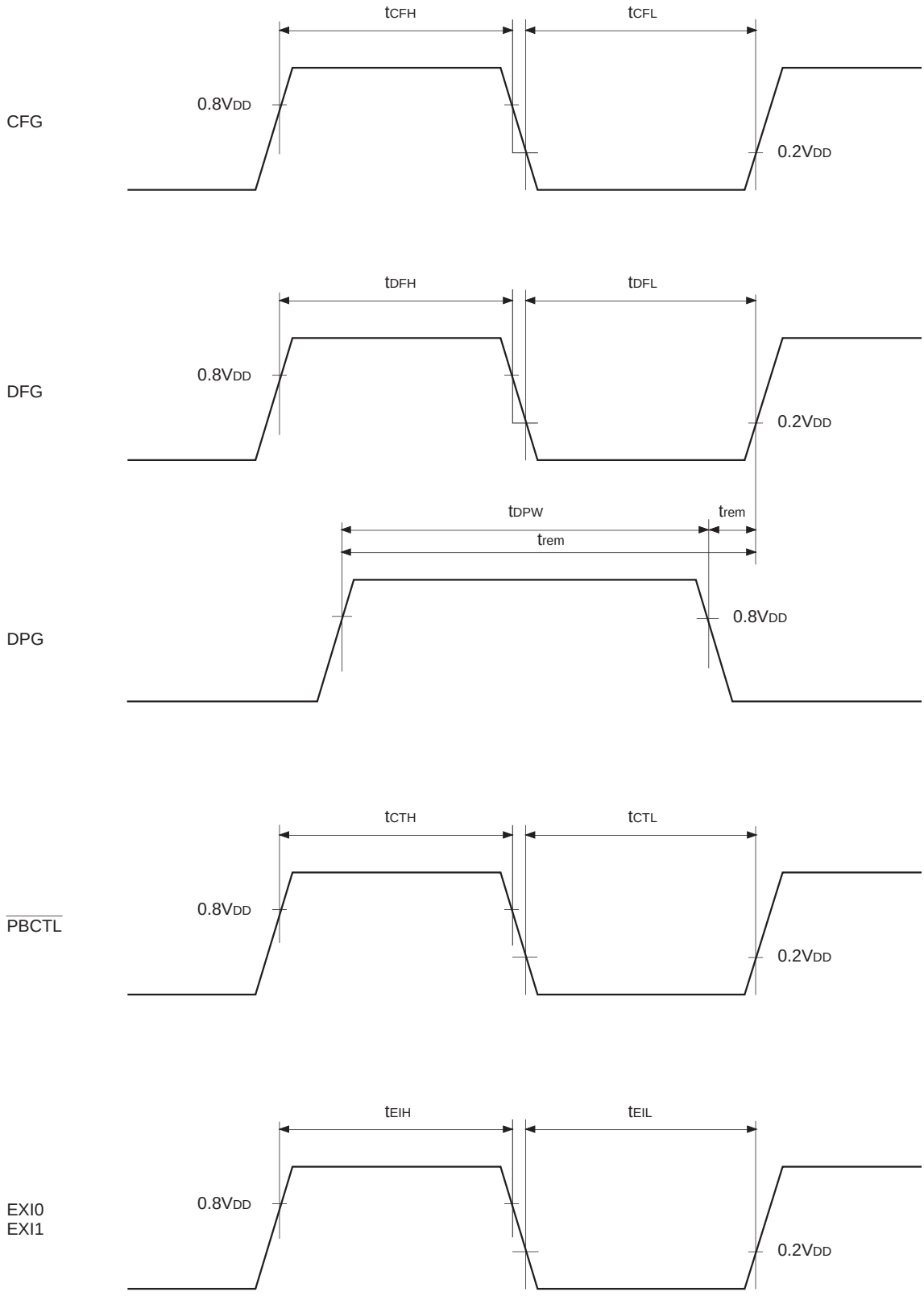


(7) Others (Ta=–10 to +75°C, V_{DD}=3.0 to 5.5V, Vss=0V)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
CFG input high and low level widths	t_{CFH} t_{CFL}	CFG		t_{FRC} x 24+200		ns
DFG input high and low level widths	t_{DFH} t_{DFL}	DFG		t_{FRC} x 16+200		ns
DPG minimum pulse width	t_{DPW}	DPG		t_{FRC} x 8+200		ns
DPG minimum removal time	t_{rem}	DPG		t_{FRC} x 16+200		ns
$\overline{PBCTL}$ input high and low level widths	t_{CTH} t_{CTL}	$\overline{PBCTL}$	tsys=2000/fc	t_{FRC} x 8+200+tsys		ns
EXI input high and low level widths	t_{EIH} t_{EIL}	EXI0 EXI1	tsys=2000/fc	t_{FRC} x 8+200+tsys		ns

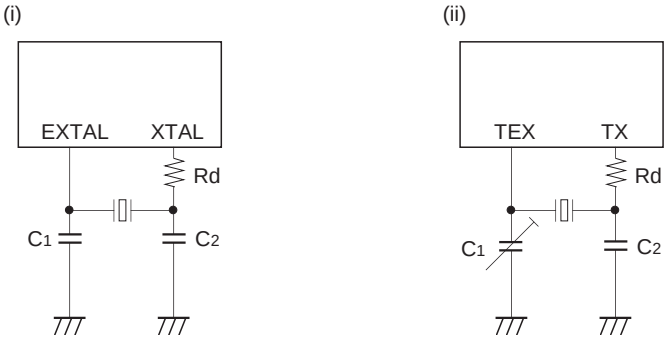
Note) tsys indicates three values according to the contents of the clock control register (address; 00FE$_H$) upper 2 bits (CPU clock selection).
tsys [ns]=2000/fc (Upper 2 bits="00"), 4000/fc (Upper 2 bits="01"), 16000/fc (Upper 2 bits="11")
t_{FRC}=1000/fc [ns]

Fig. 12. Other timings



Supplement

Fig. 13. Recommended oscillation circuit



Manufacturer	Model	fc (MHz)	C_1 (pF)	C_2 (pF)	Rd (Ω)	Circuit example
RIVER ELETEC CO., LTD.	HC-49/U03	8.00	10	10	0	(i)
		10.00	5	5		
		12.00				
		16.00				
KINSEKI LTD.	HC-49/U (-S)	8.00	16 (12)	16 (12)	0	(i)
		10.00	16 (12)	16 (12)		
		12.00	12	12		
		16.00	12	12	0	
	P3	32.768kHz	30	18	470k	(ii)

Selection Guide

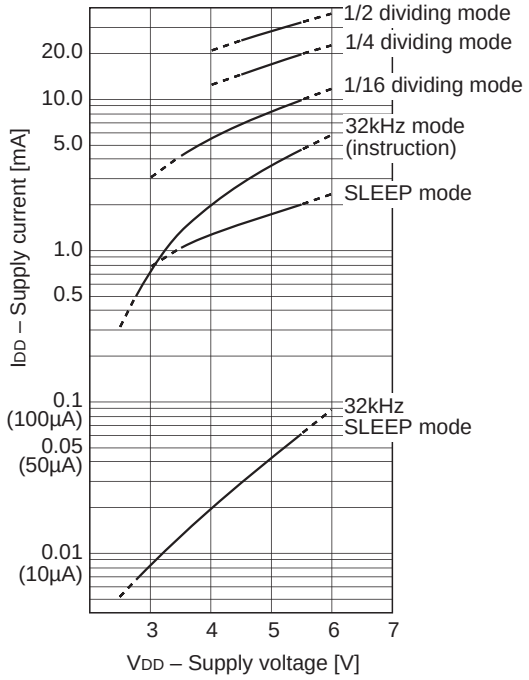
Option item	Mask product	CXP873P60Q-1 -□□□	CXP873P60R-1 -□□□	CXP873P60Q-2 -□□□	CXP873P60R-2 -□□□
Package	100-pin plastic QFP/LQFP	100-pin plastic QFP	100-pin plastic LQFP	100-pin plastic QFP	100-pin plastic LQFP
ROM capacitance	52K byte /60K byte	PROM 60K byte	PROM 60K byte	PROM 60K byte	PROM 60K byte
Reset pin pull-up resistor	Existent /Non-Existent	Existent	Existent	Existent	Existent
Input circuit format*	CMOS schmitt /TTL schmitt	TTL schmitt	TTL schmitt	CMOS schmitt	CMOS schmitt

* Pins PG4/SYNC0, PG5/SYNC1 only.

Characteristics Curve

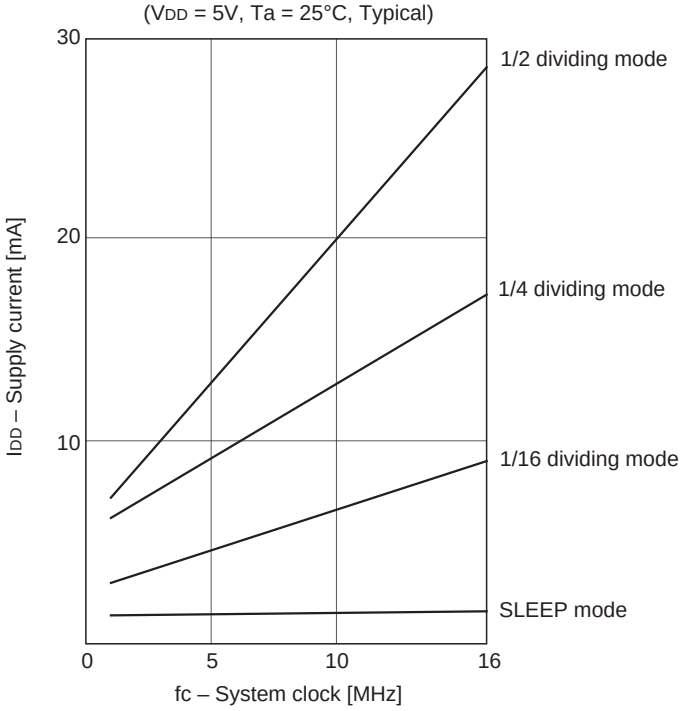
IDD vs. VDD

(fc = 16MHz, Ta = 25°C, Typical)



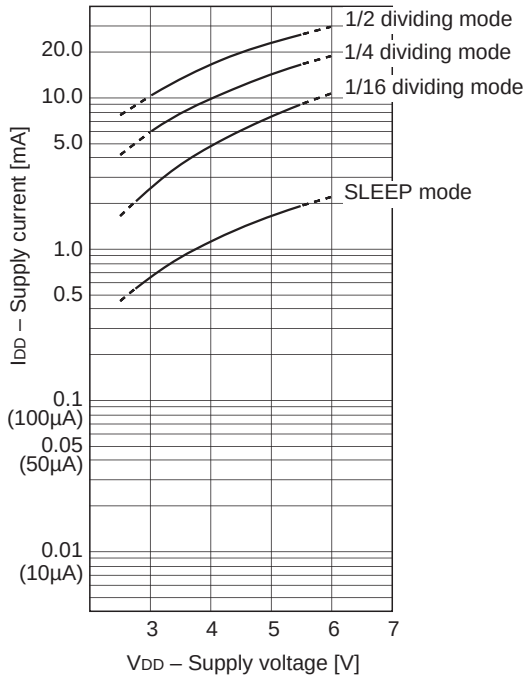
IDD vs. fc

(VDD = 5V, Ta = 25°C, Typical)



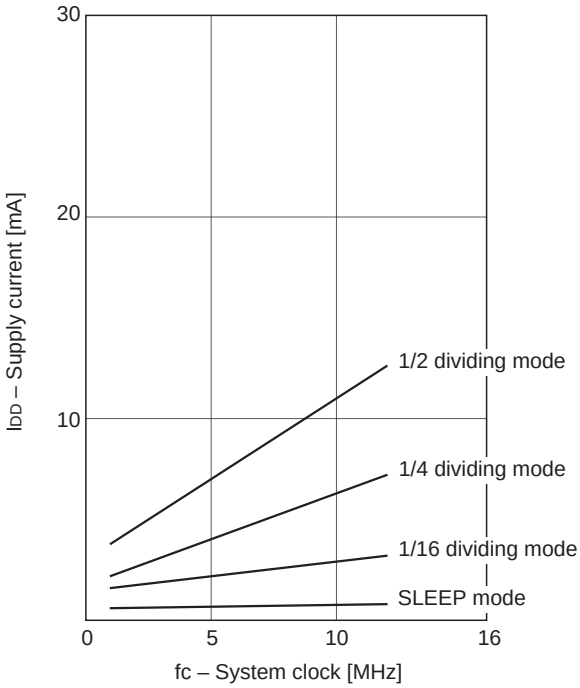
IDD vs. VDD

(fc = 12MHz, Ta = 25°C, Typical)



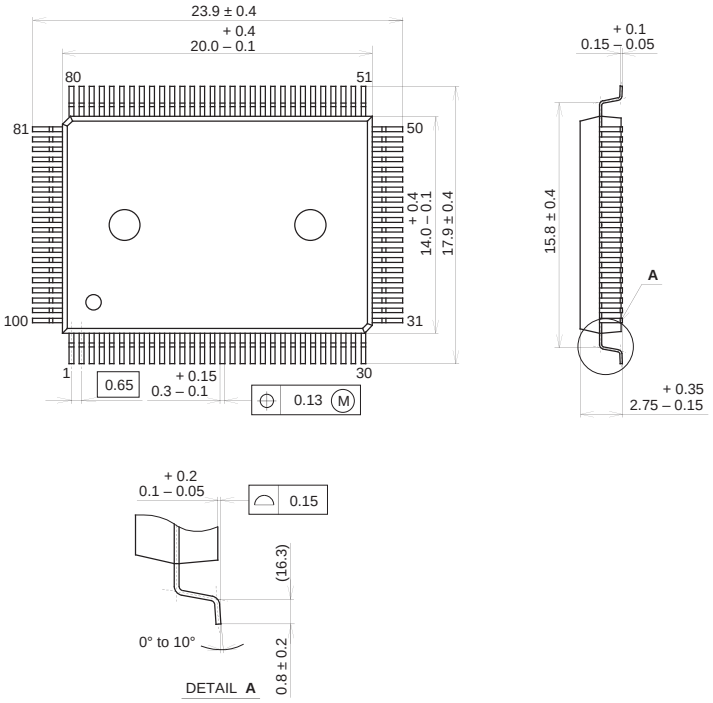
IDD vs. fc

(VDD = 3.3V, Ta = 25°C, Typical)



Package Outline Unit: mm

100PIN QFP (PLASTIC)

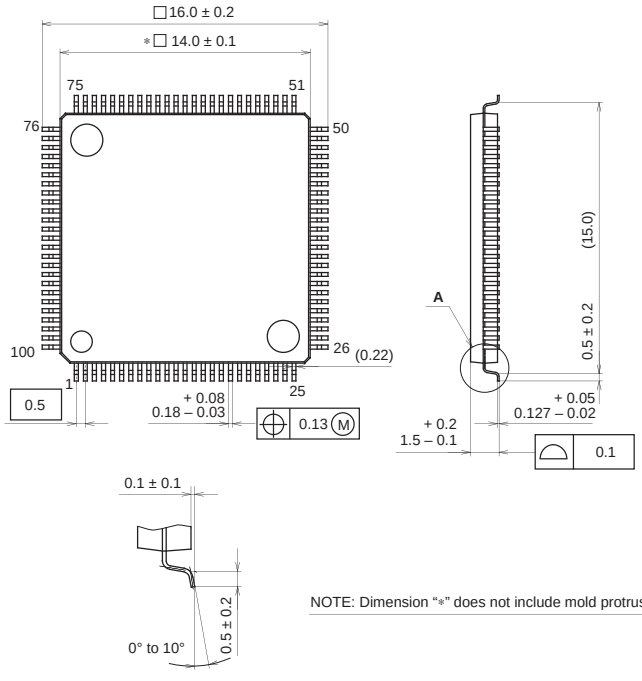


SONY CODE	QFP-100P-L01
EIAJ CODE	QFP100-P-1420
JEDEC CODE	———

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.7g

100PIN LQFP (PLASTIC)



NOTE: Dimension "*" does not include mold protrusion.

SONY CODE	LQFP-100P-L01
EIAJ CODE	LQFP100-P-1414
JEDEC CODE	———

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	0.8g