CY14V116F7
CY14V116G7

16-Mbit nvSRAM with Asynchronous NAND Interface

Features

- 16-Mbit nonvolatile static random access memory (nvSRAM)
  - Performance up to 33 MT/s per I/O
  - Maximum data throughput using ×16 bus – 528 Mbps
  - Industry-standard asynchronous NAND Flash interface with reduced instruction set
  - Shared address, data, and command bus
    - Address and command bus is 8 bits
    - Command is sent in one or two command cycles
    - Address is sent in five address cycles
    - Data bus width is ×8 or ×16 bits
- Modes of operation:
  - Asynchronous NAND Interface I/O with 30-ns access time
  - Status Register with a software method for detecting the following:
    - Nonvolatile STORE completion
    - Pass/Fail condition of previous command
    - Write protect status
- Hands-off automatic STORE on power-down with only a small capacitor
- STORE to QuantumTrap nonvolatile elements is initiated by a software command, a dedicated hardware pin, or AutoStore on power-down
- RECALL to SRAM initiated by software or power-up
- High reliability
  - Infinite read, write, and RECALL cycles
  - 1 million STORE cycles to QuantumTrap
- Data retention: 20 years at 85 °C
- Operating voltage
  - Core V_{CC} = 2.7 V to 3.6 V; I/O V_{CCQ} = 1.70 V to 1.95 V
- 165-ball fine-pitch ball grid array (FBGA) package
- Industrial temperature: –40 °C to +85 °C
- Restriction of hazardous substances (RoHS) compliant

Overview

Cypress nvSRAM combines high-performance SRAM cells with nonvolatile elements in a monolithic integrated circuit. The embedded nonvolatile elements incorporate the Silicon-Oxide-Nitride-Oxide-Silicon (SONOS) technology, producing the world's most reliable nonvolatile memory. The SRAM can be read and written an infinite number of times. The nonvolatile data resides in the nonvolatile elements and does not change when data is written to the SRAM.

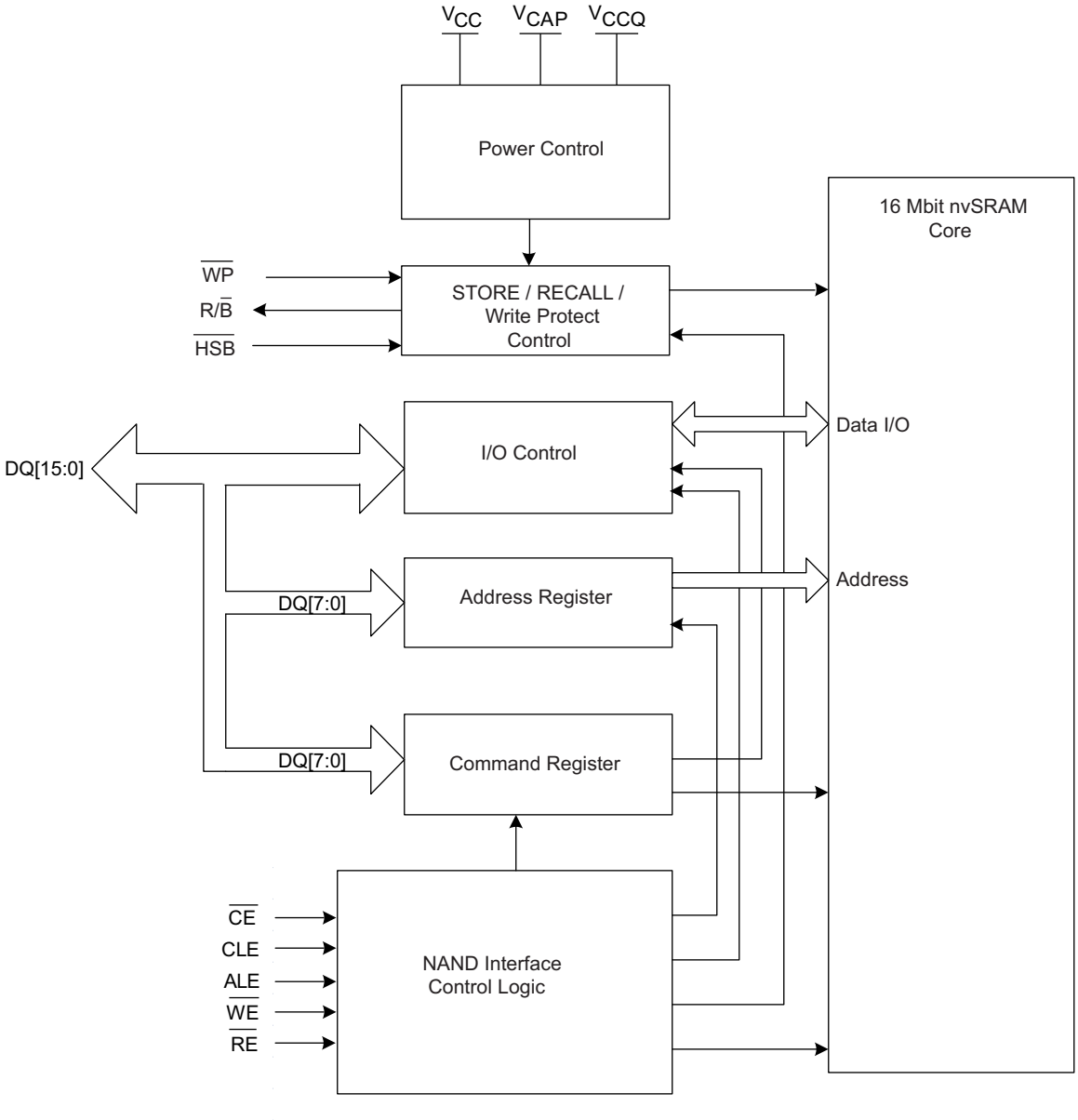
The CY14V116F7/CY14V116G7 nvSRAM provides access through a standard asynchronous NAND interface and supports the ×8 and ×16 interface options. In the case of ×16 interface, data bytes are transmitted over the DQ[15:0] lines and has double the throughput compared to the DQ[7:0] bus. The CY14V116F7/ CY14V116G7 uses a highly multiplexed DQ bus to transfer data, addresses, and instructions. All addresses and commands are always transmitted over the data bus DQ[7:0]. Therefore, in the case of the ×16 bus interface, the upper eight data bits DQ[15:8] become don't care bits during the address and command cycles. The CY14V116F7/CY14V116G7 uses five control pins (CLE, ALE, $\overline{CE}$, $\overline{RE}$, and $\overline{WE}$) to transfer command, address, and data during read and write operations. Additional I/O pins, such as write protect ($\overline{WP}$), ready/busy (R/$\overline{B}$), and $\overline{HSB}$ STORE, are used to support features in the device.

The asynchronous NAND interface nvSRAM is aligned to a majority of the ONFI 1.0 specifications and supports data access speed up to 33 MHz.

For a complete list of related documentation, click here.

Block Diagram

Single-Channel Architecture



Contents

Pin Configurations

Figure 1. Single-Channel (×8) Pin Diagram: 165-ball FBGA

	1	2	3	4	5	6	7	8	9	10	11
A	R	R	R	NC	NC	NC	NC	NC	R	R	R
B	R	R	R	NC	NC	NC	NC	NC	R	R	R
C	R	V_{CCQ}	V_{CCQ}	NC	V_{SS}	NC	V_{CC}	NC	V_{CCQ}	V_{CCQ}	R
D	R	V_{SS}	NC	V_{SS}	NC	NC	NC	V_{SS}	NC	V_{SS}	R
E	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
F	NC	V_{SS}	V_{CCQ}	NC	NC	NC	NC	NC	V_{CCQ}	V_{SS}	NC
G	NC	NC	NC	NC	R	NC	NC	NC	NC	$\overline{HSB}$	NC
H	NC	V_{SS}	V_{CC}	R/$\overline{B}$	NC	NC	NC	NC	V_{CC}	V_{SS}	NC
J	NC	V_{CAP}	NC	$\overline{CE}$	NC	NC	NC	$\overline{WP}$	R	NC	NC
K	NC	V_{SS}	V_{CCQ}	NC	NC	NC	CLE	ALE	V_{CCQ}	V_{SS}	NC
L	NC	DQ7	DQ6	NC	$\overline{WE}$	NC	NC	NC	DQ1	DQ0	NC
M	R	V_{SS}	DQ5	V_{SS}	$\overline{RE}$	NC	NC	V_{SS}	DQ2	V_{SS}	R
N	R	V_{CCQ}	V_{CCQ}	DQ4	V_{CC}	NC	V_{SS}	DQ3	V_{CCQ}	V_{CCQ}	R
P	R	R	R	NC	NC	NC	NC	NC	R	R	R
R	R	R	R	NC	NC	NC	NC	NC	R	R	R

Figure 2. Single-Channel (×16) Pin Diagram: 165-ball FBGA

	1	2	3	4	5	6	7	8	9	10	11
A	R	R	R	NC	NC	NC	NC	NC	R	R	R
B	R	R	R	NC	NC	NC	NC	NC	R	R	R
C	R	V_{CCQ}	V_{CCQ}	DQ11	V_{SS}	NC	V_{CC}	DQ12	V_{CCQ}	V_{CCQ}	R
D	R	V_{SS}	DQ10	V_{SS}	NC	NC	NC	V_{SS}	DQ13	V_{SS}	R
E	NC	DQ8	DQ9	NC	NC	NC	NC	NC	DQ14	DQ15	NC
F	NC	V_{SS}	V_{CCQ}	NC	NC	NC	NC	NC	V_{CCQ}	V_{SS}	NC
G	NC	NC	NC	NC	R	NC	NC	NC	NC	$\overline{HSB}$	NC
H	NC	V_{SS}	V_{CC}	R/$\overline{B}$	NC	NC	NC	NC	V_{CC}	V_{SS}	NC
J	NC	V_{CAP}	NC	$\overline{CE}$	NC	NC	NC	$\overline{WP}$	R	NC	NC
K	NC	V_{SS}	V_{CCQ}	NC	NC	NC	CLE	ALE	V_{CCQ}	V_{SS}	NC
L	NC	DQ7	DQ6	NC	$\overline{WE}$	NC	NC	NC	DQ1	DQ0	NC
M	R	V_{SS}	DQ5	V_{SS}	$\overline{RE}$	NC	NC	V_{SS}	DQ2	V_{SS}	R
N	R	V_{CCQ}	V_{CCQ}	DQ4	V_{CC}	NC	V_{SS}	DQ3	V_{CCQ}	V_{CCQ}	R
P	R	R	R	NC	NC	NC	NC	NC	R	R	R
R	R	R	R	NC	NC	NC	NC	NC	R	R	R

Pin Definitions

Pin Name	I/O Type	Description
R/$\overline{B}$	Output	**Ready/Busy.** The ready/busy signal indicates the device status. When it is pulled LOW, the signal indicates that nvSRAM is busy doing either a STORE or a power-up RECALL or a Software RECALL/Software STORE/AutoStore Disable/AutoStore Enable operation. This signal is an open drain output and requires an external pull-up resistor.
$\overline{RE}$	Input	**Read Enable.** The read enable signal enables the data output during read operation.
$\overline{CE}$	Input	**Chip Enable.** The chip enable signal selects the device when pulled LOW. When chip enable is HIGH and the device is not busy doing a STORE operation, the device goes into a low-power standby state.
CLE	Input	**Command Latch Enable.** The command latch enable signal is used to latch the command byte. This is one of the signals used by the host to indicate the type of bus cycle (command, address, and data).
ALE	Input	**Address Latch Enable.** The address latch enable signal is used to latch the address byte. This is one of the signals used by the host to indicate the type of bus cycle (command, address, and data).
$\overline{WE}$	Input	**Write Enable.** The write enable signal controls the latching of the input data on every rising edge.
$\overline{WP}$	Input	**Write Protect.** The $\overline{WP}$ disables the SRAM write operation in nvSRAM if pulled LOW.
DQ[7:0][1]	Input/Output	**I/O Port, 8 bits for the ×8 configuration.** The I/O port is an 8-bit wide bidirectional port for transferring address, command, and data to and from the device.
DQ[15:0][1]	Input/Output	**I/O Port, 16 bits for the ×16 configuration.** The I/O port is a 16-bit wide bidirectional bus to transfer data words to and from the device during write and read operations. Address and commands are always transmitted over the lower 8 bits DQ[7:0].
$\overline{HSB}$	Input	**Hardware STORE.** When pulled LOW external to the chip, it will initiate a nonvolatile STORE operation.
V_{CAP}	Power supply	**AutoStore capacitor:** Supplies power to the nvSRAM during power loss to store data from SRAM to nonvolatile elements.
V_{CC}	Power supply	**Power.** Power supply inputs to the core of the device.
V_{CCQ}	Power supply	**I/O Power.** Power supply inputs for the inputs and outputs of the device.
V_{SS}	Power supply	**Ground for the device**. Must be connected to ground of the system.
R	R	**Reserved.** These pins are reserved, should be left unconnected by the host.
NC	NC	**No Connect**. Die pads are not connected to the package pin.

Discovery and Initialization

When the power-up cycle starts and V_{CC} crosses the V_{SWITCH} threshold, the device initializes an internal Power-up RECALL operation and pulls the R/$\overline{B}$ pin LOW for t_{RECALL} duration. When the power-up cycle is completed, the device releases the R/$\overline{B}$ pin, which is then pulled HIGH by an external pull-up resistor connected to it. The R/$\overline{B}$ HIGH indicates the device's ready status and allows the host controller to communicate with the device by executing opcodes. All supported opcodes are described in Table 3 on page 9.

nvSRAM Bus Operations

The nvSRAM device I/Os are multiplexed. Data I/O, addresses, and commands all share the same I/O pins. DQ[15:8] are used only for data in the ×16 configuration. Addresses and commands are always transmitted through DQ[7:0] and data through DQ[15:0] in the ×16 configuration.

The command sequence normally consists of a Command Latch cycle, Address Input cycles, and one or more Data cycles, either Read or Write.

Control Signals

The nvSRAM control signals, such as $\overline{CE}$, $\overline{WE}$, $\overline{RE}$, CLE, ALE, and $\overline{WP}$, control the nvSRAM device read and write operations. The $\overline{CE}$ is used to enable the device when pulled LOW and the device is not in the busy state. When the nvSRAM is selected, it accepts command, address, and data bytes. The nvSRAM will enter the standby mode if $\overline{CE}$ goes HIGH while data is being transferred and the device is not busy.

A HIGH CLE signal, along with $\overline{CE}$ and $\overline{WE}$ LOW, indicates a command input cycle. Similarly, a HIGH ALE signal, along with $\overline{CE}$ and $\overline{WE}$ LOW, indicates an Address Input cycle.

Note
1. Data DQ[7:0] for the ×8 configuration and data DQ[15:0] for the ×16 configuration.

nvSRAM Bus Modes

Depending upon the input control signals status, the nvSRAM takes any of the following bus states as defined in Table 1.

Table 1. Asynchronous NAND Interface Bus Modes

$\overline{CE}$	ALE	CLE	$\overline{WE}$	$\overline{RE}$	$\overline{WP}$	Bus State
1	X	X	X	X	X	Standby
0	0	0	1	1	X	Bus Idle
0	0	1	0	1	X	Command cycle
0	1	0	0	1	X	Address cycle
0	0	0	0	1	H	Write Cycle
0	0	0	1	0	X	Read Cycle
0	1	1	X	X	X	Undefined
0	0	0	0	1	L	Write protect to SRAM

Note Signal with state 'X' can be either $\geq V_{IH}$ or $\leq V_{IL}$.

nvSRAM Enable/Standby

A chip enable ($\overline{CE}$) signal is used to enable or disable the device. When $\overline{CE}$ is driven LOW, all nvSRAM input signals are enabled. With $\overline{CE}$ LOW, the nvSRAM can accept commands, addresses, and data on its DQ lines. The nvSRAM is disabled when $\overline{CE}$ is driven HIGH, even when the device is busy. The nvSRAM enters the low-power standby mode when the device status is ready and R/$\overline{B}$ is pulled HIGH by the external pull-up resistor. When $\overline{CE}$ is disabled, all nvSRAM I/Os are disabled except $\overline{WP}$, R/$\overline{B}$, and $\overline{HSB}$.

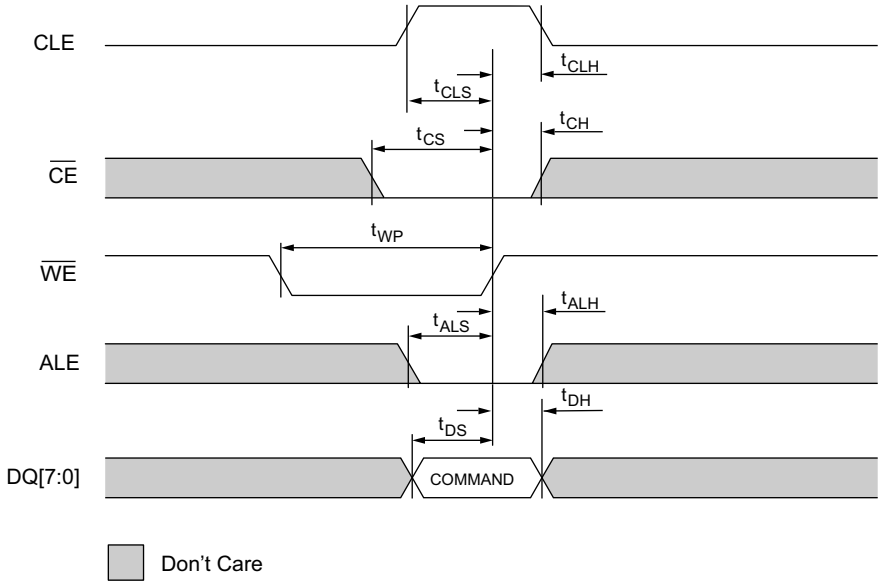
nvSRAM Bus Idle

The nvSRAM goes to the bus idle state when $\overline{CE}$, ALE, CLE are LOW, and $\overline{WE}$, $\overline{RE}$ are HIGH. During bus idle, all the input signals are enabled but the commands, addresses, and data are not latched in the device and there is also no data output from the device.

nvSRAM Commands

A command is written from DQ[7:0] to the command register on the rising edge of $\overline{WE}$ when $\overline{CE}$ is LOW, ALE is LOW, CLE is HIGH, and $\overline{RE}$ is HIGH. All commands except the status register read (70h) and reset (FFh) are ignored when the nvSRAM is busy (RDY bit is set to '0' in the status register).

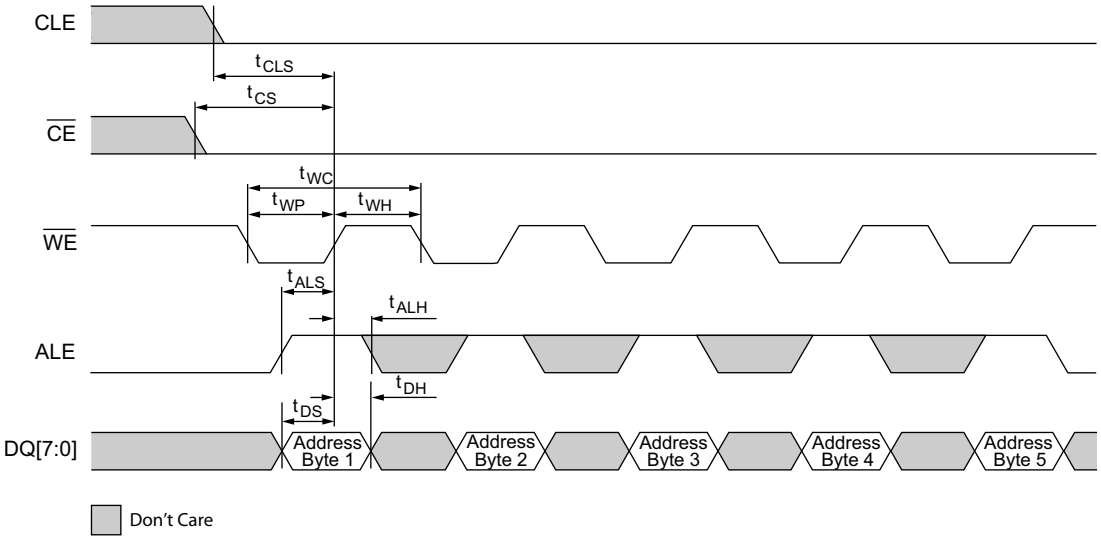
Figure 3. Command Latch Cycle



nvSRAM Address Input

During the nvSRAM address cycle, the host transmits the five consecutive address bytes through DQ[7:0] to the address register on every rising edge of $\overline{WE}$ toggle when $\overline{CE}$ is LOW, ALE is HIGH, CLE is LOW, and $\overline{RE}$ is HIGH. In five-byte addressing, the least significant address byte is sent in the first address cycle and the most significant address byte is sent in the fifth address cycle. nvSRAM requires only the first three address bytes to address its entire 16-Mbit memory. Therefore, the two extra address bytes in the five-byte address are don't care bytes. All unused address bits, including the don't care bits, should be set to '0' by the host controller. The address cycle is ignored by the nvSRAM during the busy (RDY bit is set to '0' in the status register) period. Refer to Table 2 on page 9 for nvSRAM addressing.

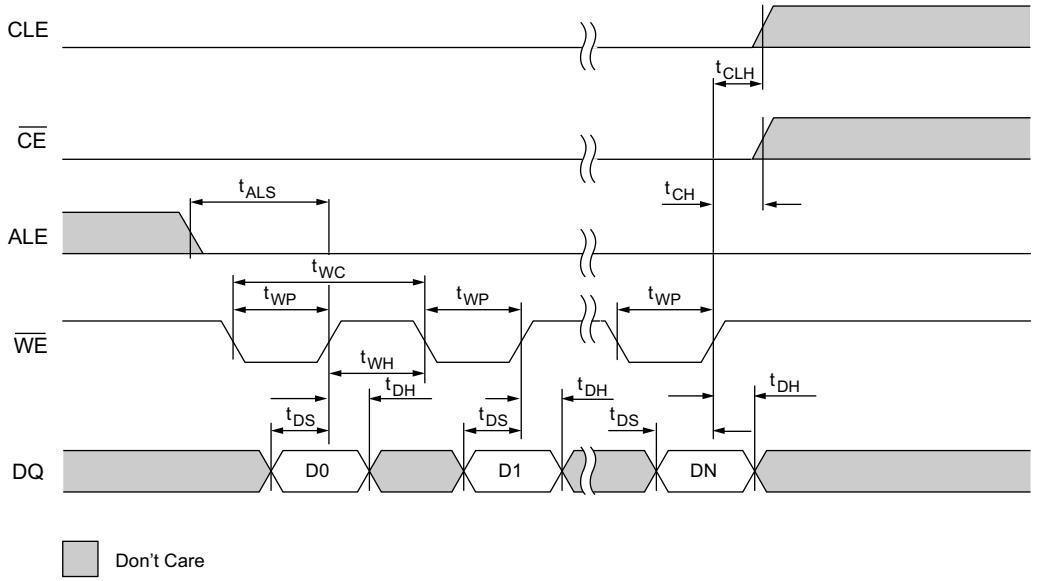
Figure 4. Address Latch Cycle



nvSRAM Data Input

Data is written from DQ (DQ[7:0] or DQ[15:0]) to the data register of the nvSRAM on the rising edge of $\overline{WE}$ when $\overline{CE}$ is LOW, ALE is LOW, CLE is LOW, and $\overline{RE}$ is HIGH. Data inputs are ignored by the nvSRAM during device busy (RDY bit is set to '0' in the status register) state.

Figure 5. Data Input Cycle



nvSRAM Data Output

Data is sent out (during read) on the DQ bus (DQ[7:0] or DQ[15:0]) by the nvSRAM if it is in the ready status. Data is output from the data register on every falling edge of $\overline{RE}$ when $\overline{CE}$ is LOW, ALE is LOW, CLE is LOW, and $\overline{WE}$ is HIGH. nvSRAM ignores the read request if it is busy (RDY bit is set to '0' in the status register) during a STORE cycle.

Figure 6. Data Output Cycles

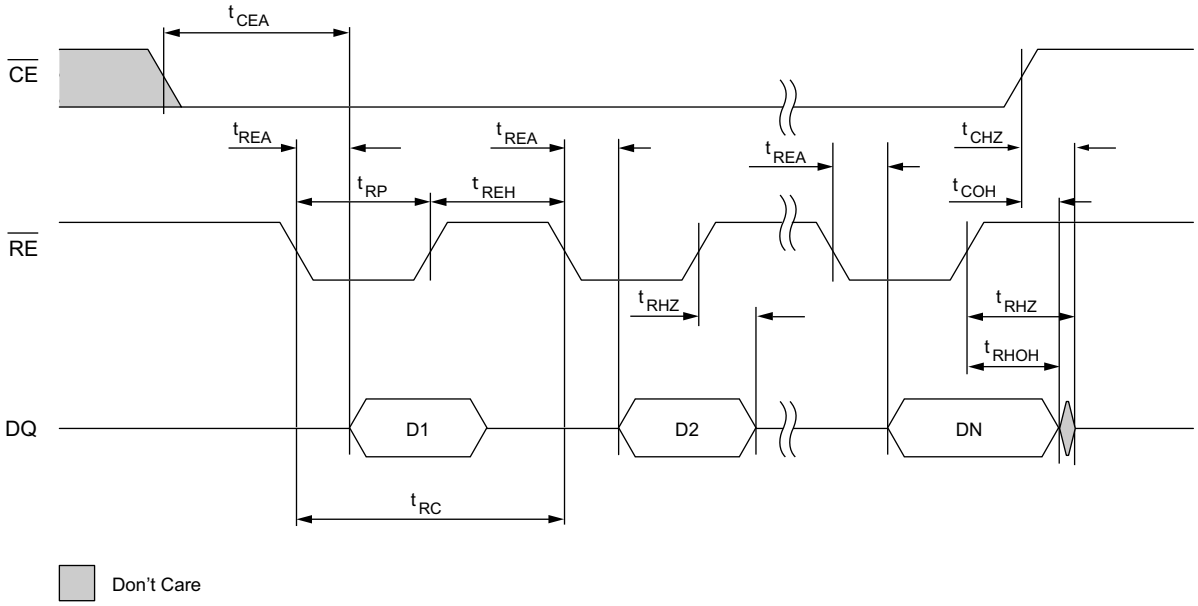


Table 2. nvSRAM Addressing

Address Cycle	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
First	A7	A6	A5	A4	A3	A2	A1	A0
Second	A15	A14	A13	A12	A11	A10	A9	A8
Third	Don't care[3]			A20/LOW [2]	A19	A18	A17	A16
Fourth	Don't care[3]							
Fifth	Don't care[3]							

Command Definition

The nvSRAM has address, command, and data multiplexed on its I/Os. All commands and addresses are written through the DQ bus DQ[7:0] by toggling $\overline{WE}$ to LOW while $\overline{CE}$ and CLE are LOW and ALE is HIGH for the address cycle and $\overline{CE}$ and ALE are LOW and CLE is HIGH for the command cycle. The status of all the input pins are latched on the rising edge of $\overline{WE}$ after which the device determines whether the bus cycle is a command cycle, address cycle, data input cycle, or data output cycle. All the asynchronous NAND interface nvSRAM commands are listed in Table 3.

Table 3. nvSRAM Commands Table

nvSRAM Function	First Cycle	Second Cycle	Description
Read ID	90h		Identifies that the target supports the ONFI specification. If the target supports the ONFI specification, then the ONFI signature is returned.
Read Parameter Page	ECh		The read parameter page function retrieves the data structure that describes the target's organization, features, timings and other behavioral parameters.
Read Status	70h		Retrieves a status value for the last operation issued.
Read	00h	30h	The read function reads from the nvSRAM array location specified by the address bytes.
Write	80h	10h[4]	Data is written to the SRAM array of nvSRAM. 10h is an optional command cycle for the nvSRAM write operation and a successful write will execute even without the host issuing this command.
Reset	FFh		Aborts the current operation (all writes and reads) and puts the nvSRAM in its power-up state. If an NV operation is in progress, it will be completed first and then the reset request will be serviced.
Software RECALL	FCh		Software RECALL
Software STORE	84h	A5h	Software STORE
AutoStore Disable	A3h		Disables the AutoStore
AutoStore Enable	ACh		Enables the AutoStore
Reserved	EEh		Reserved
Reserved	EFh		Reserved

Notes
2. A20 address bit should be set to LOW for the ×16 configuration.
3. Although these address bits are 'don't care', Cypress recommends that these bits are treated as 0s.
4. The 10h command at the end of the write cycle is optional and used only for flash compatibility.

Basic Operations

The following sections describe the nvSRAM commands.

Read ID (90h) Definition

The read ID function identifies that the device supports the ONFI specification. If the nvSRAM supports the ONFI specification, the ONFI signature shall be returned. The ONFI signature is the ASCII encoding of 'ONFI' where 'O' = 4Fh, 'N' = 4Eh, 'F' = 46h, and 'I' = 49h. Reading beyond four bytes will yield indeterminate values. Figure 7 and Figure 8 define the read ID behavior and timings.

For the read ID command, only the addresses of 00h and 20h are valid. Any other addresses, except 00h and 20h, following the read ID command (90h) will return invalid data to the host. To retrieve the ONFI signature, an address of 20h shall be entered.

For a device that supports 16-bit data access, the upper 8 bits DQ[15:8] are not used and are “Don’t Care” bits.

Figure 7. Read ID Operation Diagram for ONFI Signature

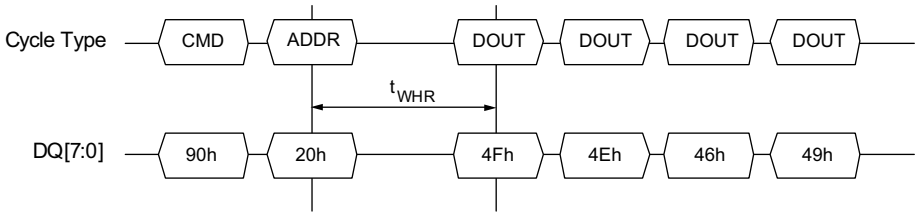
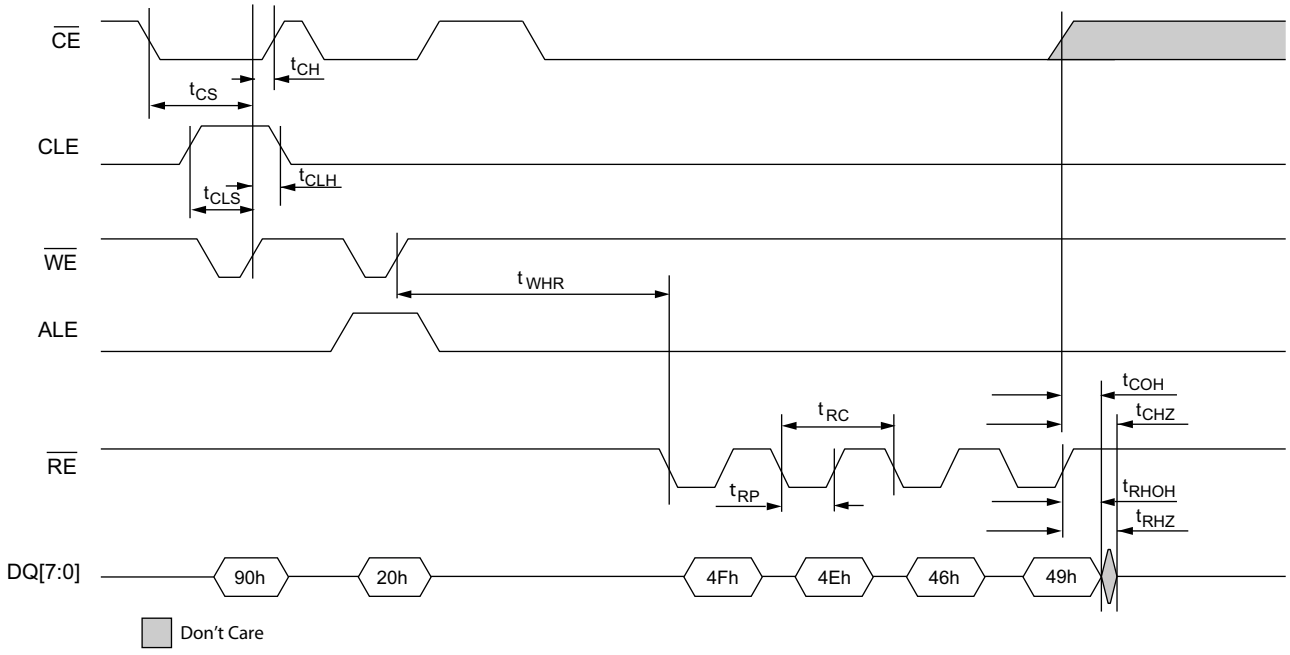


Figure 8. Read ID Timing Diagram for ONFI Signature



The read ID function can also be used to determine the JEDEC manufacturer ID and the device ID for the particular NAND part by specifying an address of 00h. Figure 9 defines the read ID behavior and timings for retrieving the device ID. Reading beyond the first two bytes yields undetermined value.

Figure 9. Read ID Operation Diagram for Manufacturer ID

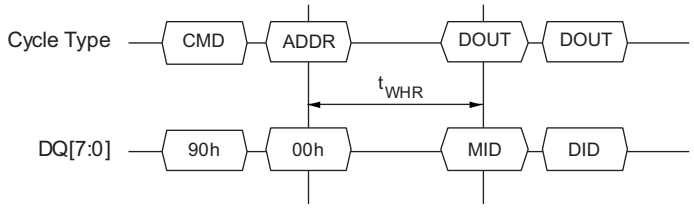
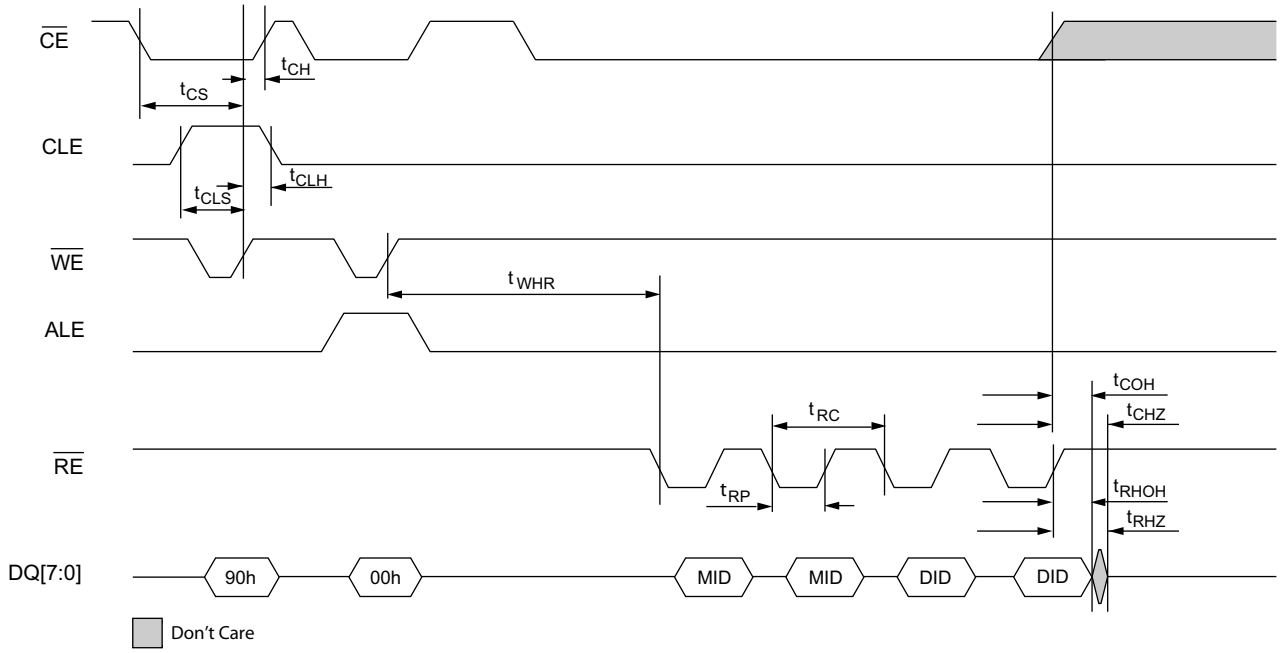


Figure 10. Read ID Timing Diagram for Manufacturer ID



MID is a 2-byte code consisting of the assigned manufacturer ID. MID registers are set in factory and are read-only registers for the user. This is the JEDEC-assigned manufacturer ID for Cypress. JEDEC assigns the manufacturer ID in different banks. The first eight bits represents the bank in which the ID is assigned. The next eight bits represent the manufacturer ID. The Cypress manufacturer ID is 34h in bank 0. Therefore, the manufacturer ID for all Cypress NAND interface nvSRAM products is:

MID: 0000_0000_0011_0100

DID is a 2-byte code consisting of the device ID for the part, assigned by Cypress. The device ID is 22h, 00h for the ×8 part and 22h, 40h for the ×16 part.

DID (×8): 0010_0010_0000_0000

DID (×16): 0010_0010_0100_0000

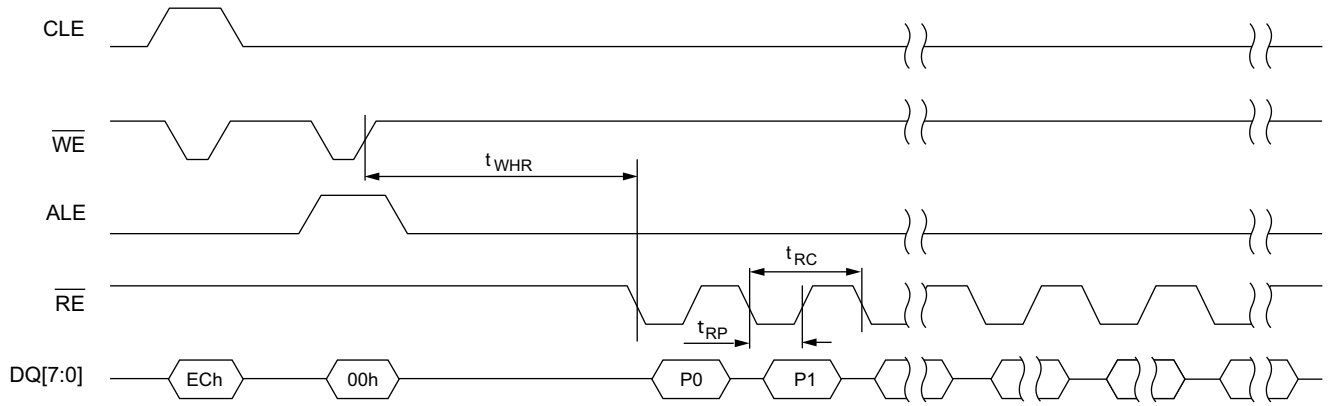
Read Parameter Page (ECh)

The read parameter page command (ECh) retrieves the data structure that describes the target's organization, features, timings, and other behavioral parameters. Figure 11 defines the read parameter page command. This command is accepted by the target only when the nvSRAM is idle. Writing ECh to the command register puts the target in the Read Parameter Page mode. The device stays in this mode until another valid command is issued.

When the ECh command is sent, followed by the 00h address cycle, the host should wait for at least t_{WHR} time before reading the parameter page byte. The nvSRAM starts sending parameter bytes for every $\overline{RE}$ toggle.

The read parameter page (ECh) output data can be used by the host to configure its internal settings for properly using the nvSRAM device. The parameter page data is static for every part. However, the value can be changed through the product cycle of the device. The host should interpret the data and configure itself accordingly.

Figure 11. Read Parameter Page command timing



Parameter Page Data Structure Definition

Table 4 defines the parameter page data structure of nvSRAM. The parameter page spans into multiple bytes and the least significant byte of the parameter corresponds to the first byte in the parameter page data structure. Values are reported in the parameter page in units of bytes. For a device that supports 16-bit data access, the upper 8 bits DQ[15:8] are not used and are “Don’t Care” bits.

Table 4. Parameter Page Data Structure Definition

Byte	Parameter Description[5]	Value: (For SDR Timing Mode - 3)		Value: (For SDR Timing Mode - 2)	
		×8	×16	×8	×16
0–3	Parameter page signature				
	Byte 0: 4Fh, “O”	4Fh	4Fh	4Fh	4Fh
	Byte 1: 4Eh, “N”	4Eh	4Eh	4Eh	4Eh
	Byte 2: 46h, “F”	46h	46h	46h	46h
	Byte 3: 49h, “I”	49h	49h	49h	49h
4–5	Revision number	00h, 02h	00h, 02h	00h, 02h	00h, 02h
	Bits 15–2: Reserved (0)				
	Bit 1: Supports ONFI version 1.0				
	Bit 0: Reserved (0)				

Note
5. ( ) designates values shipped from the factory.

Table 4. Parameter Page Data Structure Definition (continued)

Byte	Parameter Description[5]	Value: (For SDR Timing Mode - 3)		Value: (For SDR Timing Mode - 2)	
		×8	×16	×8	×16
6–7	Feature Supported	00h, 00h	00h, 01h	00h, 00h	00h, 01h
	Bits 15–1: Reserved (0)				
	Bit 0: When set to ‘1’, supports 16-bit data bus width				
8–9	Optional Command supported	00h, 00h	00h, 00h	00h, 00h	00h, 00h
	Bits 15–3: Reserved (0)				
	Bit 2: Supports Get Feature and Set Feature				
	Bit 1–0: Reserved (0)				
10–31	Reserved (0)	All bytes 00h			
32–43	Device manufacturer (12 ASCII characters)	All bytes 00h			
44–63	Device model (20 ASCII characters)	All bytes 00h			
64	JEDEC manufacturer ID	34h	34h	34h	34h
65–66	Date Code (Optional)	All bytes 00h			
67–79	Reserved (0)	All bytes 00h			
80–100	Unused (0)	All bytes 00h			
101	Number of address cycles Bits 7–4: Column address cycles Bits 3–0: Row address cycles	32h	32h	32h	32h
102–127	Unused (0)	All bytes 00h			
128	I/O pin capacitance	08h	08h	08h	08h
129–130	Timing mode support	00h, 08h	00h, 08h	00h, 04h	00h, 04h
	Bits 15–4: Reserved (0)				
	Bit 3: When set to ‘1’, supports timing mode 3				
	Bit 2: When set to ‘1’, supports timing mode 2				
	Bits 1–0: Reserved(0)				
131–140	Unused (0)	All bytes 00h			
141–163	Reserved (0)	All bytes 00h			
164–253	Unused (0)	All bytes 00h			
254–255	Integrity CRC	All bytes 00h			
256–768	Reserved (0)	All bytes 00h			

Read Status (70h) Definition

The read status command retrieves a status value for the last operation issued. See Table 5 on page 15 (Status field definition) for status register bit definitions. Figure 12 and Figure 13 define the read status behavior and timings.

SR: Status register bits are defined in Table 6 on page 15.

Figure 12. Read Status Operation

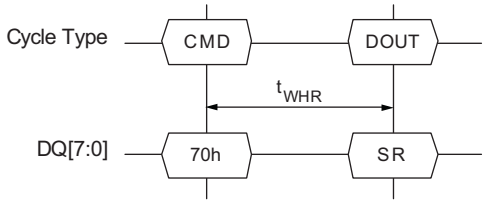
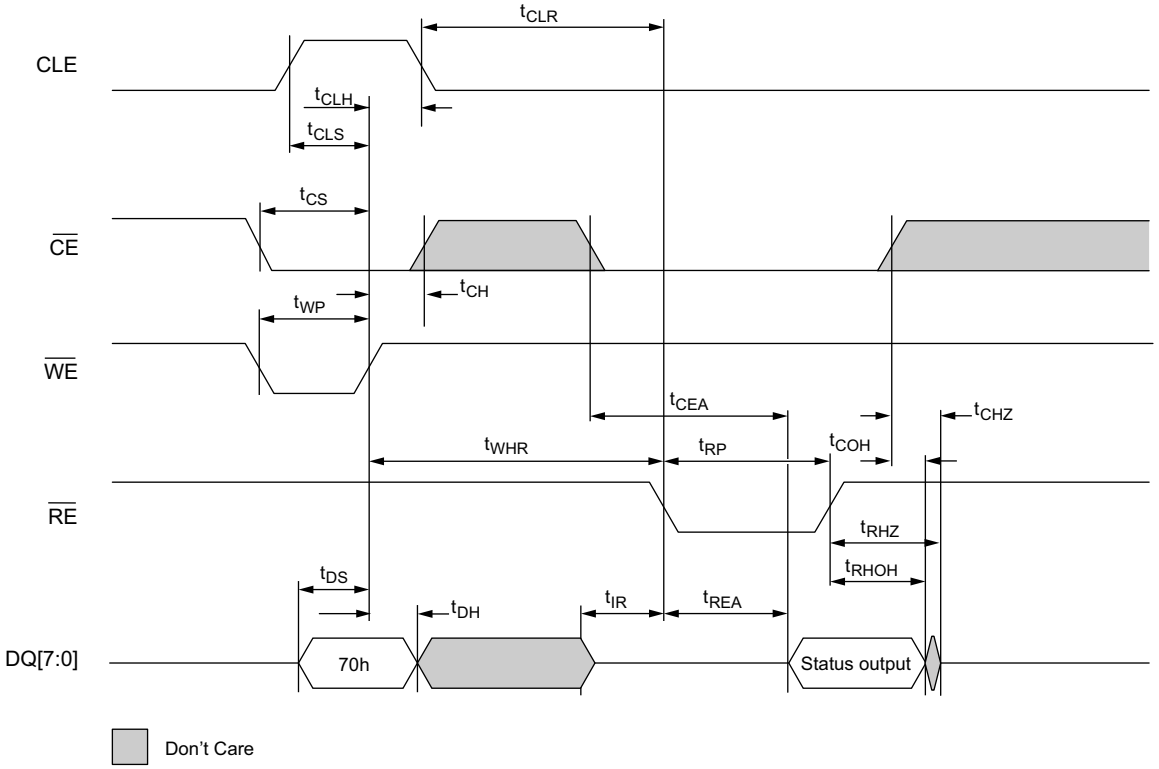


Figure 13. Read Status Timing



Status Field Definition

The read status register command returns the status register byte value (SR). If the RDY bit is cleared to zero, all other bits in the status byte (except $\overline{WP}$) are invalid and shall be ignored by the host. The RDY bit can be polled to check the ready or busy status while a nvSRAM STORE or Software RECALL cycle is in progress.

Table 5. Status Field Definition

SR bit	7	6	5	4	3	2	1	0
Status Register	$\overline{WP}$	RDY	X (0)	X (0)	X (0)	R (0)	X (0)	FAIL

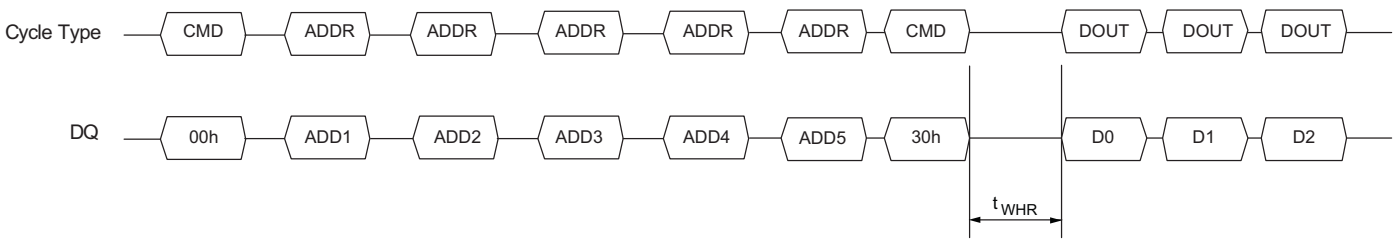
Table 6. Status Register Bit Definition

SR Bit	SR Bit Definition	SR Bit Description
Bit 0	FAIL	This shows the status of the last executed command by the nvSRAM. The FAIL bit is set to '1' if the last command did not execute successfully. The nvSRAM sets the FAIL bit when the last command sent by the host did not get registered properly, or the command did not receive the associated address bytes, or an invalid command was sent by the host.
Bit 1	Don't care	Reading this bit always returns a '0'.
Bit 2	Reserved	Reading this bit always returns a '0'.
Bit 3	Don't care	Reading this bit always returns a '0'.
Bit 4	Don't care	Reading this bit always returns a '0'.
Bit 5	Don't care	Reading this bit always returns a '0'.
Bit 6	RDY	If set to '1', the nvSRAM is ready for another command and all other bits in the status value are valid. If cleared to '0', the last command issued is not yet complete and the SR bits 5:0 are invalid and shall be ignored by the host. This bit impacts the value of R/$\overline{B}$ accordingly. This bit is set to '0' by the device while a STORE or Software RECALL is in progress.
Bit 7	$\overline{WP}$	If set to '1', the device is not write protected. If cleared to '0', the device is protected from writing. This bit shall always be valid regardless of the state of the RDY bit.

nvSRAM Burst Mode Read (00h, 30h)

The nvSRAM enters the Read mode when the host controller sends a 00h command, followed by five Address bytes, and the 30h second command cycle. After the read command is registered, the nvSRAM starts sending data out on its DQ bus after t_{REA} time from the falling edge of the $\overline{RE}$ control signal on every $\overline{RE}$ toggling. The nvSRAM allows reading in the Burst mode, where the host can continue reading the data from the device by repeatedly pulsing $\overline{RE}$ at the maximum t_{RC} rate. The host controller can read the entire memory by initiating a single read request. In the burst mode read, the internal address counter of the nvSRAM automatically increments to the next addressable location and the device continues sending data on its DQ bus. After the internal address counter reaches the last addressable memory location, the counter rolls over to the start address and continues sending data bytes. The device stays in the Read mode until the read is interrupted by another valid command. Refer to Figure 14 for the data output cycle timing.

Figure 14. Read Timing



nvSRAM Burst Write (80h, 10h)

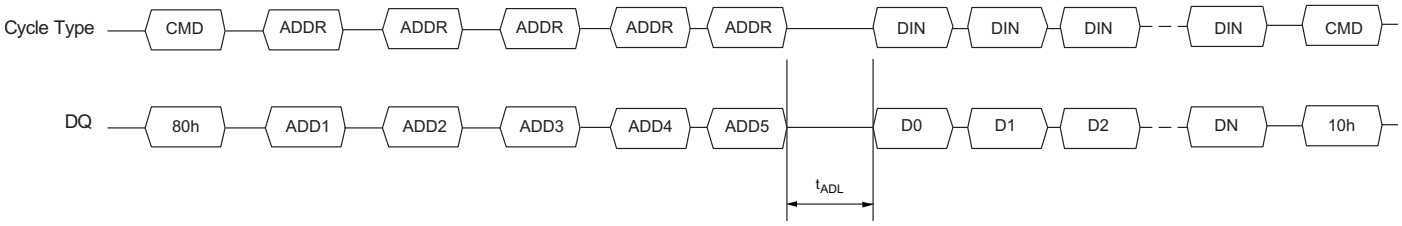
The nvSRAM enters the Write mode when the host controller sends an 80h command, followed by five Address bytes, and data bytes to be written. After the write command is initiated, subsequent data bytes are written to the nvSRAM on every $\overline{WE}$ toggle. The Write mode terminates when the host sends a 10h command at the end of a write data cycle. The nvSRAM supports the burst mode write operation, in which the host initiates the Write command, once at the beginning of the write cycle, and continues sending data bytes to be written by pulsing the $\overline{WE}$. The host should maintain the minimum write pulse width (t_{WP}) of $\overline{WE}$, and setup (t_{CS}) and hold (t_{CH}) criteria for the $\overline{CE}$ signal.

When the burst mode write is in progress, the internal address counter of the nvSRAM advances automatically after every data word write. After the internal address counter reaches the last addressable memory location, the address counter rolls over to the starting address and continues writing data from the starting address location by overwriting the previously written data.

Note Command 10h is an optional command for the nvSRAM write operation and a successful write executes without the host issuing this command. If the host executes the 10h command when the write operation is in progress, the ongoing Write mode is terminated.

Refer to Figure 15 for the data input cycle timing.

Figure 15. Write Timing



Reset (FFh) Definition

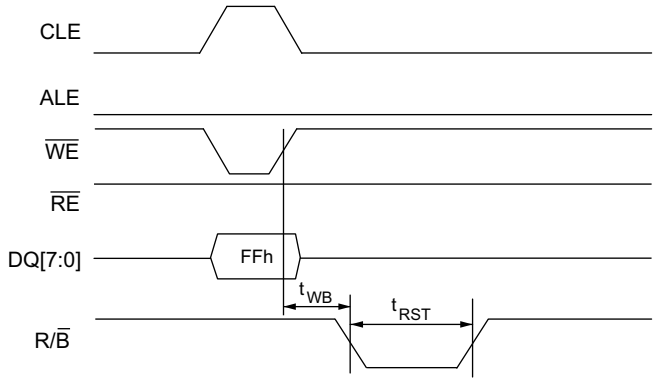
The Reset function puts the nvSRAM in its power-up state. The reset command can be executed when the device is in any state, except when a power-up RECALL operation is in progress. When the power-up RECALL operation is in progress, the reset command is not issued and the host must wait for R/$\overline{B}$ to become HIGH after the device is ready. Figure 16 defines the Reset behavior and timings.

For a device that supports 16-bit data access, the upper 8 bits DQ[15:8] are not used and are “Don’t Care” bits.

Note If the Reset (FFh) command is issued when any NV operation is in progress, then the reset request is executed only after the ongoing NV operation is completed. Depending upon the present state of the device, the t_{RST} timing varies based on the following:

- If the reset command is executed when the device is ready, it takes t_{SS} time to process the reset request.
- If the reset command is issued when the software RECALL cycle is in progress, it takes t_{RECALL} time to process the reset request.
- If the reset command is issued when a software or $\overline{HSB}$ STORE cycle is in progress, it takes t_{STORE} time to process the reset request.

Figure 16. Reset Timing Diagram

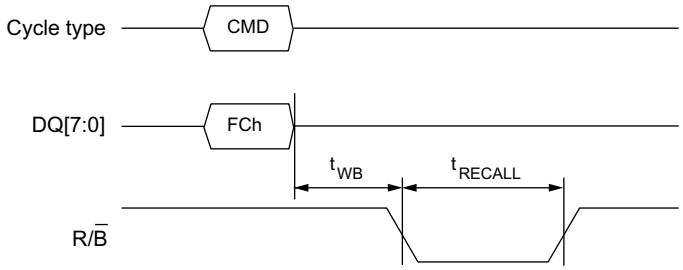


nvSRAM Software RECALL (FCh)

The software RECALL initiates a software RECALL operation in the nvSRAM. The command may be executed any time when the device is in the ready status. Figure 17 defines the nvSRAM Software RECALL behavior and timings. After the software RECALL command is registered by the nvSRAM, it takes t_{SS} time to process the software command before initiating the Software RECALL operation internally. All accesses to the nvSRAM, except reset (FFh) and read status (70h), are inhibited during t_{RECALL} time. During the RECALL operation, the nvSRAM sets the RDY bit of the status register to '0' and pulls the R/$\overline{B}$ pin to LOW for t_{RECALL} duration. After the RECALL completes, the RDY bit is set to '1' and R/$\overline{B}$ is pulled to HIGH by an external pull-up resistor indicating the ready status.

For a device that supports 16-bit data access, the upper 8 bits DQ[15:8] are not used and are "Don't Care" bits.

Figure 17. nvSRAM Software RECALL

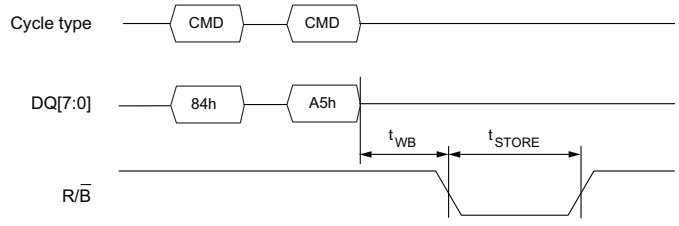


Software STORE (84h, A5h) in nvSRAM

Sending a software STORE command initiates a software STORE operation within the nvSRAM, regardless of whether there was an SRAM write or not. After the software STORE command is registered, the device takes t_{STORE} time to complete the STORE operation. All accesses to the nvSRAM, except Reset (FFh) and read status (70h), are inhibited during the STORE operation. After you initiate the STORE cycle, the nvSRAM pulls the R/$\overline{B}$ pin LOW for t_{STORE} duration. The RDY bit of the status register SR[6] transitions from '1' to '0' and remains at '0' until the STORE cycle is completed. Figure 18 defines the Software STORE behavior and timing. After the software STORE command is initiated, it pulls the R/$\overline{B}$ signal LOW for t_{STORE} time and all accesses, including FFh reset to the nvSRAM, are disabled.

For a device that supports 16-bit data access, the upper 8 bits DQ[15:8] are not used and are "Don't Care" bits.

Figure 18. Software STORE Timing

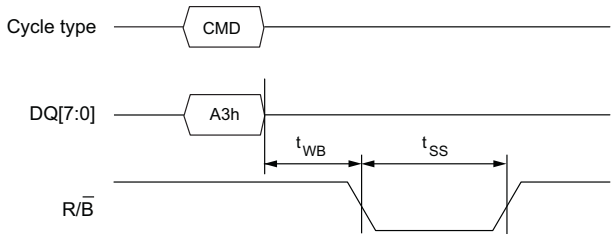


nvSRAM AutoStore Disable (A3h)

The AutoStore disable command (A3h) disables the nvSRAM AutoStore. All accesses to the nvSRAM, except Reset (FFh) and read status (70h), are inhibited during t_{SS} time. When the AutoStore Enable command is executing, the device pulls R/$\overline{B}$ LOW for t_{SS} time. Because this setting is volatile, you must perform a manual software STORE operation if this is desired to survive subsequent power cycles. The command may be executed any time when the device is in the ready status. Figure 19 defines the nvSRAM AutoStore disable timing.

For a device that supports 16-bit data access, the upper 8 bits DQ[15:8] are not used and are "Don't Care" bits.

Figure 19. nvSRAM AutoStore Disable

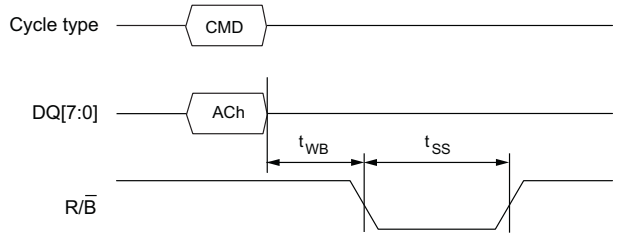


nvSRAM AutoStore Enable (ACh)

The AutoStore enable command (ACh) enables the nvSRAM AutoStore. All accesses to the nvSRAM, except reset (FFh) and read status (70h), are inhibited during t_{SS} time. When the AutoStore Enable command is executing, the device pulls R/$\overline{B}$ LOW for t_{SS} time. Because this setting is volatile, you must perform a manual software STORE operation if this is desired to survive subsequent power cycles. The command may be executed any time when the device is in the ready status. Figure 20 defines the nvSRAM AutoStore enable timing.

For a device that supports 16-bit data access, the upper 8 bits DQ[15:8] are not used and are "Don't Care" bits.

Figure 20. nvSRAM AutoStore Enable



Write Protect

The write protect feature disables the write operation in the nvSRAM. When the $\overline{WP}$ pin is pulled LOW externally by the host before initiating the write command (80h), the nvSRAM clears the $\overline{WP}$ (SR[7]) status in the status register and disables the write into the SRAM memory. However, writing into the status register is not protected. The status of the write protect pin is latched by the device along with the write command (80h) on the rising edge of the $\overline{WE}$ signal. After the write protect status is latched, it is locked for the current write cycle. After modifying the value of the $\overline{WP}$, the host shall not issue a new command to the device for at least t_{WW} time. The host must not toggle the $\overline{WP}$ pin during a command cycle. Figure 21 describes the t_{WW} timing requirement, which shows the start of an nvSRAM write command after toggling the $\overline{WP}$. The transition of the $\overline{WP}$ signal is asynchronous. The bus shall be idle for t_{WW} time after every $\overline{WP}$ transition from LOW to HIGH or HIGH to LOW before a new command is issued by the host.

Figure 21. Write Protect Disable Timing

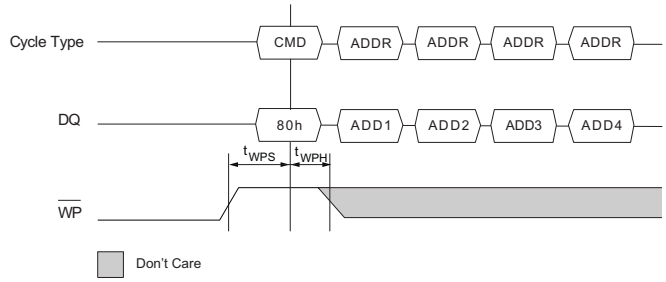
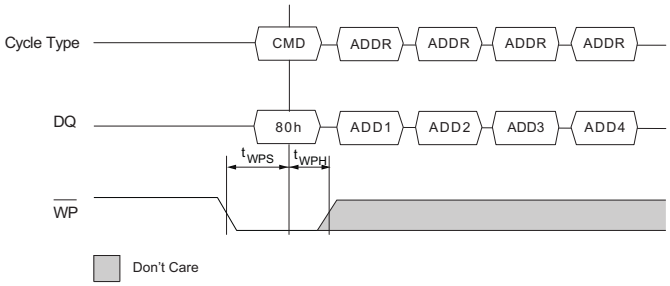


Figure 22. Write Protect Enable Timing



nvSRAM Store Operations

The nvSRAM stores data in the nonvolatile memory cell using one of the three store operations. These three operations are: AutoStore, automatically triggered on device power-down; Hardware STORE, activated by the $\overline{HSB}$; and Software STORE activated by issuing a software command.

AutoStore Operation

The AutoStore operation is a unique feature of the SONOS technology and is enabled by default on the device. During normal operation, the device draws current from V_{CC} to charge a capacitor connected to the V_{CAP} pin. This stored charge is used by the chip to perform a STORE operation during power-down. If the voltage on the V_{CC} pin drops below V_{SWITCH}, the part automatically disconnects the V_{CAP} pin from V_{CC} and a STORE operation is initiated with power provided by the V_{CAP} capacitor.

Note If the capacitor is not connected to the V_{CAP} pin, disable AutoStore using the AutoStore disable command (A3h). If AutoStore is enabled without a capacitor on the V_{CAP} pin, the device attempts an AutoStore operation without sufficient charge to complete the STORE. This corrupts the nvSRAM data.

Figure 23. AutoStore Mode

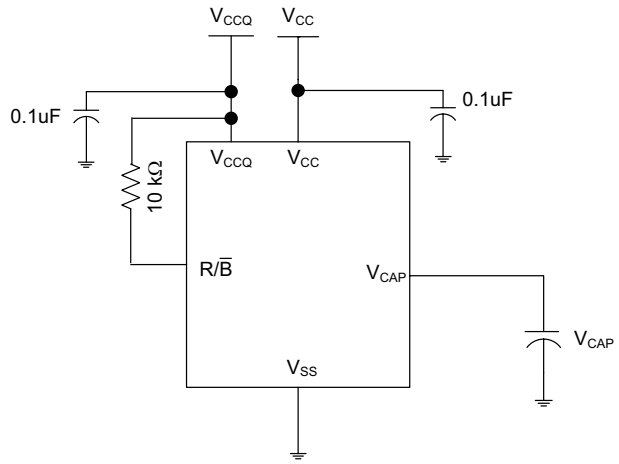


Figure 23 shows the proper connection of the storage capacitor (V_{CAP}) for automatic STORE operation. Refer to DC Electrical Characteristics on page 20 for the size of the V_{CAP}. The voltage on the V_{CAP} pin is driven to V_{VCAP} by a regulator on the chip. A pull-up resistor should be placed on $\overline{R/B}$ to hold it inactive during power-up. This pull-up resistor is only effective if the $\overline{R/B}$ signal is tristate during power-up. When the nvSRAM comes out of power-up RECALL, the host microcontroller must be active or the $\overline{R/B}$ held inactive until the host microcontroller comes out of reset. To reduce unnecessary nonvolatile STOREs, AutoStore and Hardware STORE operations are ignored unless at least one write operation has taken place since the most recent STORE or RECALL cycle.

Hardware STORE ($\overline{HSB}$) Operation

The device provides the $\overline{HSB}$ pin to control the Hardware STORE operation. The $\overline{HSB}$ pin is used to request a Hardware STORE cycle. When the $\overline{HSB}$ pin is driven LOW, the device conditionally initiates a STORE operation after t_{DELAY}. An actual STORE cycle begins only if a write to the SRAM has taken place since the last STORE or RECALL cycle. SRAM write operations that are in progress when $\overline{HSB}$ is driven LOW by any means are given time (t_{DELAY}) to complete before the STORE operation is initiated. However, any SRAM write cycles requested after $\overline{HSB}$ goes LOW are inhibited until $R/\overline{B}$ returns HIGH. $R/\overline{B}$ remains LOW by the device as long as $\overline{HSB}$ is LOW. Any SRAM read and write cycles are inhibited until $\overline{HSB}$ is returned HIGH by host microcontroller or any other external source. The $\overline{HSB}$ pin must be set to HIGH during the normal device operation. If $\overline{HSB}$ is not used in application, this pin should be pulled HIGH using an external pull-up resistor of value between 4.7 kΩ and 10 kΩ.

Software Store Operation

The software store operation is initiated by sending a Software STORE command (84h, A5h). The nvSRAM initiates a STORE cycle irrespective of whether the write latch is set or not. Refer to Software STORE (84h, A5h) in nvSRAM on page 17 for further details.

nvSRAM RECALL Operations

The nvSRAM recalls data from the nonvolatile memory cell using one of the two recall operations. These two recall operations are: Hardware Recall, activated automatically by the device during a power cycle or brown out, and a software initiated RECALL cycle.

Hardware RECALL (Power Up)

During power-up or after any low-power condition ($V_{CC} < V_{SWITCH}$), an internal RECALL request is latched. When V_{CC} again exceeds the V_{SWITCH} on power-up, a RECALL cycle is automatically initiated and takes $t_{HRECALL}$ to complete. During this time, the $R/\overline{B}$ pin is driven LOW by the nvSRAM and all reads and writes to nvSRAM inhibited.

Software Recall

The software recall operation is initiated by sending a Software RECALL command (FCh). The nvSRAM initiates a RECALL cycle and overwrites the SRAM data with the recalled data from the nonvolatile cell. Refer to the nvSRAM Software RECALL (FCh) on page 17 for further details.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. These user guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Maximum accumulated storage time

At 150 °C ambient temperature 1000h

At 85 °C ambient temperature ..... 20 Years

Maximum Junction temperature ..... 150 °C

Supply voltage on V_{CC} relative to V_{SS} .....–0.5 V to +4.1 V

Supply voltage on V_{CCQ} relative to V_{SS} .....–0.5 V to +2.4 V

DC voltage applied to outputs in HIGH Z State .....–0.5 V to V_{CCQ} + 0.5 V

Input voltage .....–0.5 V to V_{CCQ} + 0.5 V

Transient voltage (< 20 ns) on any pin to ground potential .....–2.0 V to V_{CCQ} + 2.0 V

Package power dissipation capability (T_A = 25 °C) ..... 1.0 W

Package Pb soldering temperature (3 seconds) ..... +260 °C

DC output current (1 output at a time, 1s duration). .... 20 mA

Static discharge voltage (per MIL-STD-883, Method 3015) ..... > 2001 V

Latch up current ..... > 140 mA

Operating Range

Range	Ambient Temperature (T_A)	V_{CC}	V_{CCQ}
Industrial	–40 °C to +85 °C	2.7 V to 3.6 V	1.70 V to 1.95 V

DC Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		Min	Typ [6]	Max	Unit
V_{CC}	Core power supply			2.7	3.0	3.6	V
V_{CCQ}	I/O power supply			1.70	1.80	1.95	V
I_{CC1}	Average V_{CC} current	$t_{RC} \geq$ 30 ns		–	–	100	mA
I_{CCQ1}	Average V_{CCQ} current	$t_{RC} \geq$ 30 ns Values obtained without output loads (I_{OUT} = 0 mA)	CY14V116F7	–	–	30	mA
			CY14V116G7	–	–	60	mA
I_{CC2}	Average V_{CC} current during STORE	All inputs don't care, V_{CC} = V_{CC} (Max) Average current for duration t_{STORE}		–	–	10	mA
I_{CC3}	Average V_{CC} current $t_{RC} \geq$ 200 ns; V_{CC} = V_{CC}(Typ), 25 °C	All inputs cycling at CMOS levels.		–	–	50	mA
I_{CCQ3}	Average V_{CCQ} current $t_{RC} \geq$ 200 ns; V_{CCQ} = V_{CCQ}(Typ), 25 °C	All inputs cycling at CMOS levels. Values obtained without output loads (I_{OUT} = 0 mA)	CY14V116F7	–	–	15	mA
			CY14V116G7	–	–	30	mA
I_{CC4}[7]	Average V_{CAP} current during AutoStore cycle	All inputs don't care. Average current for duration t_{STORE}		–	–	6	mA
I_{SB}	V_{CC} standby current	$\overline{CE} \geq (V_{CCQ} – 0.2 V)$. $V_{IN} \leq$ 0.2 V or $\geq (V_{CCQ} – 0.2 V)$		–	–	5	mA
I_{SB1}	V_{CCQ} standby current			–	–	2	mA
I_{IX}	Input leakage current	V_{CCQ} = V_{CCQ} (Max), $V_{SS} \leq V_{IN} \leq V_{CCQ}$		–1	–	+1	µA
I_{OZ}	Output leakage current	V_{CCQ} = V_{CCQ} (Max), $V_{SS} \leq V_{IN} \leq V_{CCQ}$; output disabled		–1	–	+1	µA
V_{IH}	Input HIGH voltage			0.8 × V_{CCQ}	–	V_{CCQ} + 0.3	V
V_{IL}	Input LOW voltage			V_{SS} – 0.3	–	0.2 × V_{CCQ}	V
V_{OH}	Output HIGH voltage	I_{OH} = -100 µA		V_{CCQ} – 0.1	–	V_{CCQ}	V

Notes

6. Typical values are at 25 °C, V_{CC} = V_{CC}(Typ) and V_{CCQ} = V_{CCQ}(Typ). Not 100% tested.
7. This parameter is only guaranteed by design and is not tested.

DC Electrical Characteristics (continued)

Over the Operating Range

Parameter	Description	Test Conditions	Min	Typ [6]	Max	Unit
V_{OL}	Output LOW voltage (except R/$\overline{B}$)	I_{OL} = 100 µA	–	–	0.1	V
	Output LOW voltage (for R/$\overline{B}$)	I_{OL} = 3 mA	–	–	0.2	V
V_{CAP}[8]	Storage capacitor	Between V_{CAP} pin and V_{SS}	19.8	22.0	82.0	µF
V_{VCAP}[9, 10]	Maximum voltage driven on V_{CAP} pin by the device	V_{CC} = V_{CC}(Max)	–	–	5.0	V

Data Retention and Endurance

Over the Operating Range

Parameter	Description	Min	Unit
$DATA_R$	Data retention	20	Years
NV_C	Nonvolatile STORE operations	1,000,000	Cycles

Capacitance

Parameter [10]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance on clock and input pins	T_A = 25 °C, f = 1 MHz, V_{CC} = V_{CC}(Typ), V_{CCQ} = V_{CCQ}(Typ)	10	pF
C_{IO}	Input capacitance on data and I/O pins		10	pF
C_{OTHER}	Capacitance on all other control pins		10	pF

Thermal Resistance

Parameter [10]	Description	Test Conditions	165-ball FBGA	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, according to EIA / JESD51.	15.6	°C/W
Θ_{JC}	Thermal resistance (junction to case)		2.9	°C/W

Notes

8. Min V_{CAP} value guarantees that there is a sufficient charge available to complete a successful AutoStore operation. Max V_{CAP} value guarantees that the capacitor on V_{CAP} is charged to a minimum voltage during a Power-Up RECALL cycle so that an immediate power-down cycle can complete a successful AutoStore. Therefore, it is always recommended to use a capacitor within the specified min and max limits.
9. Maximum voltage on V_{CAP} pin (V_{VCAP}) is provided for guidance when choosing the V_{CAP} capacitor. The voltage rating of the V_{CAP} capacitor across the operating temperature range should be higher than the V_{VCAP} voltage.
10. These parameters are guaranteed by design and are not tested.

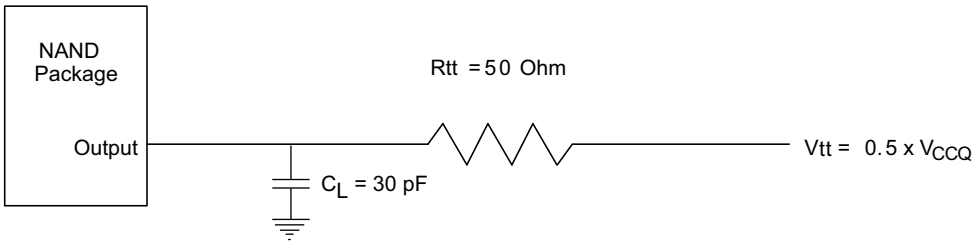
AC Test Conditions

Input pulse levels..... 0 V to V_{CCQ}

Input rise and fall times (10% - 90%)..... 5 ns

Input and output timing reference levels.....$V_{CCQ}/2$

Figure 24. Driver Output Reference



AC Switching Characteristics

Timing Modes

Over the Operating Range

Parameter[11]	Description	Mode 2		Mode 3		Unit
		35 ns		30 ns		
		Min	Max	Min	Max	
t_{ADL}	Address cycle to data loading time	100	–	100	–	ns
t_{ALH}	ALE hold time	10	–	5	–	ns
t_{ALS}	ALE setup time	15	–	10	–	ns
t_{AR}	ALE to $\overline{RE}$ delay	10	–	10	–	ns
t_{CEA}	$\overline{CE}$ access time	–	30	–	25	ns
t_{CH}	$\overline{CE}$ hold time	10	–	5	–	ns
t_{CHZ}[12]	$\overline{CE}$ HIGH to output HIGH Z	–	50	–	50	ns
t_{CLH}	CLE hold time	10	–	5	–	ns
t_{CLR}	CLE to $\overline{RE}$ delay	10	–	10	–	ns
t_{CLS}	CLE setup time	15	–	10	–	ns
t_{COH}	$\overline{CE}$ HIGH to output hold	15	–	15	–	ns
t_{IR}	Output HIGH Z to $\overline{RE}$ LOW	0	–	0	–	ns
t_{CS}	$\overline{CE}$ setup time	25	–	25	–	ns
t_{DH}	Data hold time	5	–	5	–	ns
t_{DS}	Data setup time	15	–	10	–	ns
t_{RC}	$\overline{RE}$ cycle time	35	–	30	–	ns
t_{REA}	$\overline{RE}$ access time	–	25	–	20	ns
t_{REH}	$\overline{RE}$ HIGH hold time	15	–	10	–	ns
t_{RHOH}	$\overline{RE}$ HIGH to output hold	15	–	15	–	ns
t_{RHW}	$\overline{RE}$ HIGH to $\overline{WE}$ LOW	100	–	100	–	ns
t_{RHZ}[12]	$\overline{RE}$ HIGH to output HIGH Z	–	100	–	100	ns
t_{RP}	$\overline{RE}$ pulse width	17	–	15	–	ns
t_{RST}[13]	Device reset time	–	500/600/8000	–	500/600/8000	µs
t_{WC}	$\overline{WE}$ cycle time	35	–	30	–	ns
t_{WB}	$\overline{WE}$ HIGH or clock rising edge to SR[6] LOW	–	100	–	100	ns
t_{WH}	$\overline{WE}$ HIGH hold time	15	–	10	–	ns
t_{WHR}	$\overline{WE}$ command, address or data input cycle to data output cycle	80	–	80	–	ns
t_{WP}	$\overline{WE}$ pulse width	17	–	15	–	ns
t_{WW}	$\overline{WP}$ transition to command cycle	100	–	100	–	ns
t_{WPS}	$\overline{WP}$ set up time	25	–	25	–	ns
t_{WPH}	$\overline{WP}$ hold time	10	–	10	–	ns

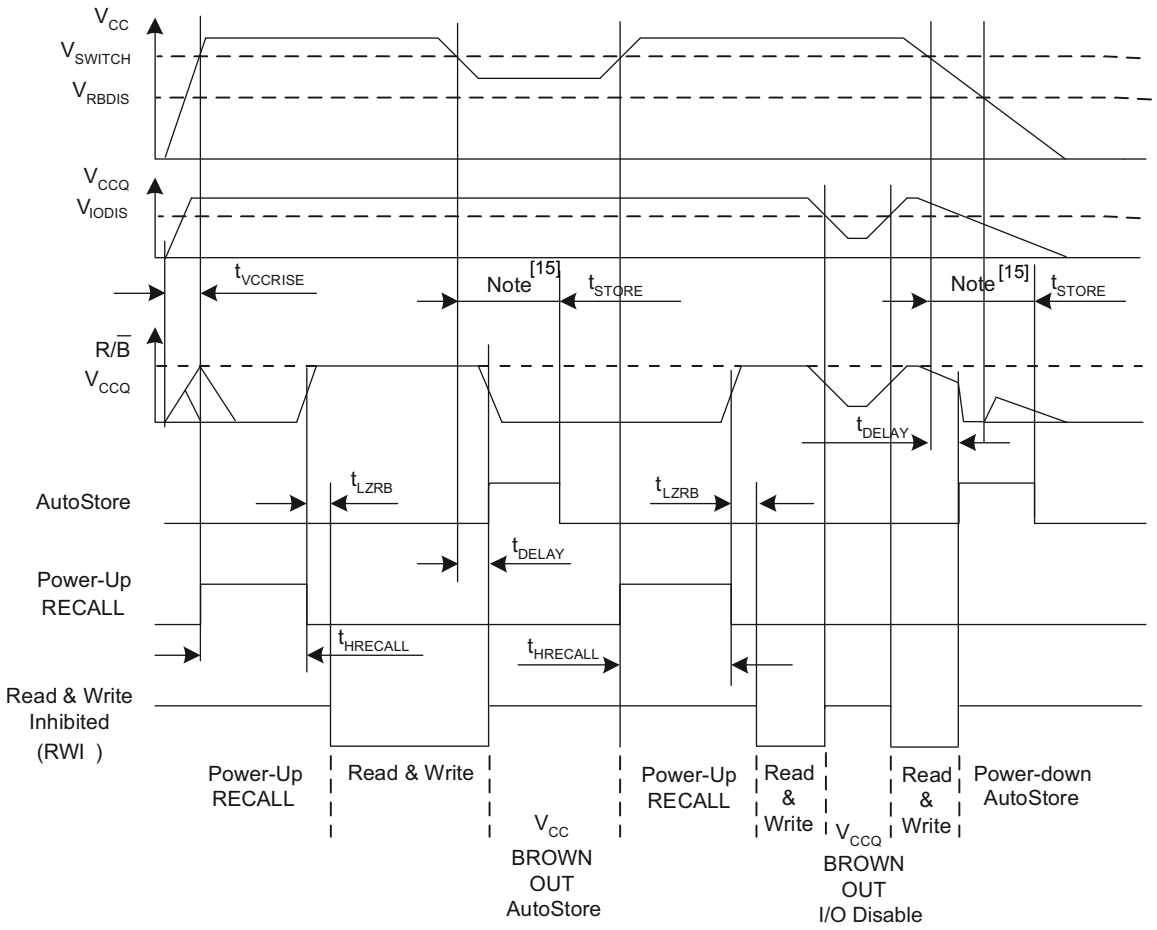
Notes

11. Test conditions assume a signal transition time of 5 ns or less, timing reference levels of $V_{CCQ}/2$, input pulse levels of 0 to V_{CCQ}(Typ), and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance shown in Figure 24.
12. These parameters are guaranteed by design and are not tested.
13. There are three maximums listed for t_{RST}: Device is not performing any STORE or RECALL operation/Device is performing RECALL operation/Device is performing STORE operation.

nvSRAM AutoStore/Power-Up RECALL Characteristics

Parameter	Description	Min	Max	Unit
$t_{HRECALL}$ [14]	Power-Up RECALL duration	–	30	ms
t_{STORE} [15]	STORE cycle duration	–	8	ms
t_{DELAY} [16]	Time allowed to complete SRAM write cycle	–	45	ns
$t_{VCCRISE}$ [17]	V_{CC} rise time	150	–	µs
V_{SWITCH}	LOW voltage trigger level for V_{CC}	–	2.65	V
V_{IODIS}	I/O disable voltage on V_{CCQ}	–	1.6	V
t_{LZRB} [17]	R/$\overline{B}$ to output active time	–	5	µs
V_{RBDIS} [17]	R/$\overline{B}$ output disable voltage on V_{CC}	–	1.9	V

Figure 25. AutoStore or Power-Up RECALL [18, 19]



Notes

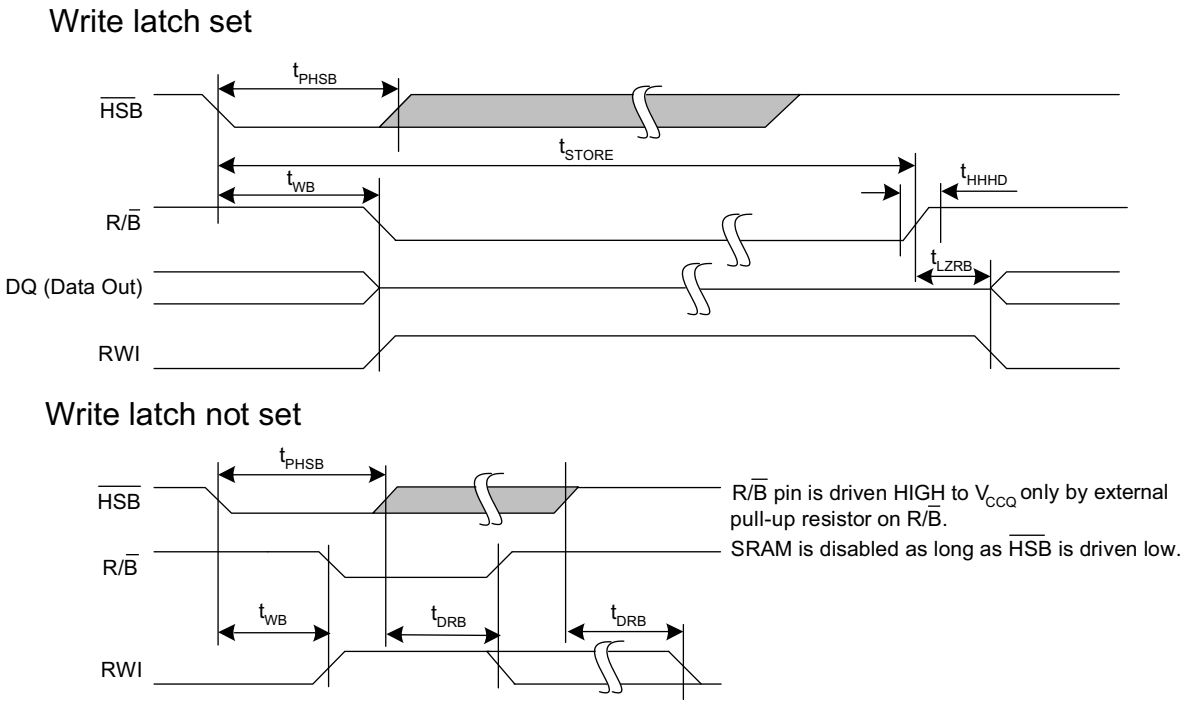
14. $t_{HRECALL}$ starts from the time V_{CC} rises above V_{SWITCH}.
15. If an SRAM write has not taken place since the last nonvolatile cycle, no AutoStore or Hardware STORE takes place.
16. On a Hardware STORE and AutoStore initiation, SRAM write operation continues to be enabled for time t_{DELAY}.
17. These parameters are guaranteed by design and are not tested.
18. Read and Write cycles are ignored during STORE, RECALL, and while V_{CC} is below V_{SWITCH}.
19. Pin is driven HIGH to V_{CCQ} only when an external pull-up is connected on the R/$\overline{B}$ pin. R/$\overline{B}$ driver is disabled.

Hardware STORE Characteristics

Over the Operating Range

Parameter	Description	Min	Max	Unit
t_{PHSB}	Hardware STORE pulse width	15	–	ns
t_{DRB}	R/$\overline{B}$ to output active time when write latch not set	–	100	ns
t_{RECALL}	RECALL duration	–	600	µs
t_{SS}[20]	Soft sequence processing time	–	500	µs

Figure 26. Hardware STORE Cycle [21]

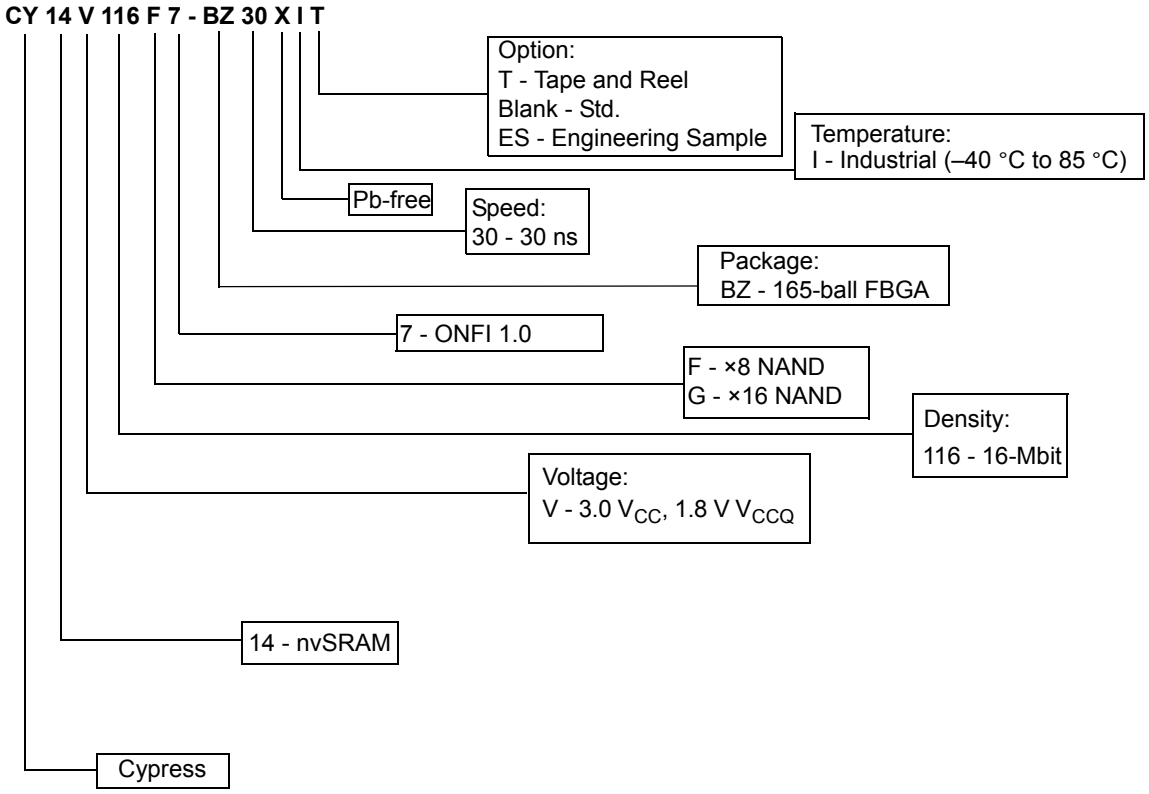


Notes
20. This is the amount of time it takes to take action on a soft sequence command. Vcc power must remain high to effectively register command.
21. If an SRAM write has not taken place since the last nonvolatile cycle, AutoStore or Hardware STORE is not initiated.

Ordering Information

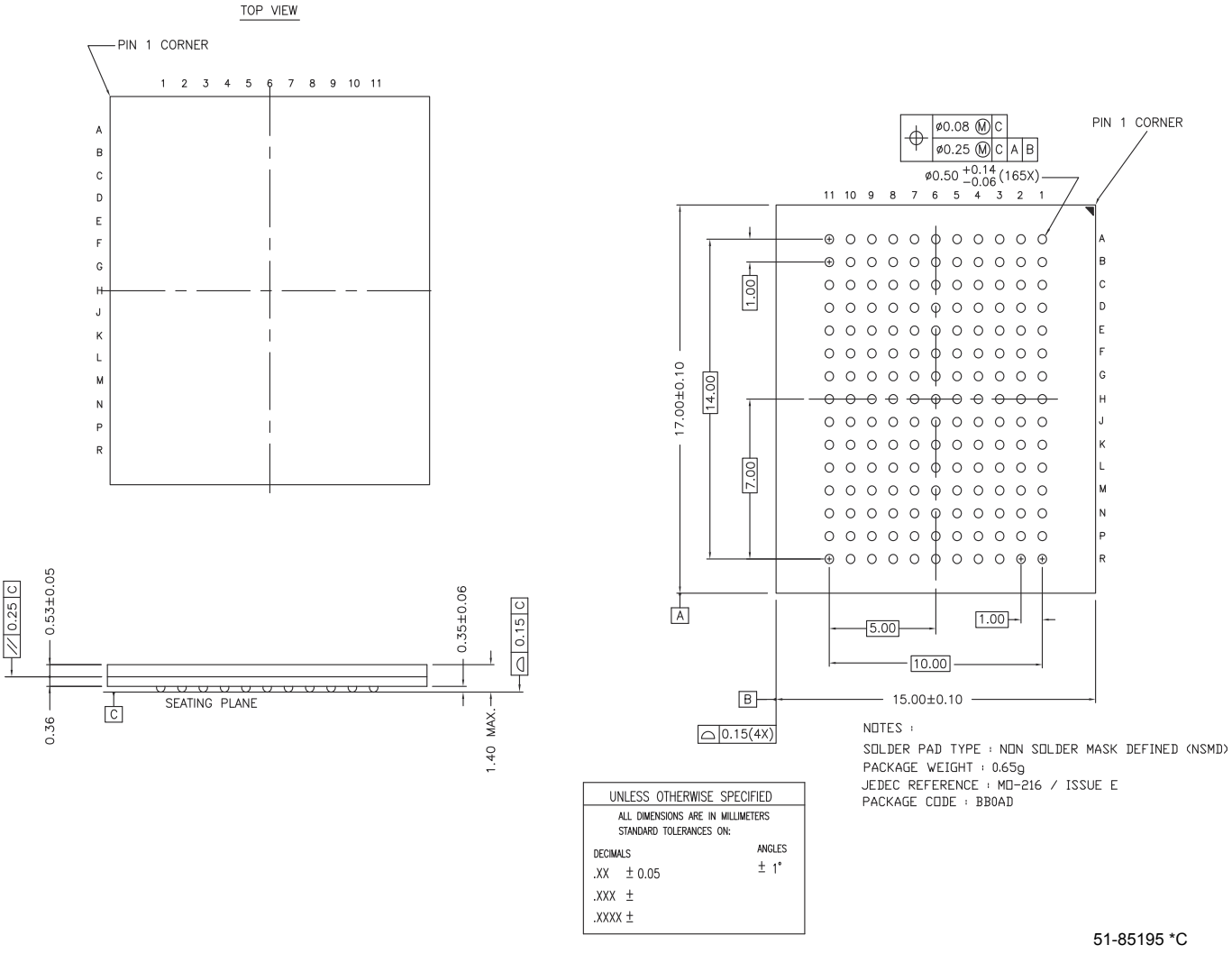
Ordering Code	Package Diagram	Package Type	Operating Range
CY14V116G7-BZ30XI	51-85195	165-ball FBGA	Industrial
CY14V116G7-BZ30XIT			

Ordering Code Definitions



Package Diagram

Figure 27. 165-ball FBGA (15 mm × 17 mm × 1.40 mm) Package Outline (51-85195)



Acronyms

Acronym	Description
ALE	address latch enable
$\overline{CE}$	chip enable
CLE	command latch enable
CMOS	complementary metal oxide semiconductor
CRC	cyclic redundancy check
EIA	electronic industries alliance
I/O	input/output
JEDEC	joint electron devices engineering council
JESD	JEDEC Standards
nvSRAM	nonvolatile static random access memory
ONFI	open NAND flash interface
NV	nonvolatile
$\overline{RE}$	read enable
RoHS	restriction of hazardous substances
R/$\overline{W}$	read/write
RWI	read and write inhibited
SR	status register
$\overline{WE}$	write enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
Hz	hertz
kHz	kilohertz
kΩ	kiloohm
MHz	megahertz
MT/s	million transfers for second
µA	microampere
µF	microfarad
µs	microsecond
mA	milliampere
ms	millisecond
ns	nanosecond
Ω	ohm
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY14V116F7/CY14V116G7, 16-Mbit nvSRAM with Asynchronous NAND Interface Document Number: 001-75528				
Rev.	**ECN No.**	**Submission Date**	**Orig. of Change**	**Description of Change**
**	3508602	02/02/2012	GVCH	New data sheet.
*A	3746140	09/17/2012	GVCH	Replaced CY14V116FX and CY14V116GX with CY14V116F7 and CY14V116G7. Updated Basic Operations (Updated Table 4, updated nvSRAM Burst Write (80h, 10h) (description), updated Reset (FFh) Definition (no change in description, updated Figure 16 only), updated nvSRAM Software RECALL (FCh) (no change in description, updated Figure 17 only), updated Software STORE (84h, A5h) in nvSRAM (no change in description, updated Figure 18 only), updated nvSRAM AutoStore Disable (A3h) (no change in description, updated Figure 19 only), updated nvSRAM AutoStore Enable (ACh) (no change in description, updated Figure 20 only, updated Write Protect (no change in description, added Figure 21 and Figure 22 only)). Updated Maximum Ratings (Removed “Ambient temperature with power applied” and added “Maximum junction temperature”). Updated DC Electrical Characteristics (Splitted the Test Conditions of I_{CCQ1}, I_{CCQ3} parameters into two rows (one for CY14V116F7 and another for CY14V116G7), retained the original values for CY14V116F7 row and added new values for CY14V116G7 row). Updated Capacitance (Changed maximum value of C_{IN} and C_{IO} parameters from 7 pF to 11.5 pF). Updated AC Switching Characteristics (Updated Timing Modes (Added t_{WPS}, t_{WPH} parameters and their details)). Added nvSRAM AutoStore/Power-Up RECALL Characteristics table and Switching Waveforms (corresponding to it (Figure 25)). Added Hardware STORE Characteristics and Switching Waveforms (corresponding to it (Figure 26)).
*B	3944873	03/26/2013	GVCH	Changed V_{CCQ} max spec value from 1.9 V to 1.95 V Removed Set Features and Get Features command Updated Parameter Page Data Structure Definition Removed t_{CEH} parameter spec Updated Capacitance (Changed maximum value of C_{IN} and C_{IO} parameters from 11.5 pF to 8 pF). Updated Capacitance (Changed maximum value of C_{OTHER} parameter from 20 pF to 8 pF). Changed I_{SB} parameter spec value 15 mA to 5 mA Changed I_{SB1} parameter spec value from 5 mA to 2 mA
*C	4260504	01/24/2014	GVCH	Added footnote 1 and 2 Updated note 4 for more clarity Updated AutoStore Operation: Removed sentence “The HSB signal is monitored by the system to detect if an AutoStore cycle is in progress.” Changed V_{CAP} min value from 20 µF to 19.8 µF Added DID values for ×8 and ×16 part Updated Figure 25 for more clarity
*D	4286722	02/20/2014	GVCH	Minor formatting correction in ordering code diagram.

Document History Page

Document Title: CY14V116F7/CY14V116G7, 16-Mbit nvSRAM with Asynchronous NAND Interface Document Number: 001-75528				
Rev.	**ECN No.**	**Submission Date**	**Orig. of Change**	**Description of Change**
*E	4417851	06/24/2014	GVCH	Added reserved commands to Table 3 DC Electrical Characteristics: Added footnote 7 Updated maximum value of V_{VCAP} parameter from 4.5 V to 5.0 V Capacitance: Updated C_{IN}, C_{IO} and C_{OTHER} value from 8 pF to 10 pF nvSRAM AutoStore/Power-Up RECALL Characteristics: Removed t_{RBHD} ($R/\overline{B}$ HIGH active time) spec Updated Figure 25 Updated Thermal Resistance values
*F	4432183	GVCH	07/07/2014	DC Electrical Characteristics: Updated maximum value of V_{CAP} parameter from 120.0 µF to 82.0 µF
*G	4456803	ZSK	07/31/2014	No content update
*H	4541059	GVCH	10/16/2014	Updated DC Electrical Characteristics: Updated test conditions of I_{CC1}, I_{CCQ1}, I_{CC3}, I_{CCQ3} parameters.
*I	4568158	GVCH	11/13/2014	Added related documentation hyperlink in page 1.
*J	4616093	GVCH	01/07/2015	Changed datasheet status from Preliminary to Final. Removed CY14V116F7-BZ30XIES and CY14V116G7-BZ30XIES part numbers. Added CY14V116G7-BZ30XI and CY14V116G7-BZ30XIT part numbers.

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