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CY24142

MediaClock™ Multimedia Clock Generator

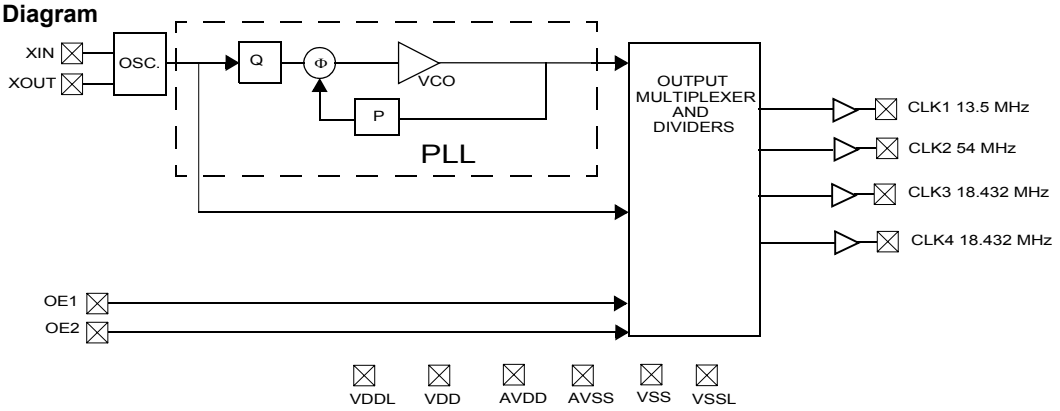
Features

- **Integrated phase-locked loop (PLL)**
- **Low-jitter, high-accuracy outputs**
- **3.3V operation**

Benefits

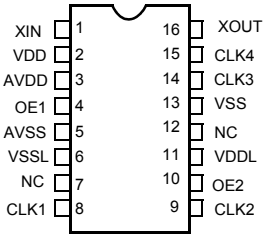
- Integrated high-performance PLL eliminates the need for — external loop filter components
- Meets critical timing requirements in complex system designs
- Enables application compatibility

Logic Block Diagram



Pin Configuration

CY24142
16-pin TSSOP



Frequency Table

Part Number	Outputs	Input Frequency	Output Frequency Range
CY24142-01	4	18.432	13.5 MHz, 54 MHz, 2 x 18.432 MHz

Output Enable Options[1]

OE2	OE1	CLK1	CLK2	CLK3	CLK4	Unit
0	0	13.5	OFF	OFF	OFF	MHz
0	1	13.5	54	18.432	OFF	MHz
1	0	13.5	OFF	OFF	18.432	MHz
1	1	13.5	54	18.432	18.432	MHz

Note:
1. Output driven LOW when “OFF.”

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Pin Description

Pin Name	Pin Number	Pin Description
XIN	1	**Crystal Input**.
V_{DD}	2	**Voltage Supply**.
AV_{DD}	3	**Analog Voltage Supply**.
OE1	4	**Output Enable 1, 0 = CLK 2 and CLK3 off, 1 = CLK 2 and CLK3 on;** weak internal pull-down.
AV_{SS}	5	**Analog Ground**.
V_{SSL}	6	**V_{DDL} Ground**.
NC	7	**No Connect**; leave floating.
CLK1	8	**13.5-MHz Clock Output**.
CLK2	9	**54-MHz Clock Output**; controlled by OE1.
OE2	10	**Output Enable 2, 0 = CLK4 off, 1 = CLK4 on**; weak internal pull-down.
V_{DDL}	11	**Voltage Supply**.
NC	12	**No Connect**; leave floating.
V_{SS}	13	**Ground**.
CLK3	14	**18.432-MHz Buffered Reference Output**, controlled by OE1.
CLK4	15	**18.432-MHz Buffered Reference Output**, controlled by OE2.
XOUT	16	**Crystal Output**.

Layout Recommendations

The X_{IN} and X_{OUT} traces and pads as well as the crystal should be placed away from any clock traces or noise sources. Noise coupling into the X_{IN} and X_{OUT} traces may cause start-up problems. A pad for a resistor to ground should be laid out on the X_{OUT} trace to be stuffed if necessary, in case start-up issues occur.

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Absolute Maximum Conditions

(Above which the useful life may be impaired. For user guidelines, not tested.

Supply Voltage (V_{DD}, AV_{DD}, V_{DDL}) .....–0.5 to +7.0V

DC Input Voltage.....–0.5V to V_{DD} + 0.5

Storage Temperature (Non-Condensing).... –55°C to +125°C

Junction Temperature..... –40°C to +125°C

Data Retention @ Tj=125°C.....> 10 years

Package Power Dissipation..... 350 mW

ESD (Human Body Model) MIL-STD-883..... 2000V

Recommended Crystal Specifications

Parameter	Description	Comments	Min.	Typ.	Max.	Unit
F_{NOM}	Nominal crystal frequency	Parallel resonance, fundamental mode, AT cut		18.432		MHz
C_{LNOM}	Nominal load capacitance			14		pF
R_1	Equivalent series resistance (ESR)	Fundamental mode			25	Ω
R_3/R_1	Ratio of third overtone mode ESR to fundamental mode ESR	Ratio used because typical R_1 values are much less than the maximum spec	3			
DL	Crystal drive level	No external series resistor assumed		0.5	2	mW

Recommended Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Unit
V_{DD}, AV_{DD}, V_{DDL}	Supply Voltage	3.15	3.45	3.6	V
T_A	Ambient Temperature	0		85	°C
C_{LOAD}	Max. Load Capacitance			15	pF
T_{PU}	Power-up time for all V_{DD}s to reach minimum specified voltage (power ramps must be monotonic)	0.05		500	ms

DC Electrical Specifications

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
I_{OH}[2]	Output High Current	$V_{OH} = V_{DD} – 0.5$, V_{DD}/V_{DDL} = 3.45V	12	24		mA
I_{OL}[2]	Output Low Current	V_{OL} = 0.5, V_{DD}/V_{DDL} = 3.45V	12	24		mA
I_{IH}	Input High Current	$V_{IH} = V_{DD}$			50	µA
I_{IL}	Input Low Current	V_{IL} = 0V		5	10	µA
V_{IH}	Input High Voltage	CMOS levels, 70% of V_{DD}	0.7			V_{DD}
V_{IL}	Input Low Voltage	CMOS levels, 30% of V_{DD}			0.3	V_{DD}
I_{VDD}	Supply Current	AV_{DD}/V_{DD} Current			25	mA
I_{VDDL}	Supply Current	V_{DDL} Current			20	mA
R_{DOWN}	Pull-down resistor on Inputs	V_{DD} = 3.15 to 3.6V, measured V_{IN} = 3.45V		100	150	kΩ
C_{XTAL}[2]	Crystal Load Capacitance	Total effective load of internal load caps		12.9		pF

Cycle-Cycle Jitter Specifications (VDD = 3.15V – 3.6V)

Parameter	Description	Conditions	1σ	Typ.	Max.	Unit
t_9	Clock Jitter–peak-peak	Cycle-Cycle Jitter–18.432 MHz	20	120	200	ps
t_9	Clock Jitter–peak-peak	Cycle-Cycle Jitter–54 MHz	40	150	250	ps
t_9	Clock Jitter–peak-peak	Cycle-Cycle Jitter–13.5 MHz	20	120	200	ps

Note:
2. Guaranteed by characterization, not 100% tested.

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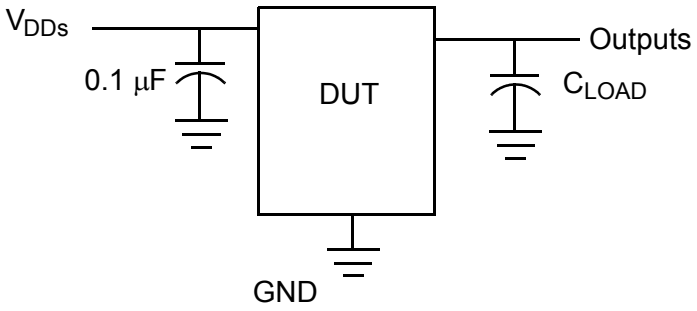
Test and Measurement Set-up



Voltage and Timing Definitions

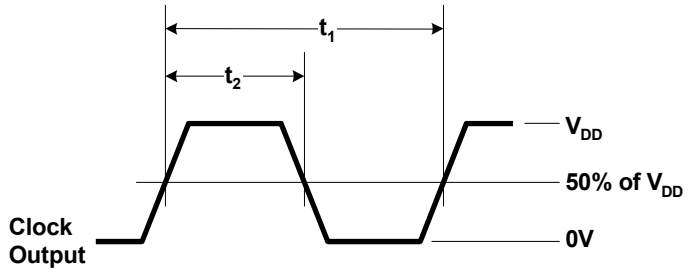


Figure 1. Duty Cycle Definition

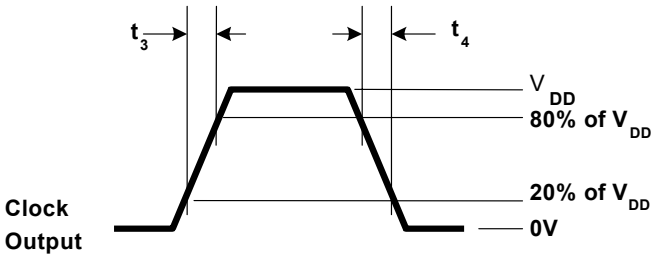


Figure 2. ER = (0.6 x V_{DD}) /t3, EF = (0.6 x V_{DD}) /t4

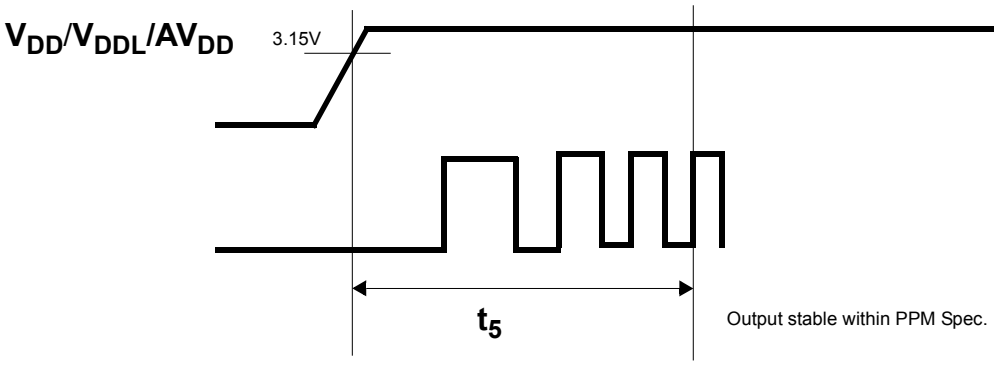


Figure 3. PLL Lock Time

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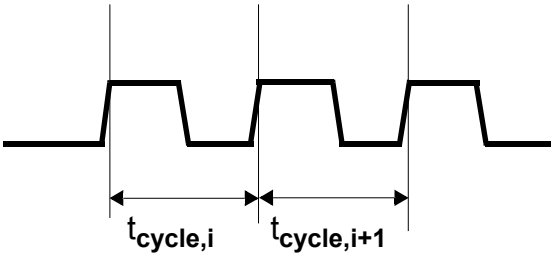
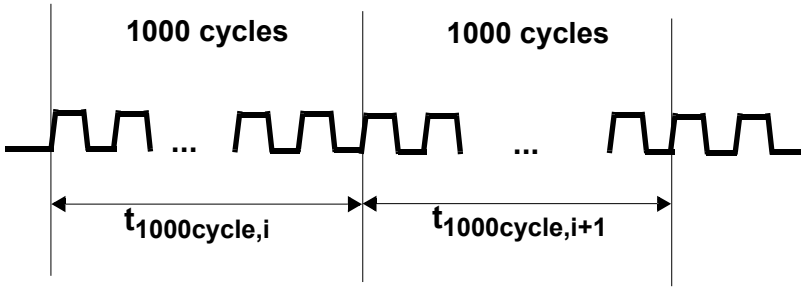


$t_6 = t_{cycle,i} - t_{cycle,i+1}$

Figure 4. 54MOUT, LCLK Cycle-to-Cycle Jitter



$t_7 = t_{1000cycle,i} - t_{1000cycle,i+1}$

Figure 5. 54MOUT, LCLK 1000 Cycle Jitter

Ordering Information

Ordering Code	Package Type	Operating Range	Operating Voltage
Standard			
CY24142ZC-01	16-pin TSSOP	Commercial	3.45V
CY24142ZC-01T	16-pin TSSOP – Tape and Reel	Commercial	3.45V
Lead-free			
CY24142ZXC-01	16-pin TSSOP	Commercial	3.45V
CY24142ZXC-01T	16-pin TSSOP – Tape and Reel	Commercial	3.45V

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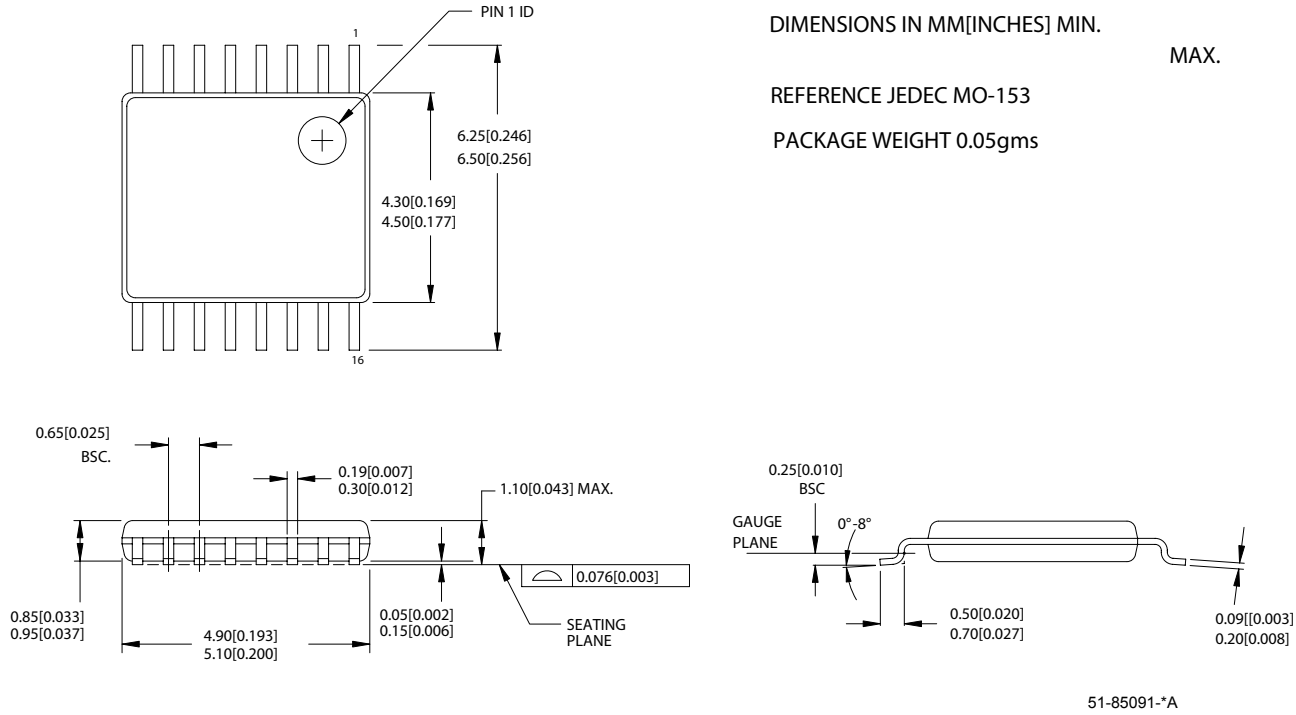
Package Drawing and Dimensions

16-lead TSSOP 4.40 MM Body Z16.173



DIMENSIONS IN MM[INCHES] MIN.

MAX.

REFERENCE JEDEC MO-153

PACKAGE WEIGHT 0.05gms

51-85091-*A

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Document History Page

Document Title: CY24142 MediaClock™ Multimedia Clock Generator Document Number: 38-07532				
REV.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	127352	09/08/03	RGL	New Data Sheet
*A	130343	10/13/03	RGL	Changed the part number from CY24142-1 to CY24142-01.
*B	310574	See ECN	RGL	Added Lead-free

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