

Three-PLL Programmable Clock Generator with Spread Spectrum

Features

- Three fully integrated phase-locked loops (PLLs)
 - Input frequency range
 - External crystal: 8 to 48 MHz
 - External reference: 8 to 166 MHz clock
 - Reference clock input voltage range
 - 2.5 V, 3.0 V, and 3.3 V for CY25483
 - 1.8 V for CY25403 and CY25423
 - Wide operating output frequency range
 - 3 to 166 MHz
 - Programmable spread spectrum with center and down spread option and lexmark and linear modulation profiles
 - V_{DD} supply voltage options
 - 2.5 V, 3.0 V, and 3.3 V for CY25403 and CY25483
 - 1.8 V for CY25423
 - Frequency select feature with option to select four different frequencies
 - Power-down, output enable, and SS ON/OFF controls
 - Low jitter, high accuracy outputs
 - Ability to synthesize nonstandard frequencies with Fractional-N capability
 - Three clock outputs with programmable drive strength
 - Glitch-free outputs while frequency switching

- 8-pin SOIC package
- Commercial and Industrial temperature ranges
- One-time programmability
 - For programming support, contact [Cypress technical support](#) or send an e-mail to clocks@cypress.com

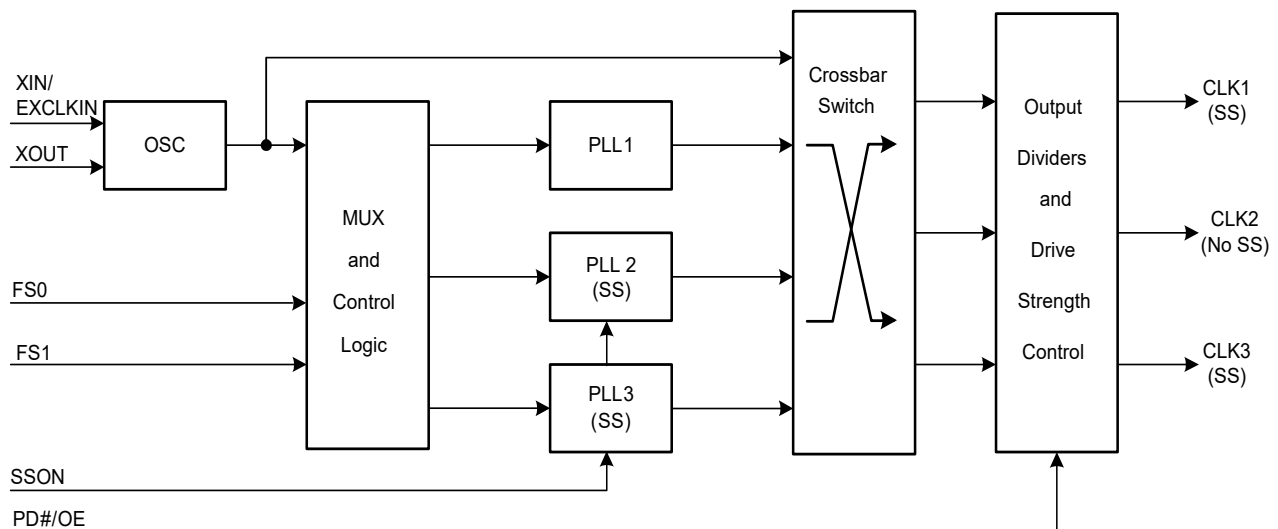
Benefits

- Multiple high-performance PLLs allow synthesis of unrelated frequencies
- Nonvolatile programming for personalization of PLL frequencies, spread spectrum characteristics, drive strength, crystal load capacitance, and output frequencies
- Application specific programmable EMI reduction using Spread Spectrum for clocks
- Programmable PLLs for system frequency margin tests
- Meets critical timing requirements in complex system designs
- Suitability for PC, consumer, portable, and networking applications
- Capable of Zero PPM frequency synthesis error
- Uninterrupted system operation during clock frequency switch
- Application compatibility in standard and low-power systems

Functional Description

For a complete list of related documentation, click [here](#).

Block Diagram



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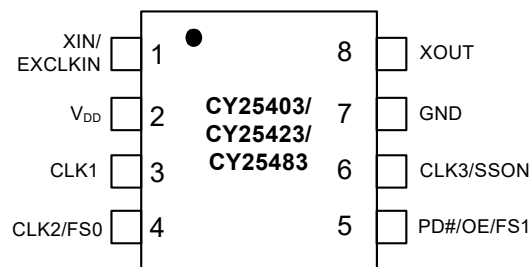
Device Selector Guide

| Device | Crystal Input | EXCLKIN Input | V _{DD} |
|---------|---------------|----------------------------|---------------------|
| CY25403 | Yes | 1.8 V LVCMOS | 2.5 V, 3.0 V, 3.3 V |
| CY25483 | No | 2.5 V, 3.0 V, 3.3 V LVCMOS | 2.5 V, 3.0 V, 3.3 V |
| CY25423 | Yes | 1.8 V LVCMOS | 1.8 V |

Pin Configuration

Figure 1. 8-pin SOIC pinout

CY25403/CY25423/CY25483



Pin Definitions

CY25403/CY25423/CY25483

| Pin Number | Name | IO | Description |
|------------|-----------------|--------------|--|
| 1 | XIN/EXCLKIN | Input | Crystal input or external clock input (Refer Device Selector Guide on page 3) |
| 2 | V _{DD} | Power | Power supply (Refer Device Selector Guide on page 3) |
| 3 | CLK1 | Output | Programmable clock output with spread spectrum |
| 4 | CLK2/FS0 | Output/Input | Multifunction programmable pin: programmable clock output with no spread spectrum or frequency select pin |
| 5 | PD#/OE/FS1 | Input | Multifunction programmable pin: power-down, output enable, or frequency select pin |
| 6 | CLK3/SSON | Output/Input | Multifunction programmable pin: programmable clock output with spread spectrum or spread spectrum ON/OFF control pin |
| 7 | GND | Power | Power supply ground |
| 8 | XOUT | Output | Crystal output |

Functional Overview

Configurable PLLs

The CY25403/CY25423/CY25483 have three programmable PLLs that can be used to generate output frequencies ranging from 3 to 166 MHz. The advantage of having three PLLs is that a single device generates up to three independent frequencies from a single crystal.

Input Reference Clocks

The input reference clock can be either a crystal or a clock signal, for CY25403 and CY25423 while just a clock signal for CY25483. The input frequency range for crystal (XIN) is 8 MHz to 48 MHz and that for external reference clock (EXCLKIN) is 8 MHz to 166 MHz. The voltage range of the reference clock input for CY25483 is 2.5 V/3.0 V/3.3 V while that for CY25403 and CY25423 is 1.8 V. This gives user an option for this device to be compatible for different input clock voltage levels in the system.

V_{DD} Power Supply Options

These devices have programmable power supply options. The CY25403/CY25483 is a high voltage part that can be programmed to operate at any voltage 2.5 V, 3.0 V, or 3.3 V while CY25423 is a low voltage part that can operate at 1.8 V.

These devices have programmable input sources for each of its clock outputs. There are four available clock sources and these clock sources are: XIN/EXCLKIN, PLL1, PLL2, and PLL3. Output clock source selection is done by using four out of four crossbar switch. Thus, any one of these four available clock sources can be arbitrarily selected for the clock outputs. This gives user a flexibility to have up to three independent clock outputs.

Spread Spectrum Control

Two of the three PLLs (PLL2 and PLL3) have spread spectrum capability for EMI reduction in the system. The device uses a Cypress proprietary PLL and spread spectrum clock (SSC) technology to synthesize and modulate the frequency of the PLL. The spread spectrum feature can be turned on or off using a multifunction control pin (CLK3/SSON). It can be programmed to either center spread range from $\pm 0.125\%$ to $\pm 2.50\%$ or down spread range from -0.25% to -5.0% with Lexmark or Linear profile.

Frequency Select

Each PLL can be programmed for up to four different frequencies. There are two multifunction programmable pins, CLK2/FS0 and PD#/OE/FS1 which if programmed as frequency select inputs, can be used to select among these arbitrarily programmed frequency settings. Each output has programmable output divider options.

Glitch-Free Frequency Switch

When the frequency select pin, FS(1:0) is used to switch frequency, the outputs are glitch-free provided frequency is switched using output dividers. This feature enables uninterrupted system operation while clock frequency is being switched.

PD#/OE Mode

Multifunction pin PD#/OE/FS1 (Pin 5) can be programmed to operate as either frequency select (FS1), power-down (PD#) or output enable (OE) mode. PD# is a low-true input. If activated it shuts off the entire chip, resulting in minimum power consumption for the device. Setting this signal high brings the device in the operational mode with default register settings.

When this pin is programmed as output enable (OE), clock outputs can be enabled or disabled using OE (pin 5). Individual clock outputs can be programmed to be sensitive to this OE pin.

Output Drive Strength

The DC drive strength of the individual clock output can be programmed for different values. Table 1 shows the typical rise and fall times for different drive strength settings.

Table 1. Output Drive Strength

| Output Drive Strength | Rise/Fall Time (ns) (Typical Value) |
|-----------------------|--|
| Low | 6.8 |
| Mid Low | 3.4 |
| Mid High | 2.0 |
| High | 1.0 |

Generic Configuration and Custom Frequency

There is a generic set of output frequencies available from the factory that can be used for the device evaluation purposes. The device, CY25403/CY25423/CY25483 can be custom programmed to any desired frequencies and listed features. For customer specific programming, contact your local Cypress Field Application Engineer (FAE) or sales representative.

Absolute Maximum Conditions

| Parameter | Description | Condition | Min | Max | Unit |
|--------------------|---|-----------------------------|------|-----------------------|-------|
| V _{DD} | Supply voltage for CY25403/CY25483 | – | –0.5 | 4.5 | V |
| | Supply voltage for CY25423 | – | –0.5 | 2.6 | |
| V _{IN} | Input voltage for CY25403/CY25423/CY25483 | Relative to V _{SS} | –0.5 | V _{DD} + 0.5 | V |
| T _S | Temperature, Storage | Non Functional | –65 | +150 | °C |
| ESD _{HBM} | ESD protection (human body model) | JEDEC EIA/JESD22-A114-E | 2000 | | Volts |
| UL-94 | Flammability rating | V-0 at 1/8 in. | – | 10 | ppm |
| MSL | Moisture sensitivity level | SOIC package | | –3 | – |

Recommended Operating Conditions

| Parameter | Description | Min | Typ | Max | Unit |
|-------------------|--|------|-----|------|------|
| V _{DD} | V _{DD} operating voltage for CY25403/CY25483 | 2.25 | – | 3.60 | V |
| | V _{DD} operating voltage for CY25423 | 1.65 | 1.8 | 1.95 | |
| T _{AC} | Commercial ambient temperature | 0 | – | +70 | °C |
| T _{AI} | Industrial ambient temperature | –40 | -- | +85 | °C |
| C _{LOAD} | Maximum load capacitance | – | – | 15 | pF |
| t _{PU} | Power-up time for all V _{DD} to reach minimum specified voltage (power ramps must be monotonic) | 0.05 | – | 500 | ms |

DC Electrical Specifications

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|-----------------------------------|---|--|-----------------------|-----|-----------------------|------|
| V _{OL} | Output low voltage | I _{OL} = 2 mA, drive strength = [00] | – | – | 0.4 | V |
| | | I _{OL} = 3 mA, drive strength = [01] | | | | |
| | | I _{OL} = 7 mA, drive strength = [10] | | | | |
| | | I _{OL} = 12 mA, drive strength = [11] | | | | |
| V _{OH} | Output high voltage | I _{OH} = –2 mA, drive strength = [00] | V _{DD} – 0.4 | – | – | V |
| | | I _{OH} = –3 mA, drive strength = [01] | | | | |
| | | I _{OH} = –7 mA, drive strength = [10] | | | | |
| | | I _{OH} = –12 mA, drive strength = [11] | | | | |
| V _{IL1} | Input low voltage of PD#/OE, FS0, FS1 and SSON | | – | – | 0.2 × V _{DD} | V |
| V _{IL2} | Input low voltage of EXCLKIN for CY25403/CY25423 | | – | – | 0.3 | V |
| V _{IL3} | Input low voltage of EXCLKIN for CY25483 | | – | – | 0.2 × V _{DD} | V |
| V _{IH1} | Input high voltage of PD#/OE, FS0, FS1 and SSON | | 0.8 × V _{DD} | – | – | V |
| V _{IH2} | Input high voltage of EXCLKIN for CY25403/CY25483 | | 1.62 | – | 2.2 | V |
| V _{IH3} | Input high voltage of EXCLKIN for CY25423 | | 0.8 × V _{DD} | – | – | V |
| I _{IL} | Input low current, PD#/OE/FS1 | V _{IN} = 0 V | – | – | 10 | μA |
| I _{IH} | Input high current, PD#/OE/FS1 | V _{IN} = V _{DD} | – | – | 10 | μA |
| I _{ILDN} | Input low current, SSON and FS0 pins | V _{IN} = 0 V (Internal pull-down resistor = 160k typ.) | – | – | 10 | μA |
| I _{IHDN} | Input high current, SSON and FS0 pins | V _{IN} = V _{DD} (Internal pull-down resistor = 160k typ.) | 14 | – | 36 | μA |
| R _{DN} | Pull-down resistor of CLK1, CLK2/FS0 and CLK3/SSON pins | Output clocks in off state by setting PD# = Low | 100 | 160 | 250 | kΩ |
| I _{DD} ^[1, 2] | Supply current for CY25403/CY25423/CY25483 | PD# = High, No load | – | 22 | – | mA |
| I _{DDS} ^[1] | Standby current | PD# = Low | – | 3 | – | μA |
| C _{IN} ^[1] | Input capacitance | SSON, PD#/OE/FS1 and FS0 pins | – | – | 7 | pF |

Thermal Resistance

| Parameter ^[3] | Description | Test Conditions | 8-pin SOIC | Unit |
|--------------------------|--|---|------------|------|
| θ _{JA} | Thermal resistance (junction to ambient) | Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51. | 131 | °C/W |
| θ _{JC} | Thermal resistance (junction to case) | | 40 | °C/W |

Notes

- Guaranteed by design but not 100% tested.
- Configuration dependent.
- These parameters are guaranteed by design and are not tested.

AC Electrical Specifications

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|------------------------------------|--|---|-----|-----|-----|------|
| F _{IN} (crystal) | Crystal frequency, XIN | – | 8 | – | 48 | MHz |
| F _{IN} (clock) | Input clock frequency (EXCLKIN) | – | 8 | – | 166 | MHz |
| F _{CLK} | Output clock frequency | – | 3 | – | 166 | MHz |
| DC | Output duty cycle, all clocks except ref out | Duty Cycle is defined in Figure 3 on page 9 ; t ₁ /t ₂ , measured at 50% of V _{DD} | 45 | 50 | 55 | % |
| DC | Ref out duty cycle | Ref In Min 45%, Max 55% | 40 | – | 60 | % |
| T _{RF1} ^[4] | Output rise/fall time | Measured from 20% to 80% of V _{DD} , as shown in Figure 4 on page 9 , CL = 15 pF, drive strength [00] | – | 6.8 | – | ns |
| T _{RF2} ^[4] | Output rise/fall time | Measured from 20% to 80% of V _{DD} , as shown in Figure 4 on page 9 , CL = 15 pF, drive strength [01] | – | 3.4 | – | ns |
| T _{RF3} ^[4] | Output rise/fall time | Measured from 20% to 80% of V _{DD} , as shown in Figure 4 on page 9 , CL = 15 pF, drive strength [10] | – | 2.0 | – | ns |
| T _{RF4} ^[4] | Output rise/fall time | Measured from 20% to 80% of V _{DD} , as shown in Figure 4 on page 9 , CL = 15 pF, drive strength [11] | – | 1.0 | – | ns |
| T _{CCJ} ^[4, 5] | Cycle-to-cycle jitter (peak) | Configuration dependent. See Configuration Example on page 8 | – | 100 | – | ps |
| T _{LOCK} ^[4] | PLL lock time | Measured from 90% of the applied power supply level | – | 1 | 3 | ms |

Notes

4. Guaranteed by design but not 100% tested.
5. Configuration dependent.

Configuration Example

For C-C Jitter

| Ref. Frequency (MHz) | CLK1 Output | | CLK2 Output | | CLK3 Output | |
|----------------------|-------------|---------------------|-------------|---------------------|-------------|---------------------|
| | Freq. (MHz) | C-C Jitter Typ (ps) | Freq. (MHz) | C-C Jitter Typ (ps) | Freq. (MHz) | C-C Jitter Typ (ps) |
| 14.3181 | 8.0 | 134 | 166 | 103 | 48 | 92 |
| 19.2 | 74.25 | 99 | 166 | 94 | 8 | 91 |
| 27 | 48 | 67 | 27 | 109 | 166 | 103 |
| 48 | 48 | 93 | 27 | 123 | 166 | 137 |

Recommended Crystal Specification

For SMD Package

| Parameter | Description | Range 1 | Range 2 | Range 3 | Unit |
|-----------|-----------------------------|---------|---------|---------|----------|
| Fmin | Minimum frequency | 8 | 14 | 28 | MHz |
| Fmax | Maximum frequency | 14 | 28 | 48 | MHz |
| R1 | Motional resistance (ESR) | 135 | 50 | 30 | Ω |
| C0 | Shunt capacitance | 4 | 4 | 2 | pF |
| CL | Parallel load capacitance | 18 | 14 | 12 | pF |
| DL(max) | Maximum crystal drive level | 300 | 300 | 300 | μ W |

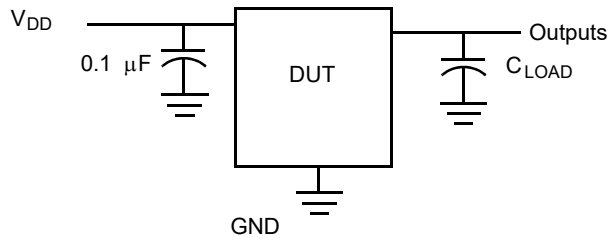
Recommended Crystal Specification

For Thru-Hole Package

| Parameter | Description | Range 1 | Range 2 | Range 3 | Unit |
|-----------|-----------------------------|---------|---------|---------|----------|
| Fmin | Minimum frequency | 8 | 14 | 24 | MHz |
| Fmax | Maximum frequency | 14 | 24 | 32 | MHz |
| R1 | Motional resistance (ESR) | 90 | 50 | 30 | Ω |
| C0 | Shunt capacitance | 7 | 7 | 7 | pF |
| CL | Parallel load capacitance | 18 | 12 | 12 | pF |
| DL(max) | Maximum crystal drive level | 1000 | 1000 | 1000 | μ W |

Test and Measurement Setup

Figure 2. Test and Measurement Setup



Voltage and Timing Definitions

Figure 3. Duty Cycle Definition

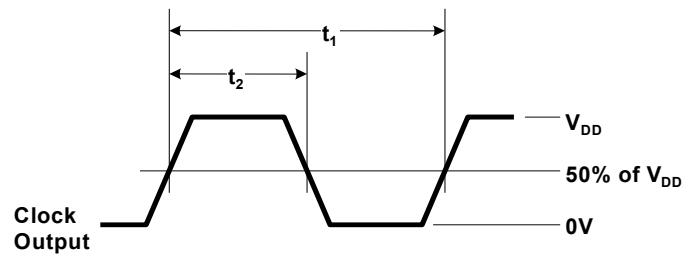
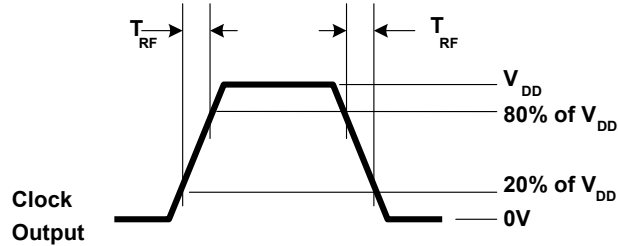


Figure 4. Rise Time = T_{RF} , Fall Time = T_{RF}



Ordering Information

| Part Number | Type | Package | Supply Voltage | Production Flow |
|-------------------|--|----------------------------|------------------------|------------------------------|
| Pb-free | | | | |
| CY25403SXC | Field Programmable | 8-pin SOIC | 2.5 V, 3.0 V, or 3.3 V | Commercial, 0 °C to 70 °C |
| CY25403SXCT | Field Programmable | 8-pin SOIC – Tape and Reel | 2.5 V, 3.0 V, or 3.3 V | Commercial, 0 °C to 70 °C |
| CY25423SXC | Field Programmable | 8-pin SOIC | 1.8 V | Commercial, 0 °C to 70 °C |
| CY25423SXCT | Field Programmable | 8-pin SOIC – Tape and Reel | 1.8 V | Commercial, 0 °C to 70 °C |
| CY25483SXC | Field Programmable | 8-pin SOIC | 2.5 V, 3.0 V, or 3.3 V | Commercial, 0 °C to 70 °C |
| CY25483SXCT | Field Programmable | 8-pin SOIC – Tape and Reel | 2.5 V, 3.0 V, or 3.3 V | Commercial, 0 °C to 70 °C |
| CY25403SXI | Field Programmable | 8-pin SOIC | 2.5 V, 3.0 V, or 3.3 V | Industrial, –40 °C to +85 °C |
| CY25403SXIT | Field Programmable | 8-pin SOIC – Tape and Reel | 2.5 V, 3.0 V, or 3.3 V | Industrial, –40 °C to +85 °C |
| CY25423SXI | Field Programmable | 8-pin SOIC | 1.8 V | Industrial, –40 °C to +85 °C |
| CY25423SXIT | Field Programmable | 8-pin SOIC – Tape and Reel | 1.8 V | Industrial, –40 °C to +85 °C |
| CY25483SXI | Field Programmable | 8-pin SOIC | 2.5 V, 3.0 V, or 3.3 V | Industrial, –40 °C to +85 °C |
| CY25483SXIT | Field Programmable | 8-pin SOIC – Tape and Reel | 2.5 V, 3.0 V, or 3.3 V | Industrial, –40 °C to +85 °C |
| Programmer | | | | |
| CY3675-CLKMAKER1 | Programming Kit | | | |
| CY3675-SOIC8A | Socket Adapter Board, for programming CY25402, CY25403, CY25422, CY25423, CY25482, and CY25483 | | | |

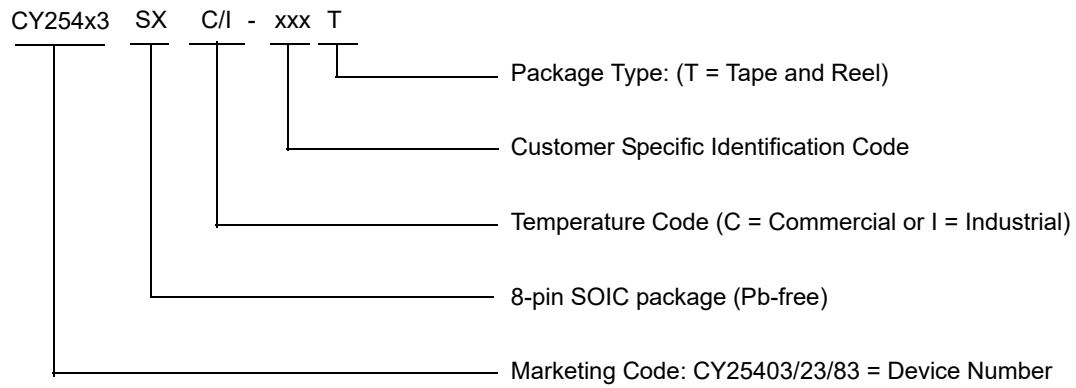
Some product offerings are factory programmed customer specific devices with customized part numbers. The [Possible Configurations](#) table shows the available device types, but not complete part numbers. Contact your local Cypress FAE or sales representative for more information.

Possible Configurations

| Part Number ^[6] | Type | V _{DD} (V) | Production Flow |
|---------------------------------|----------------------------|--|------------------------------|
| Pb-free | | | |
| CY25403/CY25423/CY25483SXC-xxx | 8-pin SOIC | Supply Voltage: 2.5 V, 3.0 V, or 3.3 V | Commercial, 0 °C to 70 °C |
| CY25403/CY25423/CY25483SXC-xxxT | 8-pin SOIC – Tape and Reel | Supply Voltage: 2.5 V, 3.0 V, or 3.3 V | Commercial, 0 °C to 70 °C |
| CY25403/CY25423/CY25483SXI-xx | 8-pin SOIC | Supply Voltage: 2.5 V, 3.0 V, or 3.3 V | Industrial, –40 °C to +85 °C |
| CY25403/CY25423/CY25483SXI-xxT | 8-pin SOIC – Tape and Reel | Supply Voltage: 2.5 V, 3.0 V, or 3.3 V | Industrial, –40 °C to +85 °C |

Note

6. xxx indicates factory programmed parts based on customer specific configuration. For more details, contact your local Cypress FAE or sales representative.

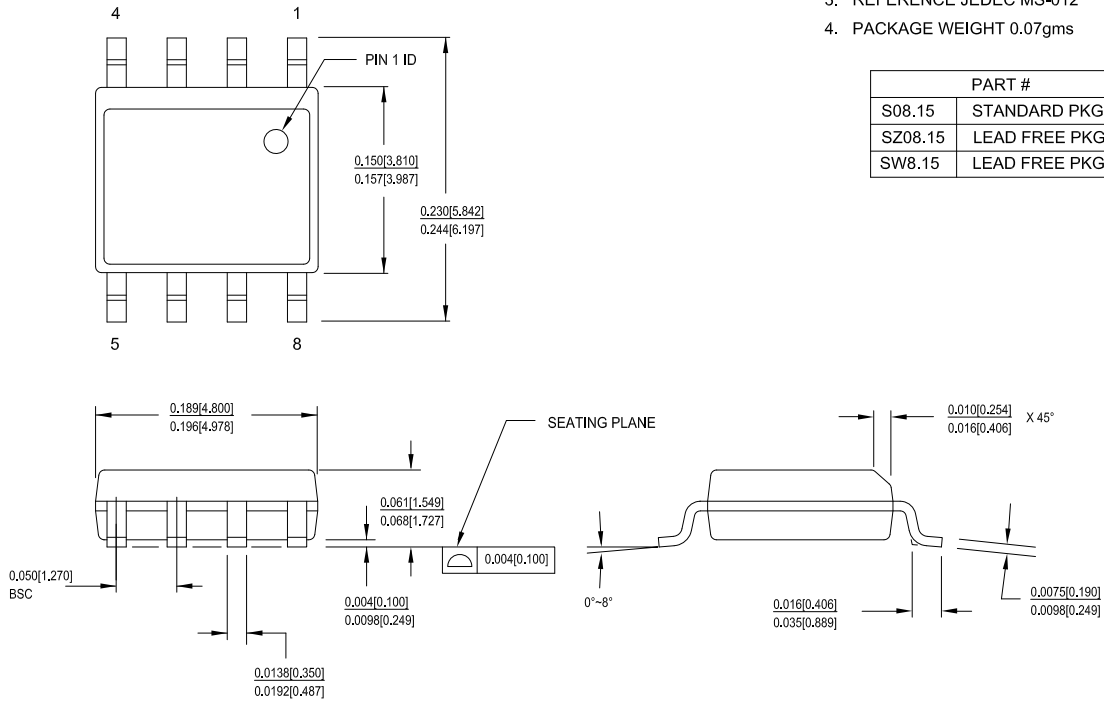
Ordering Code Definitions

Package Drawing and Dimensions

Figure 5. 8-pin SOIC (150 Mils) S0815/SZ815/SW815 Package Outline, 51-85066

1. DIMENSIONS IN INCHES[MM] MIN. MAX.
2. PIN 1 ID IS OPTIONAL, ROUND ON SINGLE LEADFRAME RECTANGULAR ON MATRIX LEADFRAME
3. REFERENCE JEDEC MS-012
4. PACKAGE WEIGHT 0.07gms

| PART # | |
|---------|---------------|
| S08.15 | STANDARD PKG |
| SZ08.15 | LEAD FREE PKG |
| SW8.15 | LEAD FREE PKG |



51-85066 *I

Acronyms

| Acronym | Description |
|---------|---|
| DL | drive level |
| DNU | do not use |
| DUT | device under test |
| EIA | Electronic Industries Alliance |
| EMI | electromagnetic interference |
| ESD | electrostatic discharge |
| FAE | field application engineer |
| FS | frequency select |
| JEDEC | Joint Electron Devices Engineering Council |
| LVC MOS | low voltage complementary metal oxide semiconductor |
| OE | output enable |
| OSC | oscillator |
| PD | power-down |
| PLL | phase-locked loop |
| PPM | parts per million |
| SS | spread spectrum |
| SSC | spread spectrum clock |
| SSON | spread spectrum on |

Document Conventions

Units of Measure

| Symbol | Unit of Measure |
|--------|-----------------|
| °C | degree Celsius |
| MHz | megahertz |
| μA | microampere |
| mA | milliampere |
| ms | millisecond |
| ns | nanosecond |
| pF | picofarad |
| ps | picosecond |
| V | volt |

Document History Page

| Document Title: CY25403/CY25423/CY25483, Three-PLL Programmable Clock Generator with Spread Spectrum Document Number: 001-12564 | | | | |
|--|---------|-----------------|-----------------|--|
| Rev. | ECN No. | Orig. of Change | Submission Date | Description of Change |
| ** | 690296 | RGL | 01/17/2007 | New data sheet. |
| *A | 815788 | RGL | 03/02/2007 | Minor Change: To post on web. |
| *B | 1428744 | RGL / AESA | 08/30/2007 | Updated Document Title to read as "CY25403/CY25423/CY25483 Three PLL Programmable Clock Generator with Spread Spectrum". Changed status from Preliminary to Final. Added CY25483 part related information in all instances across the document. Updated Block Diagram . Updated Pin Definitions: Updated details in "Description" column. Updated Functional Overview : Updated description and added sub-sections. Updated Absolute Maximum Conditions : Updated details corresponding to V_{DD} and V_{IN} parameters. Updated Recommended Operating Conditions : Updated details corresponding to V_{DD} parameter. Updated DC Electrical Specifications : Updated almost entire table. Updated Ordering Information : Updated part numbers. |
| *C | 2748211 | TSAI | 08/10/2009 | Post to external web. |
| *D | 2899300 | CXQ | 03/25/2010 | Updated Ordering Information : Added Possible Configurations . Added Note 6 and referred the same note in "Part Number" column. Updated Package Drawing and Dimensions : spec 51-85066 – Changed revision from *C to *D. |
| *E | 2898568 | CXQ | 06/02/2010 | Updated Ordering Information : Updated part numbers. Added Ordering Code Definitions . Added Acronyms . Updated to new template. |
| *F | 3319132 | BASH | 07/18/2011 | Updated Package Drawing and Dimensions : spec 51-85066 – Changed revision from *D to *E. Added Units of Measure . Updated to new template. |

Document History Page *(continued)*

| Document Title: CY25403/CY25423/CY25483, Three-PLL Programmable Clock Generator with Spread Spectrum Document Number: 001-12564 | | | | |
|--|---------|-----------------|-----------------|---|
| Rev. | ECN No. | Orig. of Change | Submission Date | Description of Change |
| *G | 4468493 | TAVA | 08/12/2014 | Updated Features : Updated details under “Reference clock input voltage range”, “V _{DD} supply voltage options:”, and “Selectable output clock voltages independent of V _{DD} supply:”. Updated Device Selector Guide : Updated details in “Crystal Input”, “EXCLKIN Input” and “V _{DD} ” columns. Updated Pin Definitions : Updated details in “Description” column corresponding to pin numbers 1 and 2. Updated Functional Overview : Updated Input Reference Clocks : Updated description. Updated VDD Power Supply Options : Updated description. Updated Absolute Maximum Conditions : Updated details corresponding to V _{DD} parameter. Updated Recommended Operating Conditions : Updated details corresponding to V _{DD} parameter. Updated DC Electrical Specifications : Updated details corresponding to V _{IH2} parameter. Added V _{IH3} parameter and its details. Updated Package Drawing and Dimensions : spec 51-85066 – Changed revision from *E to *F. Updated to new template. Completing Sunset Review. |
| *H | 4586478 | TAVA | 12/03/2014 | Updated Functional Description : Added “For a complete list of related documentation, click here .” at the end. |
| *I | 5279365 | PSR | 05/20/2016 | Added Thermal Resistance . Updated Package Drawing and Dimensions : spec 51-85066 – Changed revision from *F to *H. Updated to new template. Completing Sunset Review. |
| *J | 5778174 | PSR | 06/19/2017 | Updated Features : Added one-time programmability. |
| *K | 5952739 | XHT | 10/31/2017 | Updated DC Electrical Specifications : Updated details in “Description” and “Max” columns corresponding to V _{IL2} parameter. Added V _{IL3} parameter and its details. Updated Package Drawing and Dimensions : spec 51-85066 – Changed revision from *H to *I. Updated to new template. |

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